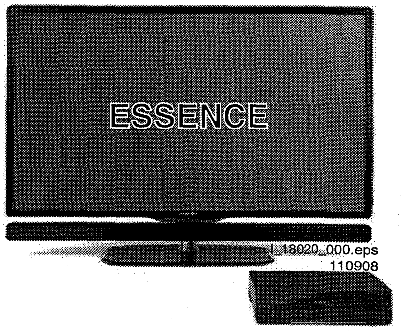
Colour Television

Chassis

Q529.1E

LC

Service
Service
Service



Service Manual

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PHILIPS

1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

1.1 Technical Specifications
1.2 Connections
1.3 Chassis Overview

Notes:
- Figures can deviate due to the different set executions.
- Specifications are indicative (subject to change).

1.1 Technical Specifications

1.1.1 Vision

Display type	: LCD
Screen size	: 42" (107 cm), 16:9
Resolution (H × V pixels)	: 1920 × 1080
Min. light output (cd/m^2)	: 500
Min. contrast ratio	: 66000 : 1
Max. response time (ms)	: 2
Viewing angle (H × V degrees)	: 176 × 176
Tuning system	: PLL
TV Colour systems	: PAL B/G, D/K, I
	: SECAM B/G, D/K, L/L'
	: DVB-T
	: DVB-C (optional)
	: MPEG4 (optional)
Video playback	: NTSC, PAL, SECAM
Tuner bands	: UHF, VHF, S, Hyper
Supported video formats	
- 60 Hz	: 480i
- 60 Hz	: 480p
- 50 Hz	: 576i
- 50 Hz	: 576p
- 50, 60 Hz	: 720p
- 50, 60 Hz	: 1080i
- 24, 25, 30, 50, 60 Hz	: 1080p
Supported computer formats:	
- 60 Hz	: 640 × 480
- 60 Hz	: 800 × 600
- 60 Hz	: 1024 × 768
- 60 Hz	: 1280 × 768
- 60 Hz	: 1360 × 768
- 60 Hz	: 1920 × 1080i
- 60 Hz	: 1920 × 1080p
Presets/channels	: automatic channel management
Tuner bands	: VHF
	: UHF
	: S-band
	: Hyper-band

1.1.2 Sound

Sound systems	: Virtual Dolby Digital
	: BBE
Maximum power (W_{RMS})	: 2 × 15

1.1.3 Multimedia

Supported formats	: Slideshow.alb files
	: MPEG1
	: MPEG2
	: MP3
	: JPEG
USB input	: USB1.1 (12 Mbps)
	: USB2.0 (480 Mbps)
Network	: DLNA PC Network link

1.1.4 Miscellaneous

Power supply:	
- Mains voltage (V_{AC})	: 220 - 240 ±10%
- Mains frequency (Hz)	: 50 / 60
Ambient conditions:	
- Temperature range (°C)	: +5 to +35
	: 90% R.H.
Power consumption (values are indicative)	
- Normal operation (W)	: ≈248
- Standby (W)	: < 0.40
Hub dimensions (W × H × D in mm)	: 320 × 84 × 320
Hub weight (kg)	: 4.7
Screen dimensions (W × H × D in mm)	: 982 × 662.5 × 49.8
Screen weight (kg)	: 16.5

1.2 Connections

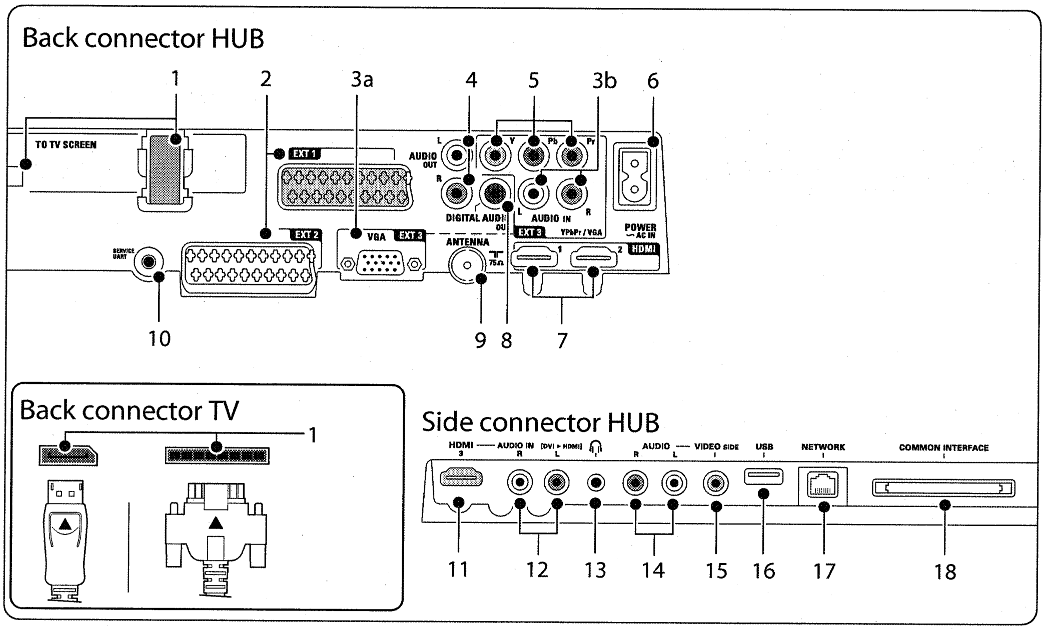
Back connector HUB
1
2
3a
4
5
3b
6
TO TV SCREEN
EXT 1
AUDIO OUT
L
R
Y
Pb
Pr
DIGITAL AUDIO OUT
L
AUDIO IN
R
EXT 2
VGA
EXT 3
ANTENNA
75Ω
EXT 3
YPbPr / VGA
1
2
HDMI
POWER ~ AC IN
SERVICE UART
10
9
8
7
Back connector TV
1
Side connector HUB
HDMI 3
AUDIO IN R
[DVI > HDMI] L
AUDIO R
L
VIDEO SIDE
USB
NETWORK
COMMON INTERFACE
11
12
13
14
15
16
17
18

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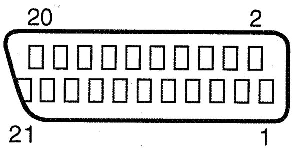
Figure 1-1 Connection overview

Note: The following connector colour abbreviations are used (acc. to DIN/IEC 757): Bk= Black, Bu= Blue, Gn= Green, Gy= Grey, Rd= Red, Wh= White, Ye= Yellow.

1.2.1 Connections

1 - Single cable connectors
Dedicated for Essence

2 - EXT1, EXT2: Video YPbPr - In, CVBS - In/Out, Audio - In/Out



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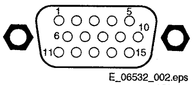
050404

Figure 1-2 SCART connector

1	- Audio R	0.5 V_{RMS} / 1 kohm	○→
2	- Audio R	0.5 V_{RMS} / 10 kohm	→○
3	- Audio L	0.5 V_{RMS} / 1 kohm	○→
4	- Ground Audio	Gnd	⏚
5	- Ground Blue	Gnd	⏚
6	- Audio L	0.5 V_{RMS} / 10 kohm	→○
7	- Video Pb	0.7 V_{PP} / 75 ohm	→○
8	- Function Select	0 - 2 V: INT 4.5 - 7 V: EXT 16:9 9.5 - 12 V: EXT 4:3	→○
9	- Ground	Gnd	⏚
10	- n.c.		
11	- Video Y	1 V_{PP} / 75 ohm	→○
12	- n.c.		
13	- Ground	Gnd	⏚
14	- Ground	Gnd	⏚
15	- Video Pr	0.7 V_{PP} / 75 ohm	→○
16	- Status/FBL	0 - 0.4 V: INT 1 - 3 V: EXT / 75 ohm	→○
17	- Ground Video	Gnd	⏚
18	- Ground FBL	Gnd	⏚
19	- Video CVBS	1 V_{PP} / 75 ohm	○→
20	- Video CVBS/Y	1 V_{PP} / 75 ohm	→○
21	- Shield	Gnd	⏚

3a - EXT 3 VGA: Video RGB - In



E_06532_002.eps
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Figure 1-3 VGA Connector

1	- Video Red	0.7 V_{PP} / 75 Ω	→○
2	- Video Green	0.7 V_{PP} / 75 Ω	→○
3	- Video Blue	0.7 V_{PP} / 75 Ω	→○
4	- n.c.		
5	- Ground	Gnd	⏚
6	- Ground Red	Gnd	⏚
7	- Ground Green	Gnd	⏚
8	- Ground Blue	Gnd	⏚
9	- +5V_{DC}	+5 V	→○
10	- Ground Sync	Gnd	⏚
11	- n.c.		
12	- DDC_SDA	DDC data	→○
13	- H-sync	0 - 5 V	→○
14	- V-sync	0 - 5 V	→○
15	- DDC_SCL	DDC clock	→○

3b - Cinch: Audio - In

Rd - Audio R	0.5 V_{RMS} / 10 kΩ	→○◎
Wh - Audio L	0.5 V_{RMS} / 10 kΩ	→○◎

4 - Cinch: Audio - Out

Rd - Audio - R	0.5 V_{RMS} / 10 kΩ	○→◎
Wh - Audio - L	0.5 V_{RMS} / 10 kΩ	○→◎

5 - Cinch: Video YPbPr - In

Gn	- Video Y	1 V_{PP} / 75 Ω	→○◎
Bu	- Video Pb	0.7 V_{PP} / 75 Ω	→○◎
Rd	- Video Pr	0.7 V_{PP} / 75 Ω	→○◎

7, 11 - HDMI 1, 2, 3 Digital Video, Digital Audio - In

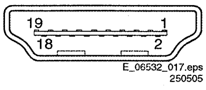

Figure 1-4 HDMI (type A) connector

1	- D2+	Data channel	→○
2	- Shield	Gnd	⏚
3	- D2-	Data channel	→○
4	- D1+	Data channel	→○
5	- Shield	Gnd	⏚
6	- D1-	Data channel	→○
7	- D0+	Data channel	→○
8	- Shield	Gnd	⏚
9	- D0-	Data channel	→○
10	- CLK+	Data channel	→○
11	- Shield	Gnd	⏚
12	- CLK-	Data channel	→○
13	- Easylink	Control channel	→○○→
14	- n.c.		
15	- DDC_SCL	DDC clock	→○
16	- DDC_SDA	DDC data	→○○→
17	- Ground	Gnd	⏚
18	- +5V		→○
19	- HPD	Hot Plug Detect	→○
20	- Ground	Gnd	⏚

8 - Cinch: S/PDIF - Out

Bk	- Coaxial	0.4 - 0.6V_{PP} / 75 Ω	○→◎

9 - Aerial - In

-	- IEC-type (EU)	Coax, 75 Ω	╦

10 - Service Connector (UART)

1	- Ground	Gnd	⏚
2	- UART_TX	Transmit	○→
3	- UART_RX	Receive	→○

12 - Cinch: Audio - In

Rd	- Audio - R	0.5 V_{RMS} / 10 kΩ	→○◎
Wh	- Audio - L	0.5 V_{RMS} / 10 kΩ	→○◎

13 - Headphone (Output)

Bk	- Headphone	32 - 600 Ω / 10 mW	◎ 3.5mm 🎧

14 - Cinch: Audio - In

Rd	- Audio - R	0.5 V_{RMS} / 10 kΩ	→○◎
Wh	- Audio - L	0.5 V_{RMS} / 10 kΩ	→○◎

15 - Cinch: Video CVBS - In, Audio - In

Ye	- Video CVBS	1 V_{PP} / 75 Ω	→○◎

16 - USB2.0

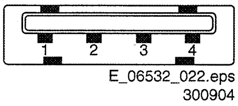

Figure 1-5 USB (type A)

1	- +5V		○→
2	- Data (-)		→○○→
3	- Data (+)		→○○→
4	- Ground	Gnd	⏚

17 - RJ45: Ethernet

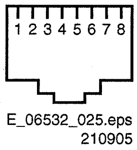

Figure 1-6 Ethernet connector

1	- TD+	Transmit signal	○→
2	- TD-	Transmit signal	○→
3	- RD+	Receive signal	→○
4	- n.c.		
5	- n.c.		
6	- RD-	Receive signal	→○
7	- n.c.		
8	- n.c.		

18 - Common Interface

68p	- See diagram B03H	→○○→

1.3 Chassis Overview

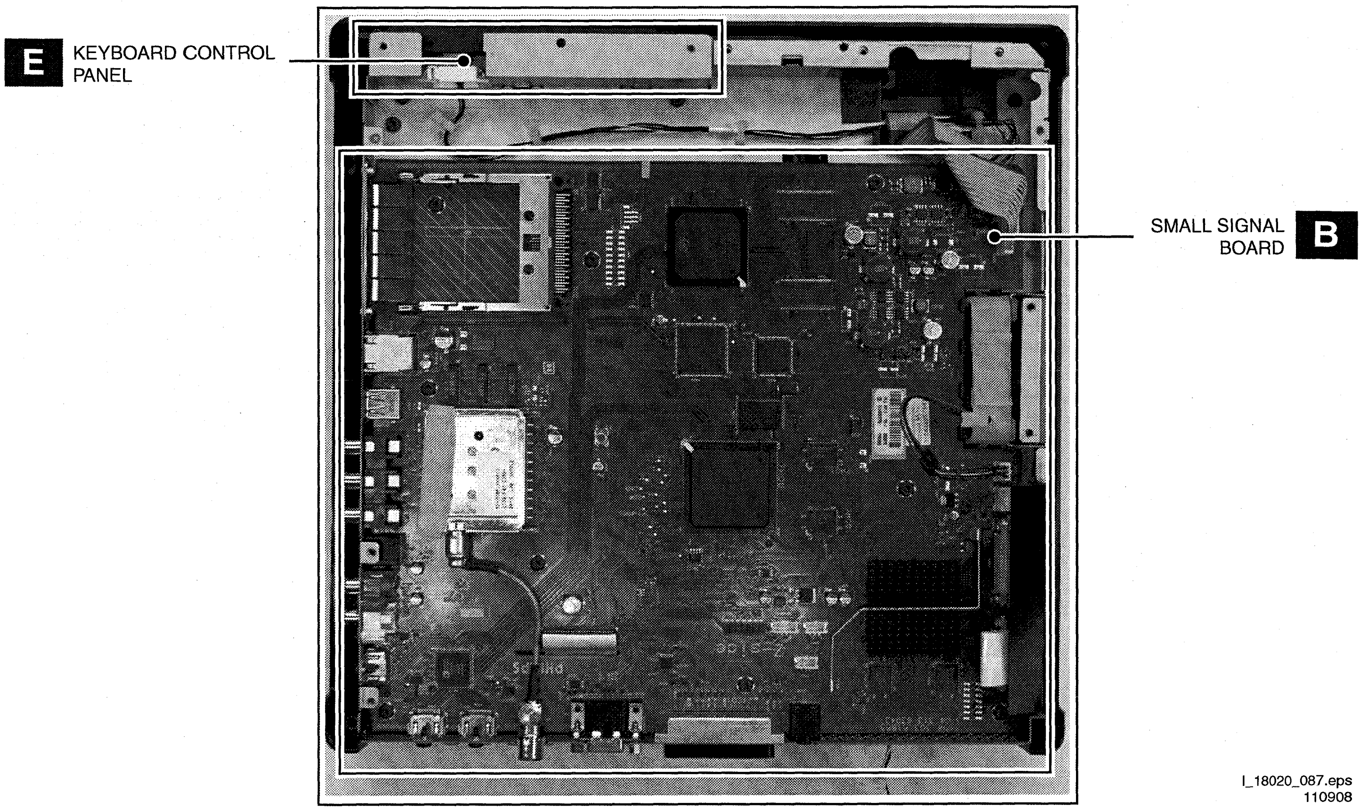
E
KEYBOARD CONTROL PANEL
SMALL SIGNAL BOARD
B

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Figure 1-7 PWB/CBA locations Hub -1-

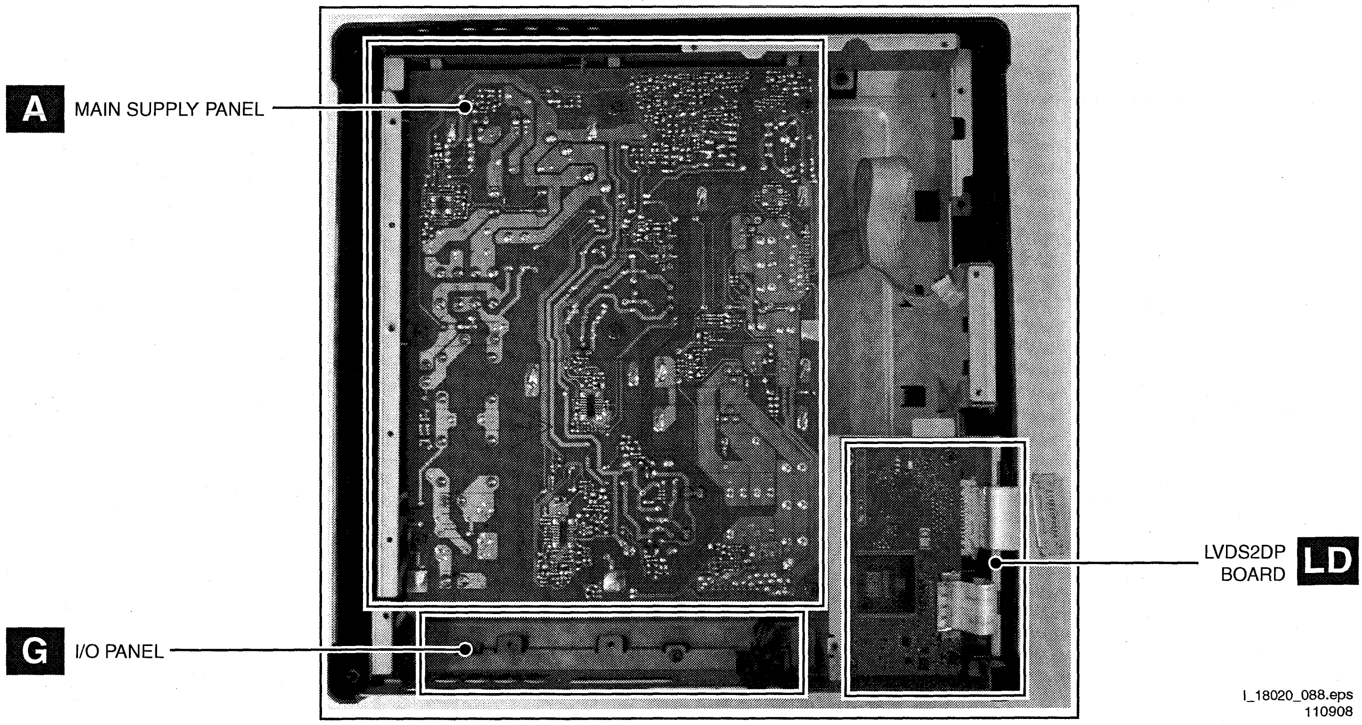
A
MAIN SUPPLY PANEL
LVDS2DP BOARD
LD
G
I/O PANEL

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Figure 1-8 PWB/CBA locations Hub -2-

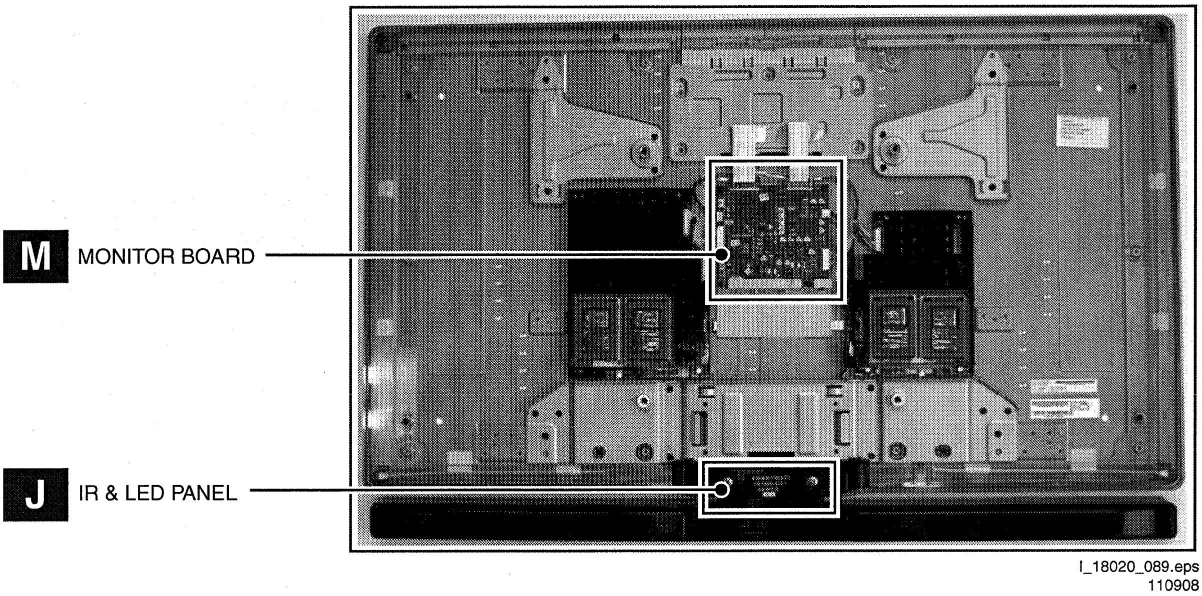
M MONITOR BOARD
J IR & LED PANEL
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Figure 1-9 PWB/CBA locations Monitor

2. Safety Instructions, Warnings, and Notes

Index of this chapter:
2.1 Safety Instructions
2.2 Warnings
2.3 Notes

2.1 Safety Instructions

Safety regulations require the following **during** a repair:

- Connect the set to the Mains/AC Power via an isolation transformer (> 800 VA).
- Replace safety components, indicated by the symbol ⚠, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that **after** a repair, the set must be returned in its original condition. Pay in particular attention to the following points:

- Route the wire trees correctly and fix them with the mounted cable clamps.
- Check the insulation of the Mains/AC Power lead for external damage.
- Check the strain relief of the Mains/AC Power cord for proper function.
- Check the electrical DC resistance between the Mains/AC Power plug and the secondary side (only for sets that have a Mains/AC Power isolated power supply):
  1. Unplug the Mains/AC Power cord and connect a wire between the two pins of the Mains/AC Power plug.
  2. Set the Mains/AC Power switch to the "on" position (keep the Mains/AC Power cord unplugged!).
  3. Measure the resistance value between the pins of the Mains/AC Power plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 MΩ and 12 MΩ.
  4. Switch "off" the set, and remove the wire between the two pins of the Mains/AC Power plug.
- Check the cabinet for defects, to prevent touching of any inner parts by the customer.

2.2 Warnings

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD ⚠). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.
- Be careful during measurements in the high voltage section.
- Never replace modules or other components while the unit is switched "on".
- When you align the set, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

2.3 Notes

2.3.1 General

- Measure the voltages and waveforms with regard to the chassis (= tuner) ground (⏚), or hot ground (⏚), depending on the tested area of circuitry. The voltages and waveforms shown in the diagrams are indicative. Measure them in the Service Default Mode (see chapter 5) with a colour bar signal and stereo sound (L: 3 kHz, R: 1 kHz unless stated otherwise) and picture carrier at 475.25 MHz for PAL, or 61.25 MHz for NTSC (channel 3).
- Where necessary, measure the waveforms and voltages with (⊓⊏) and without (⌧) aerial signal. Measure the voltages in the power supply section both in normal operation (⏽) and in stand-by (⏻). These values are indicated by means of the appropriate symbols.
- Manufactured under license from Dolby Laboratories. "Dolby", "Pro Logic" and the "double-D symbol", are trademarks of Dolby Laboratories.

2.3.2 Schematic Notes

- All resistor values are in ohms, and the value multiplier is often used to indicate the decimal point location (e.g. 2K2 indicates 2.2 kΩ).
- Resistor values with no multiplier may be indicated with either an "E" or an "R" (e.g. 220E or 220R indicates 220 Ω).
- All capacitor values are given in micro-farads ($\mu = \times 10^{-6}$), nano-farads ($n = \times 10^{-9}$), or pico-farads ($p = \times 10^{-12}$).
- Capacitor values may also use the value multiplier as the decimal point indication (e.g. 2p2 indicates 2.2 pF).
- An "asterisk" (*) indicates component usage varies. Refer to the diversity tables for the correct values.
- The correct component values are listed in the Spare Parts List. Therefore, always check this list when there is any doubt.

2.3.3 BGA (Ball Grid Array) ICs

Introduction
For more information on how to handle BGA devices, visit this URL: *www.atyourservice.ce.philips.com* (needs subscription, not available for all regions). After login, select "Magazine", then go to "Repair downloads". Here you will find Information on how to deal with BGA-ICs.

BGA Temperature Profiles
For BGA-ICs, you **must** use the correct temperature-profile, which is coupled to the 12NC. For an overview of these profiles, visit the website *www.atyourservice.ce.philips.com* (needs subscription, but is not available for all regions)
You will find this and more technical information within the "Magazine", chapter "Repair downloads".
For additional questions please contact your local repair help desk.

2.3.4 Lead-free Soldering

Due to lead-free technology some rules have to be respected by the workshop during a repair:

- Use only lead-free soldering tin Philips SAC305 with order code 0622 149 00106. If lead-free solder paste is required, please contact the manufacturer of your soldering equipment. In general, use of solder paste within workshops should be avoided because paste is not easy to store and to handle.
- Use only adequate solder tools applicable for lead-free soldering tin. The solder tool must be able:
  - To reach a solder-tip temperature of at least 400°C.
  - To stabilize the adjusted temperature at the solder-tip.
  - To exchange solder-tips for different applications.
- Adjust your solder tool so that a temperature of around 360°C - 380°C is reached and stabilized at the solder joint. Heating time of the solder-joint should not exceed ~ 4 sec. Avoid temperatures above 400°C, otherwise wear-out of tips will increase drastically and flux-fluid will be destroyed. To avoid wear-out of tips, switch "off" unused equipment or reduce heat.
- Mix of lead-free soldering tin/parts with leaded soldering tin/parts is possible but PHILIPS recommends strongly **to**

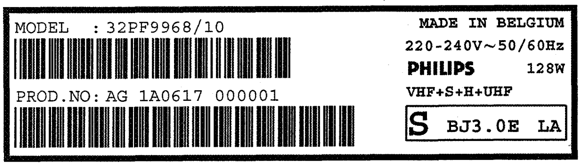
avoid mixed regimes. If this cannot be avoided, carefully clear the solder-joint from old tin and re-solder with new tin.

2.3.5 Alternative BOM identification

It should be noted that on the European Service website, “Alternative BOM” is referred to as “Design variant”.

The **third digit** in the serial number (example: AG**2**B0335000001) indicates the number of the alternative B.O.M. (Bill Of Materials) that has been used for producing the specific TV set. In general, it is possible that the same TV model on the market is produced with e.g. two different types of displays, coming from two different suppliers. This will then result in sets which have the same CTN (Commercial Type Number; e.g. 28PW9515/12) but which have a different B.O.M. number.
By looking at the third digit of the serial number, one can identify which B.O.M. is used for the TV set he is working with. If the third digit of the serial number contains the number “1” (example: AG**1**B033500001), then the TV set has been manufactured according to B.O.M. number 1. If the third digit is a “2” (example: AG**2**B0335000001), then the set has been produced according to B.O.M. no. 2. ***This is important for ordering the correct spare parts!***
For the third digit, the numbers 1...9 and the characters A...Z can be used, so in total: 9 plus 26= 35 different B.O.M.s can be indicated by the third digit of the serial number.

Identification: The bottom line of a type plate gives a 14-digit serial number. Digits 1 and 2 refer to the production center (e.g. AG is Bruges), digit 3 refers to the B.O.M. code, digit 4 refers to the Service version change code, digits 5 and 6 refer to the production year, and digits 7 and 8 refer to production week (in example below it is 2006 week 17). The 6 last digits contain the serial number.



MODEL : 32PF9968/10
PROD.NO: AG 1A0617 000001
MADE IN BELGIUM
220-240V~50/60Hz
PHILIPS 128W
VHF+S+H+UHF
S BJ3.0E LA

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260308

Figure 2-1 Serial number (example)

2.3.6 Board Level Repair (BLR) or Component Level Repair (CLR)

If a board is defective, consult your repair procedure to decide if the board has to be exchanged or if it should be repaired on component level.
If your repair procedure says the board should be exchanged completely, do not solder on the defective board. Otherwise, it cannot be returned to the O.E.M. supplier for back charging!

2.3.7 Practical Service Precautions

- **It makes sense to avoid exposure to electrical shock.** While some sources are expected to have a possible dangerous impact, others of quite high potential are of limited current and are sometimes held in less regard.
- **Always respect voltages.** While some may not be dangerous in themselves, they can cause unexpected reactions that are best avoided. Before reaching into a powered TV set, it is best to test the high voltage insulation. It is easy to do, and is a good service precaution.

3. Directions for Use

Directions for use can be downloaded from the following websites:
http://www.philips.com/support
http://www.p4c.philips.com

4. Mechanical Instructions

Index of this chapter:
4.1 Cable Dressing
4.2 Service Positions
4.3 Assy/Panel Removal Hub
4.4 Assy/Panel Removal Monitor
4.5 Set Re-assembly.

Notes:

- Figures below can deviate slightly from the actual situation, due to the different set executions.

4.1 Cable Dressing

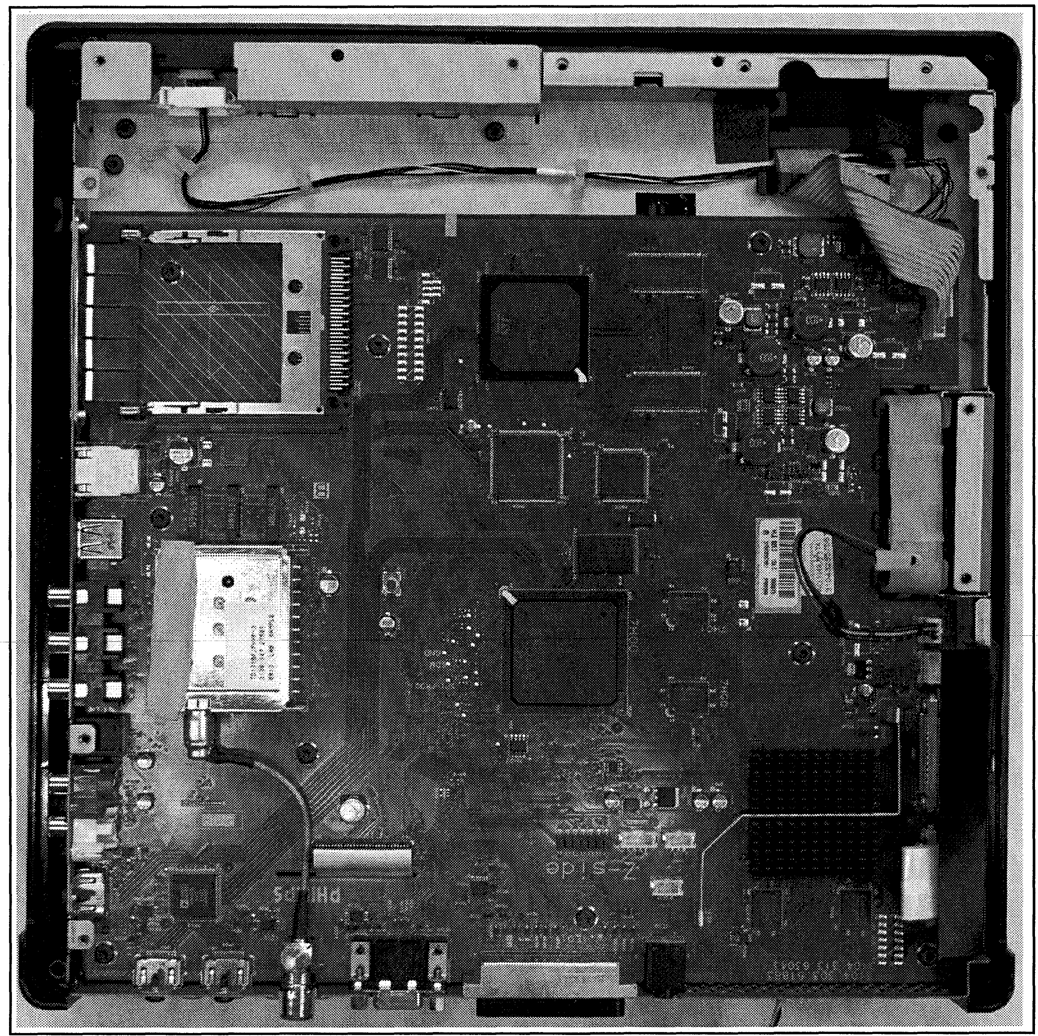

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Figure 4-1 Cable dressing hub; bottom view

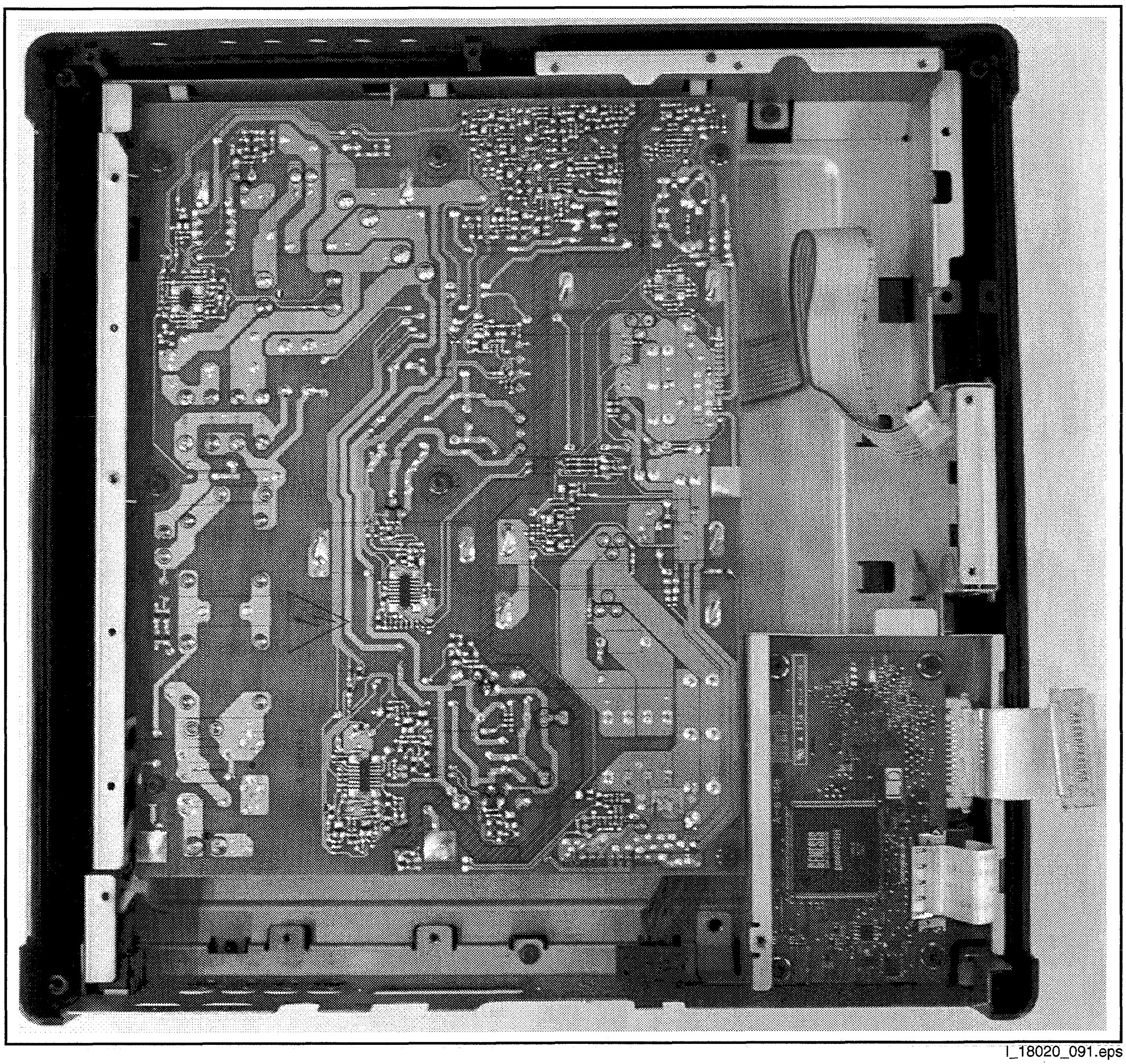

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Figure 4-2 Cable dressing hub; bottom view (SSB removed)

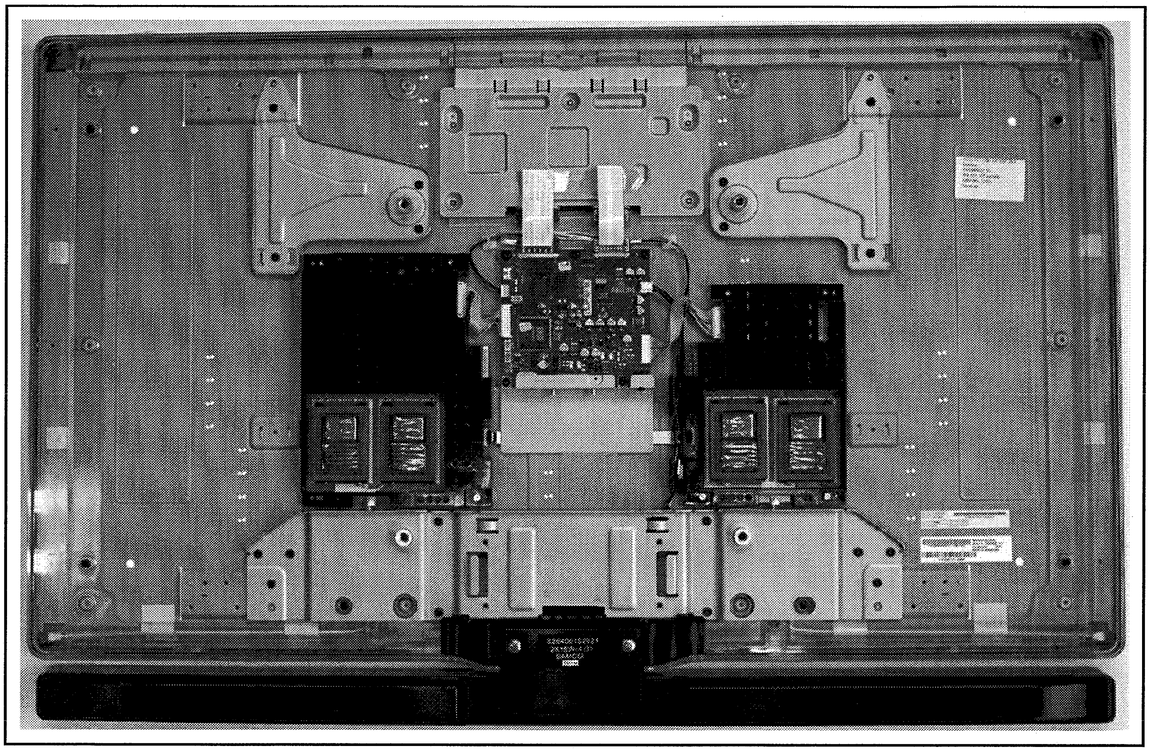

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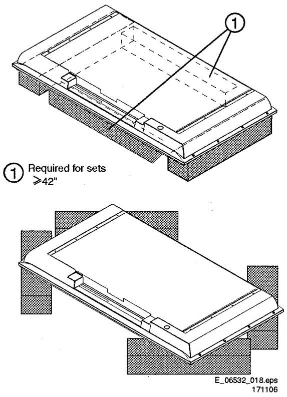
Figure 4-3 Cable dressing monitor

4.2 Service Positions

For easy servicing of the monitor of the set, there are a few possibilities created:

- The buffers from the packaging.
- Foam bars (created for Service).

4.2.1 Foam Bars



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171106

Figure 4-4 Foam bars

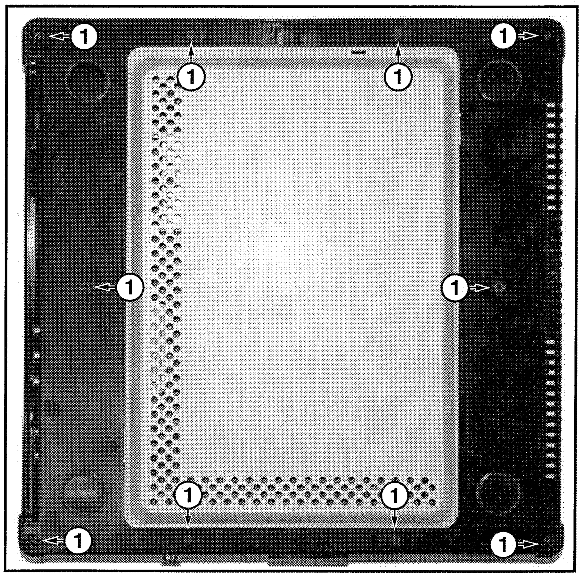
The foam bars (order code 3122 785 90580 for two pieces) can be used for all types and sizes of Flat TVs. See figure "Foam bars" for details. Sets with a display of 42" and larger, require **four** foam bars [1]. Ensure that the foam bars are always supporting the cabinet and **never** only the display.
Caution: Failure to follow these guidelines can seriously damage the display!
By laying the TV face down on the (ESD protective) foam bars, a stable situation is created to perform measurements and alignments. By placing a mirror under the TV, the screen can be monitored.

4.3 Assy/Panel Removal Hub

4.3.1 Bottom Cover and -Shield

Warning: Disconnect the mains power cord before removing the rear cover.
Refer to next figures for details.

1. Place the hub upside-down and remove the bottom cover by removing the screws [1].
2. Remove the bottom shield by removing the screws [2] indicated with an arrow.



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081008

Figure 4-5 Bottom Cover and -Shield -1-

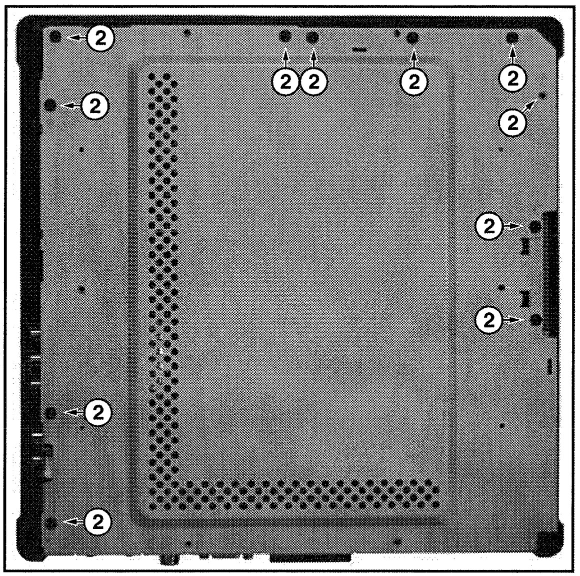

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Figure 4-6 Bottom Cover and -Shield -2-

4.3.2 Key Board

Refer to next figure for details.

1. Unplug the key board connector [1] from the IR & LED board.
2. Remove the screws [2].
3. Lift the unit and take it out of the set.

When defective, replace the whole unit.

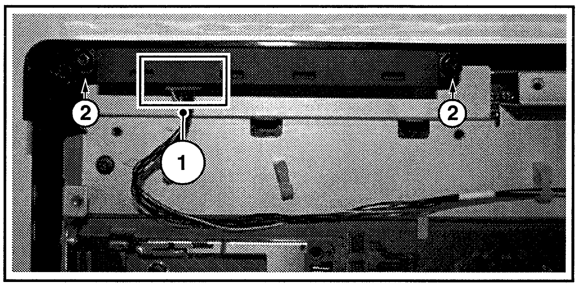

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Figure 4-7 Keyboard Control Panel

4.3.3 Fan

Refer to next figure for details.

1. Unplug connector [1].
2. Lift the fan from the set. During replacement, ensure you replace it at its original position.

When defective, replace the unit.

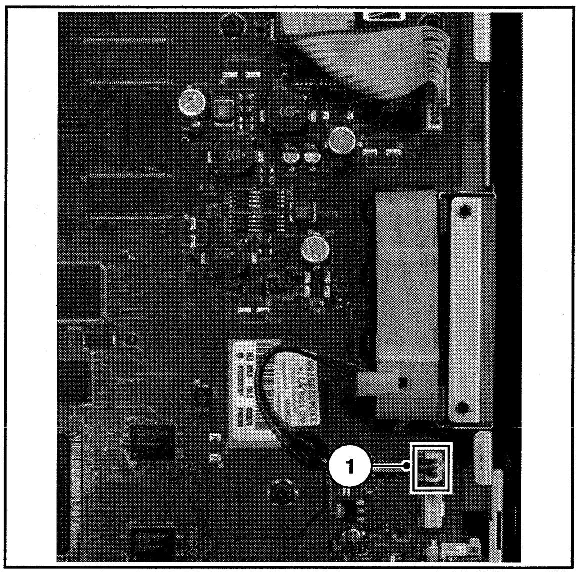

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Figure 4-8 Fan

4.3.4 Small Signal Board (SSB)

Refer to next figures or details.

1. Remove fan.
2. Unplug keyboard cable [1] on SSB.
3. Unplug flat cable [2] on SSB.
4. Unplug two LVDS connectors [3] on SSB. These are very fragile connectors!
5. Lift the flatcable gently with a screwdriver [4] that leads to the underlaying I/O Panel.
6. Remove three screws near side I/O Panel.
7. Remove four screws near back I/O Panel (including the two screws of the VGA connector).
8. Remove all remaining screws that secure the SSB.
9. Slide the SSB sidewards out of the hub.

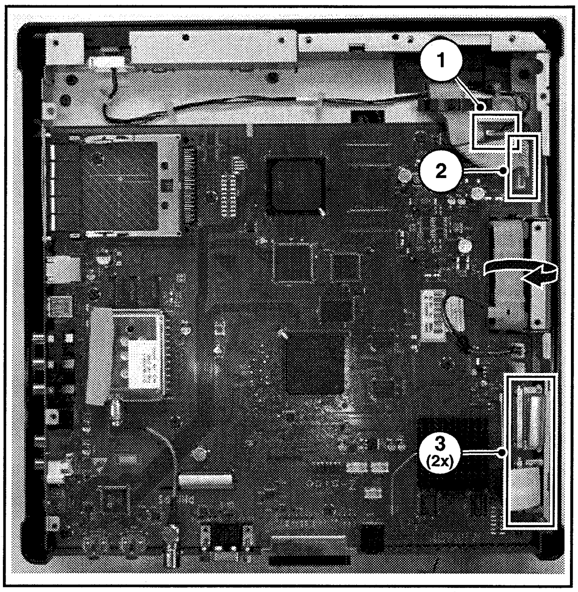

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Figure 4-9 Small Signal Board -1-

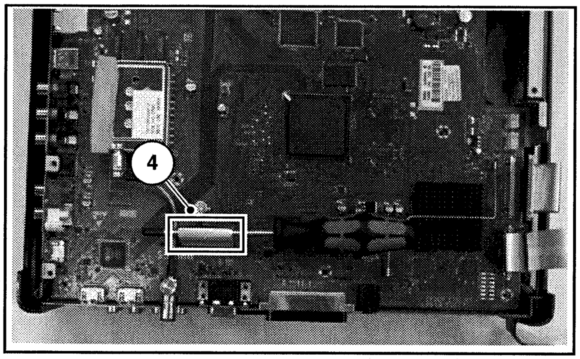

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Figure 4-10 Small Signal Board -2-

4.3.5 Subframe underneath SSB

Refer to next figures for details.

1. Remove keyboard, fan and SSB.
2. Remove two screws [1] on Additional I/O Panel (near cinch plugs).
3. Remove two screw [2] on Additional I/O Panel (near SCART plug).
4. Remove screw [3].
5. Unclamp flat cable coming from Power Supply Unit [4].
6. Take the board out.
7. Remove screws on the subframe indicated with an arrow [5].
8. Lift the subframe on the right side, then lift the subframe forwards, then take the subframe out of the hub.

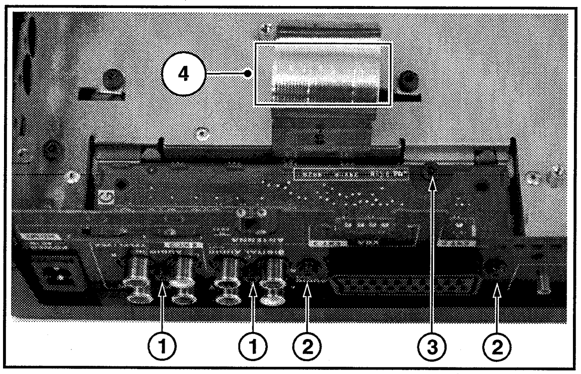

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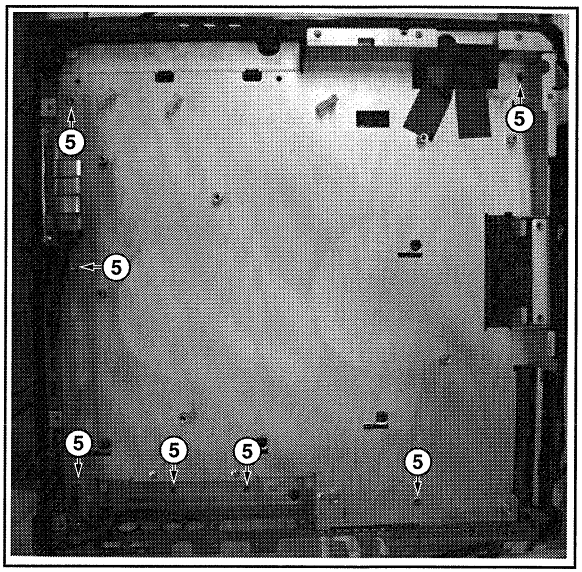
Figure 4-11 Subframe -1-



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151008

Figure 4-12 Subframe -2-

4.3.6 Additional I/O Panel

Refer to section “Subframe underneath SSB”. When defective, replace the whole unit.

4.3.7 Display Port Panel Hub

Refer to next figure for details.

1. Remove screws [1].
2. Unplug the other connectors.
3. Remove all fixation screws.
4. Take the board out.

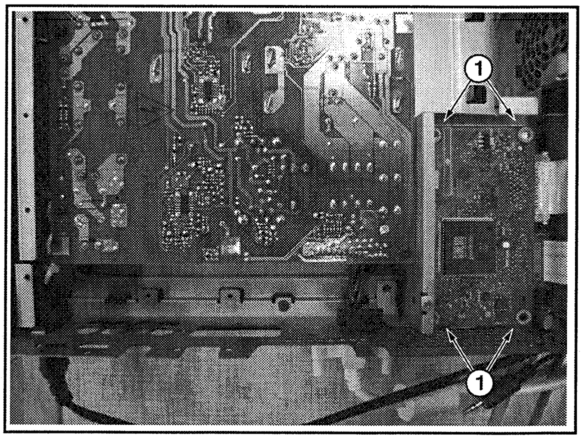

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Figure 4-13 Display Port Panel Hub

4.3.8 Power Supply Unit

Refer to next figure for details.

1. Remove the fixation screws [1].
2. Lift the board.
3. Unplug the connector to the mains inlet.
4. Unplug the connector from the supply connector to the screen.
5. Take the supply out.

When defective, replace the whole unit.

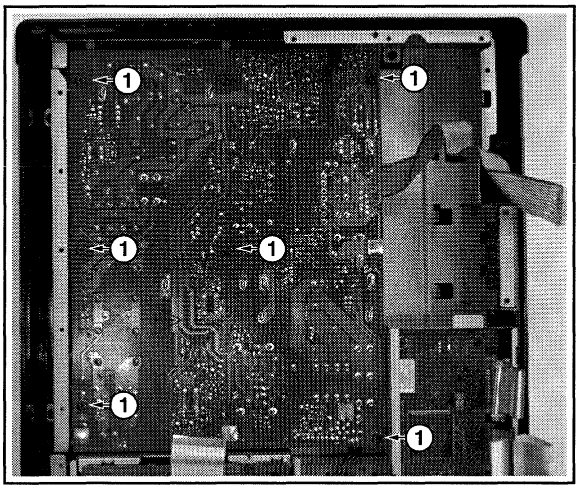

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Figure 4-14 Power Supply Unit

4.4 Assy/Panel Removal Monitor

4.4.1 Sound Interface

Refer to next figure for details.

1. Remove stand (four screws).
2. Lift set from stand.
3. Remove soundbar.
4. Remove sound interface by removing the screws [1].

When defective, replace the whole module.

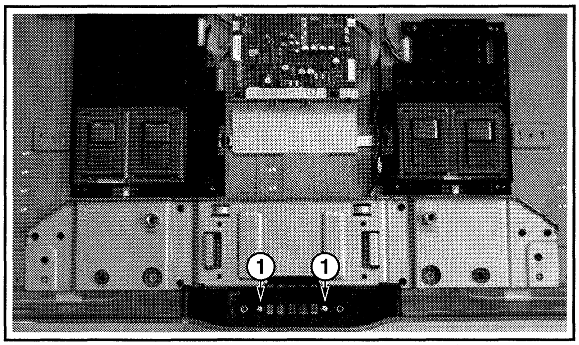

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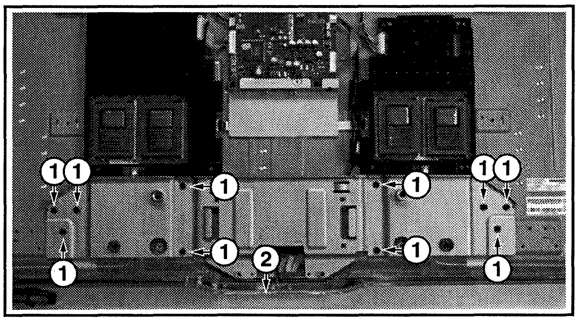
Figure 4-15 Sound Interface

4.4.2 IR & LED Board

Refer to next figures for details.

1. Remove lower part of VESA stand [1].
2. Remove flare [2] (six screws).
3. Unplug connector [3].
4. Remove screws [4].

When defective, replace the whole unit.



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110908

Figure 4-16 IR & LED Panel -1-

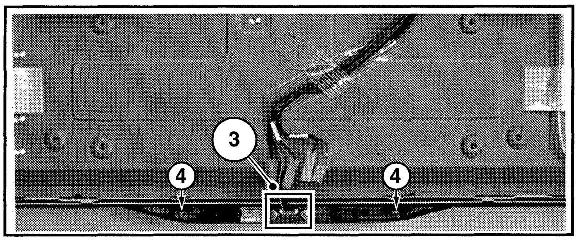

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Figure 4-17 IR & LED Panel -2-

4.4.3 Display Port Panel

Refer to next figure for details.

1. Unplug connectors [1].
2. Unplug LVDS connectors [2]. Be careful, as these are very fragile connectors.
3. Remove screws [3] and subframe [4].
4. Remove screws [5].

When defective, replace the whole unit.

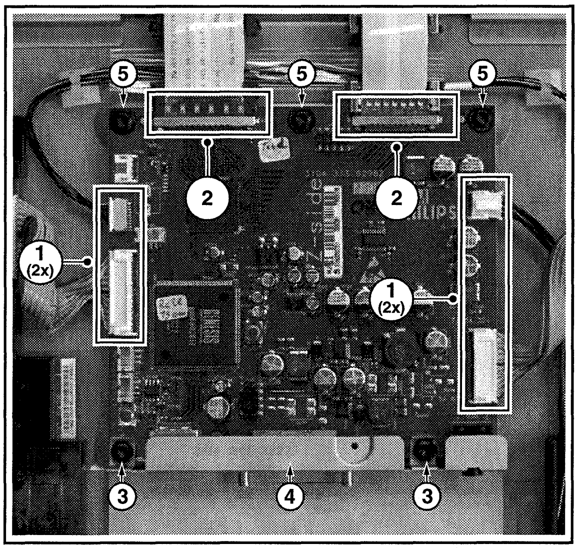

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Figure 4-18 Display Port Panel Monitor

4.4.4 LCD Panel

SPECIAL NOTICE

The dis-assembly, re-assembly and/or exchange of the LCD Panel is an elaborate process. Reason for this is the mounting method of the Panel in the cabinet. Due to physical restraints, no screws could be used, but instead adhesive foams and -tapes are used.

Use gloves where indicated to avoid **personal injury** and **pollution** of the LCD Panel (dust and/or fingerprints).

Exactly **follow the instructions** to avoid **warranty issues**, especially when a defective LCD Panel has to be returned to the supplier.

Step A. to F. describe the removal of the LCD Panel of the cabinet.
Step K. to N. describe the mounting of the LCD Panel back into the cabinet.

Step G. to J. describe which additional actions have to be taken in the event the original LCD Panel has to be replaced.

Additional Spare Parts are needed when remounting the (new) LCD Panel in the cabinet. These spare parts can be ordered as one Service Kit using ordering code 3122 785 91150. The kit contains the following items:

- 5 x Foam L × W × T = 20 × 43 × 0.5 mm.
- 6 x Foam L × W × T = 70 × 50 × 0.5 mm.
- 4 x Foam L × W × T = 30 × 43 × 0.5 mm.
- 1 x Foam L × W × T = 55 × 20 × 0.8 mm.
- 5 x Cable clamp (wire saddle) 11.2 mm.

LCD Panel Removal

A. Refer to next figure for details.

1. Remove stand.
2. Remove soundbar.
3. Remove backcover.
4. Remove sound interface.
5. Remove flare.
6. Remove stand bracket.
7. Remove leading edge.

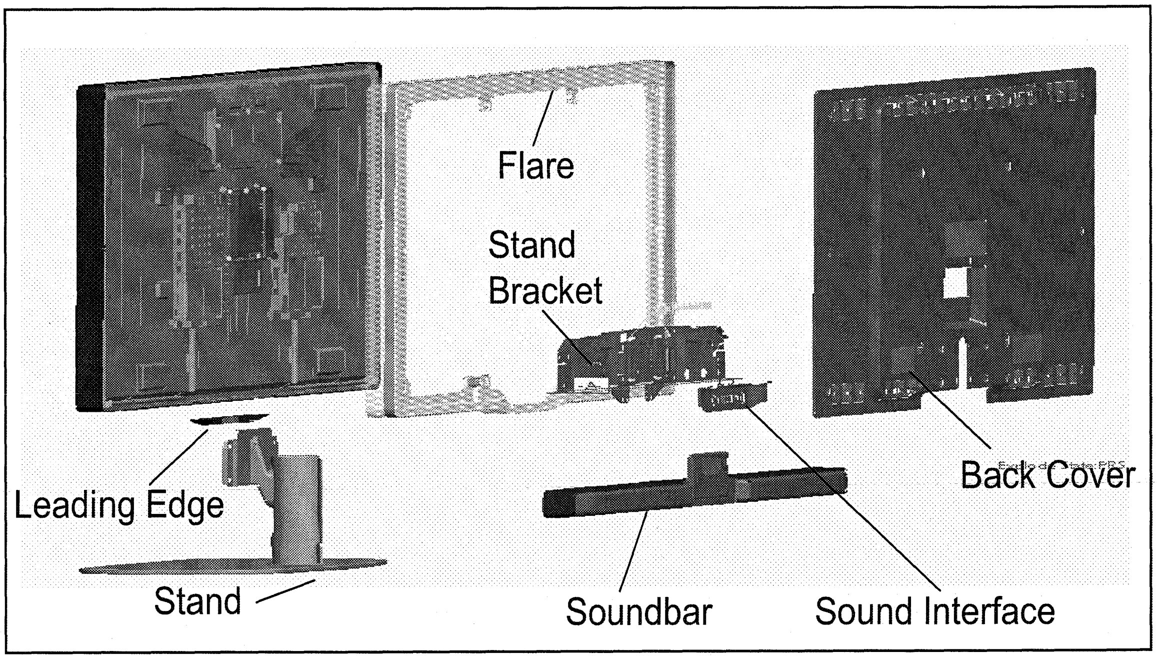

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Figure 4-19 LCD Panel -1-

B. Bend metal lips in each corner of Front open.

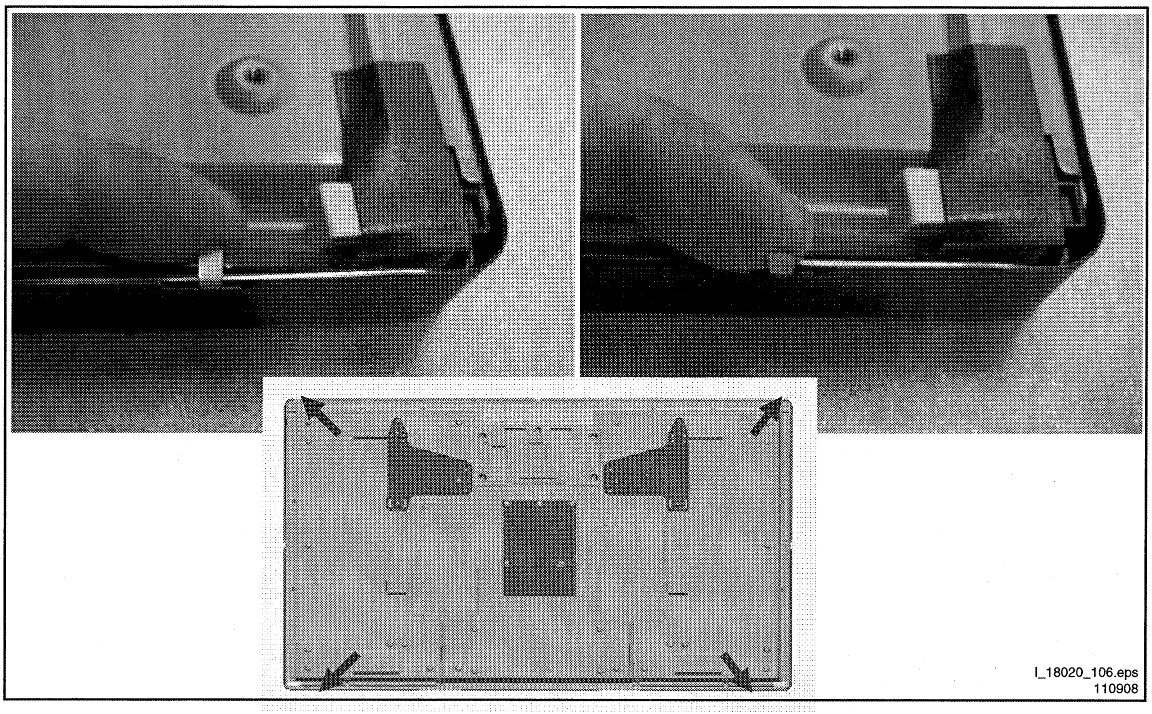
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Figure 4-20 LCD Panel -2-

C. Remove thermal foams (3x) between LCD-panel and upper wall of metal Front.

1. Pull the upper bend open.
2. Move out the thermal foam with e.g. a screwdriver.
3. Pull out the thermal foam.

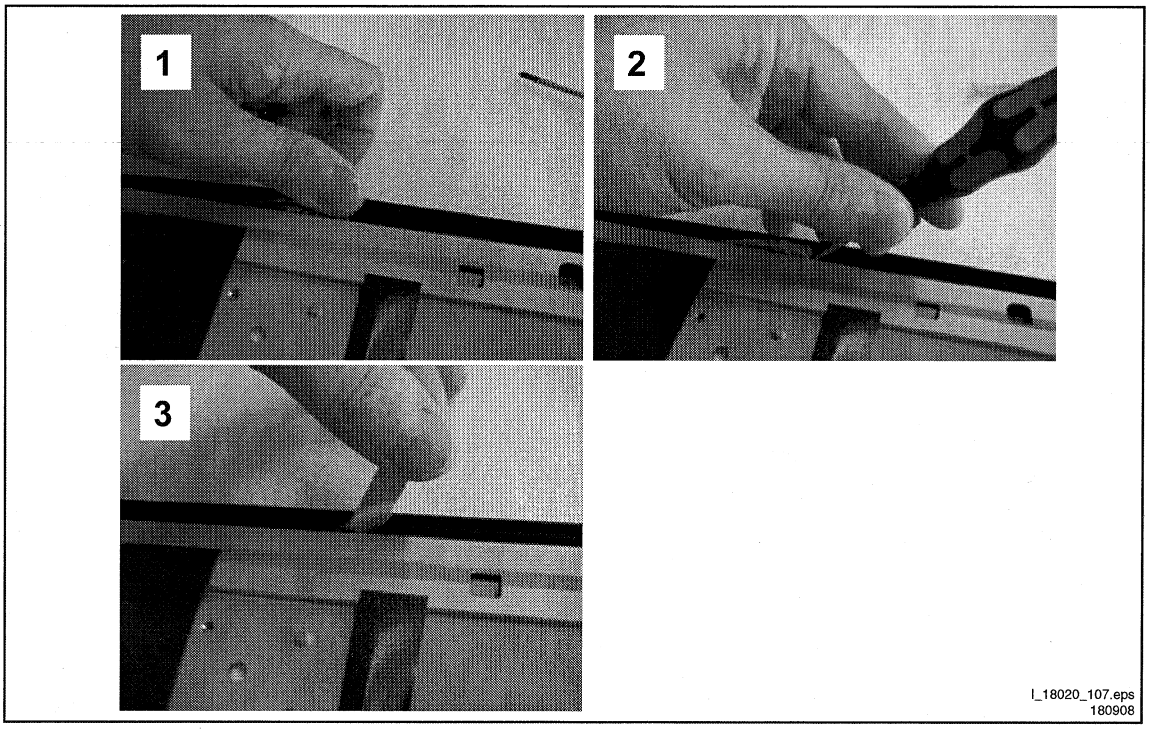
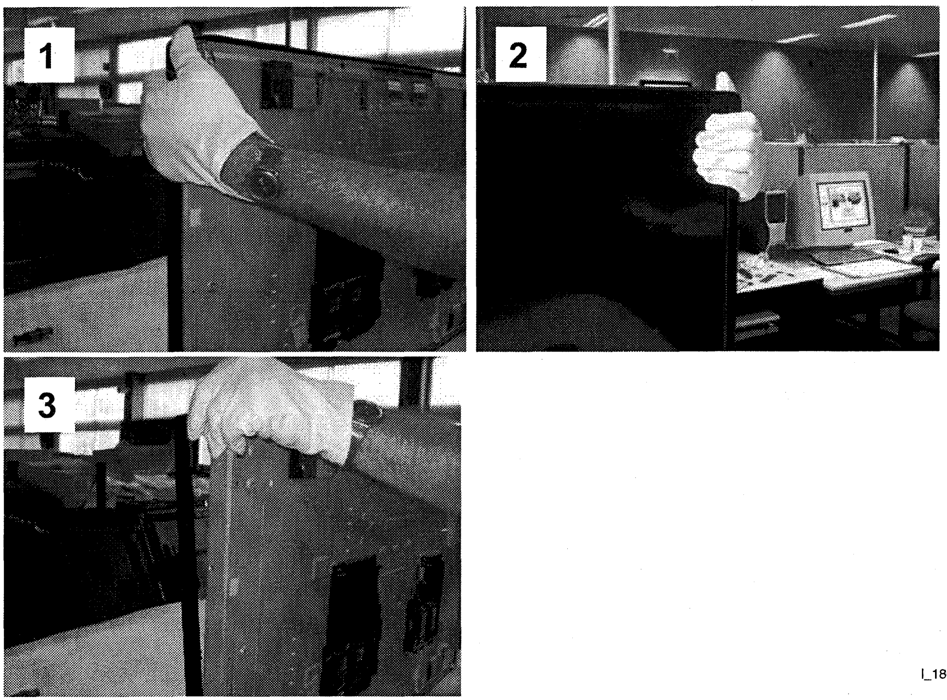

1
2
3
I_18020_107.eps
180908

Figure 4-21 LCD Panel -3-

D. Release two side walls of metal Front (use gloves).

1. Place thumb against each upper corner of the metal Front.
2. Place fingers against LCD Panel.
3. Push out LCD Panel in each corner until tape in middle of side wall releases.



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110908

Figure 4-22 LCD Panel -4-

E. Release bottom wall of metal Front (use gloves).

1. Place hands in top/middle of metal Front and LCD Panel.
2. Pull metal Front and LCD Panel further apart until 2 tapes in bottom wall release.
3. Take out LCD Panel.

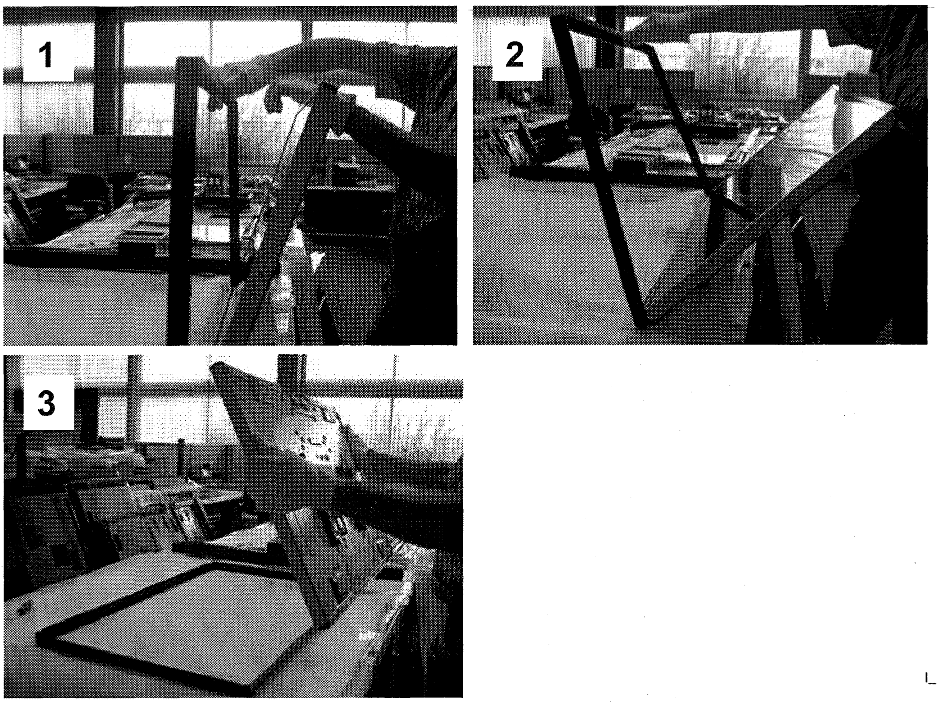

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Figure 4-23 LCD Panel -5-

F. Removing tapes/foams from LCD Panel (use “Label Off 50”; “Intronics L50/200”).

1. Remove remains of thermal foam on top of LCD Panel.
2. Remove remains of double-sided tapes (4x) on front of LCD Panel.
3. Remove protective foam on bottom of LCD Panel.

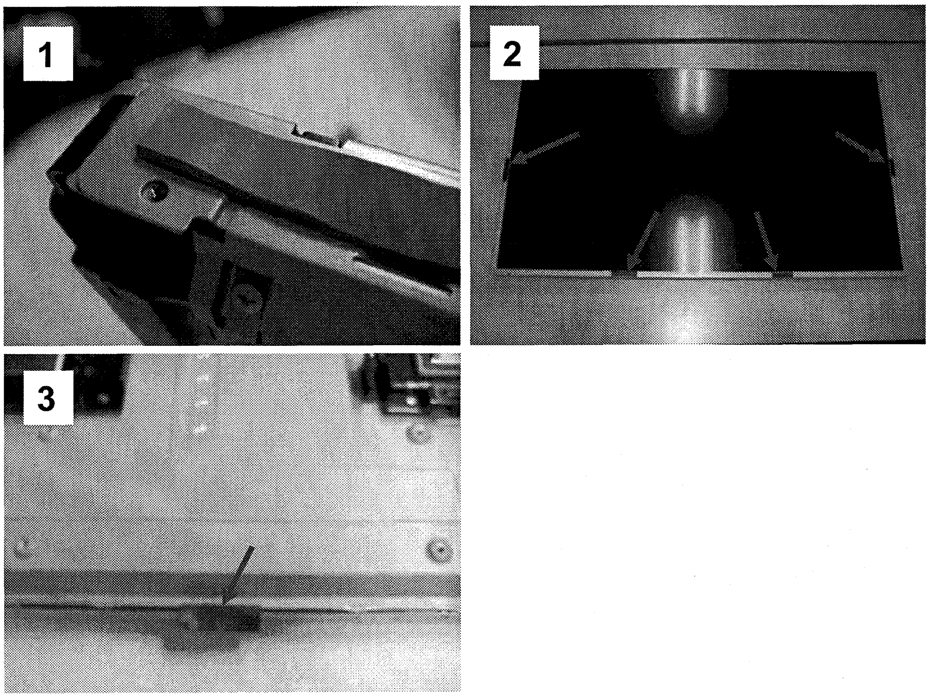

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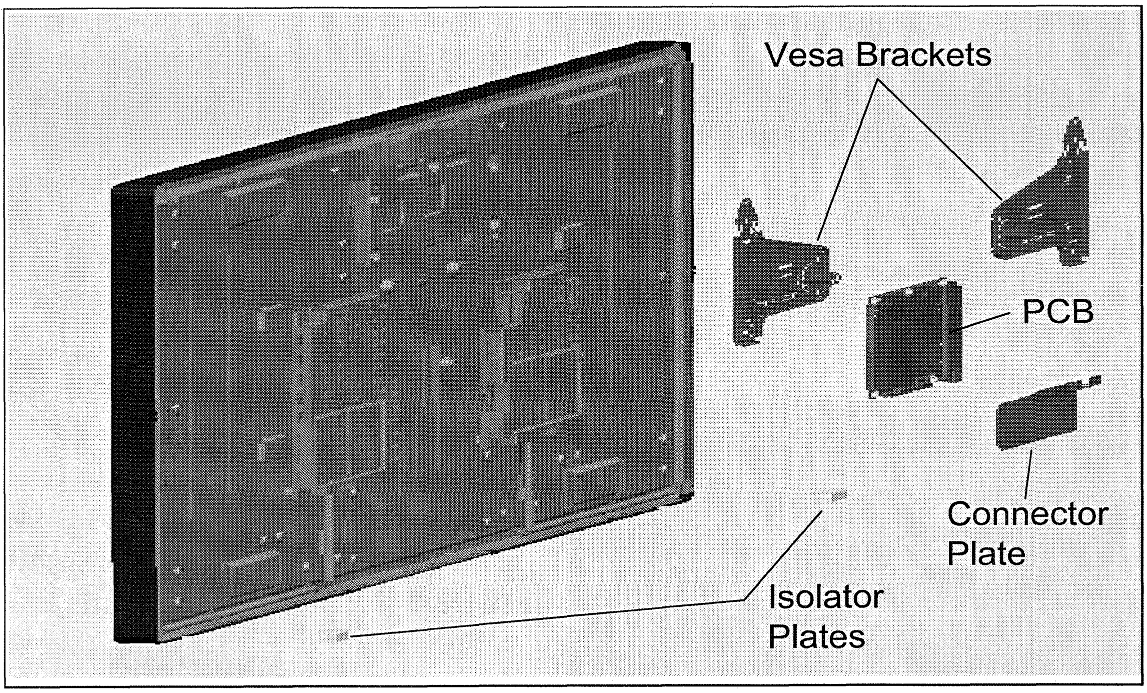
Figure 4-24 LCD Panel -6-

For re-assembly instructions, proceed with step K.

LCD Panel Replacement
Instructions G to J apply if you have to replace the LCD Panel.

G. Remove VESA brackets, PCB connector plate, wiring, and isolator plates.


Vesa Brackets
PCB
Connector Plate
Isolator Plates

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151008

Figure 4-25 LCD Panel -7-

H. Remove all remaining tapes/foams/cable clamps.
1. Remove remaining tapes for wiring.
2. Remove cable clamps (five times).
3. Remove all backlight blocking foams.
4. Remove all glue remains with “Label Off 50”.

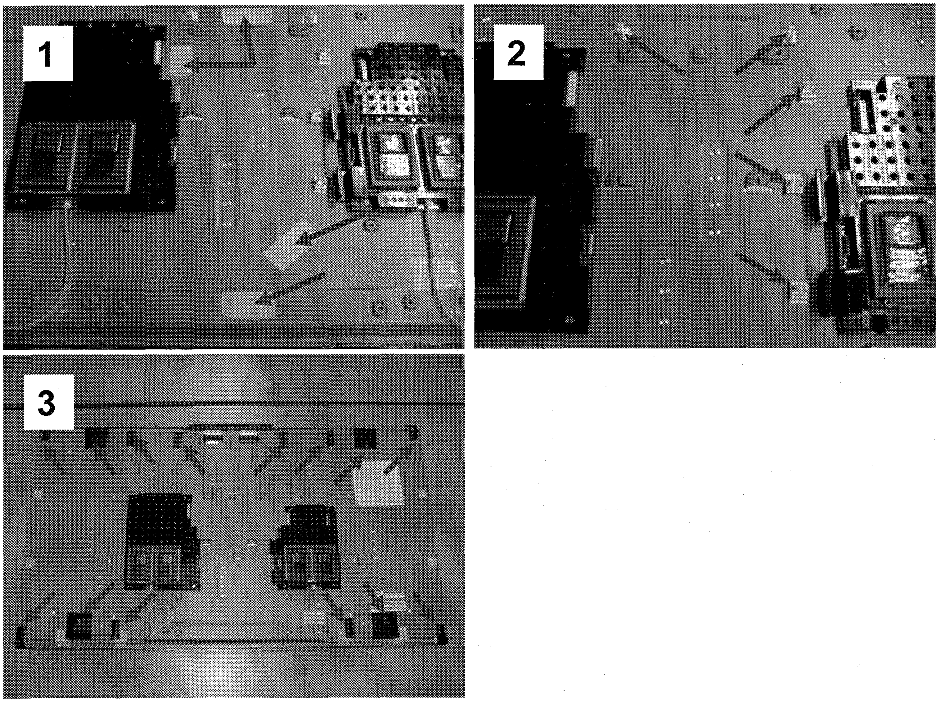

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Figure 4-26 LCD Panel -8-

I. Prepare new LCD Panel.

1. Take new LCD Panel and place two isolator plates.
2. Glue **new** foams on LCD Panel with the following specifications:
   - four times foam L × W × T = 20 × 43 × 0.5 mm [A].
   - six times foam L × W × T = 70 × 50 × 0.5 mm [B].
   - four times foam L × W × T = 30 × 43 × 0.5 mm [C].
3. Figure [3] show the upper- and lower foams.

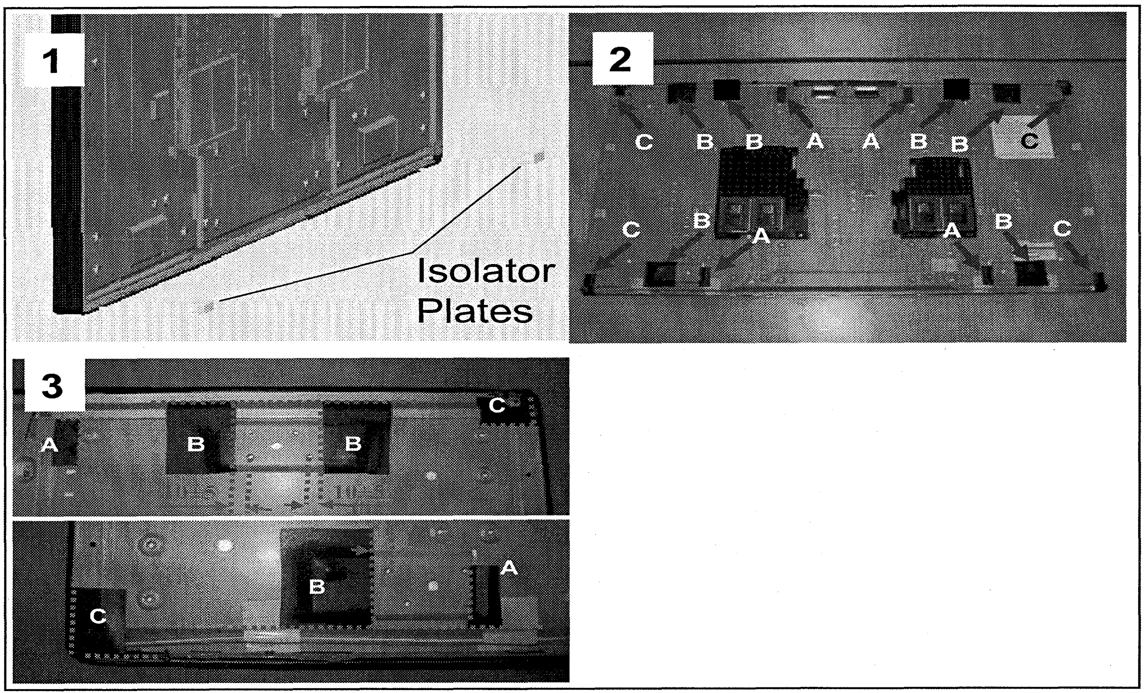
1
Isolator Plates
2
C
B
B
A
A
B
B
C
C
B
A
A
B
C
3
C
A
B
B
A
B
C

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Figure 4-27 LCD Panel -9-

J. Assemble VESA brackets, PCB, connector plate, and wiring.

1. Assemble VESA brackets, PCB and connector plate.
2. Assemble cable clamps:
   - five times cable clamp 11.2 mm.
3. Assemble wiring.

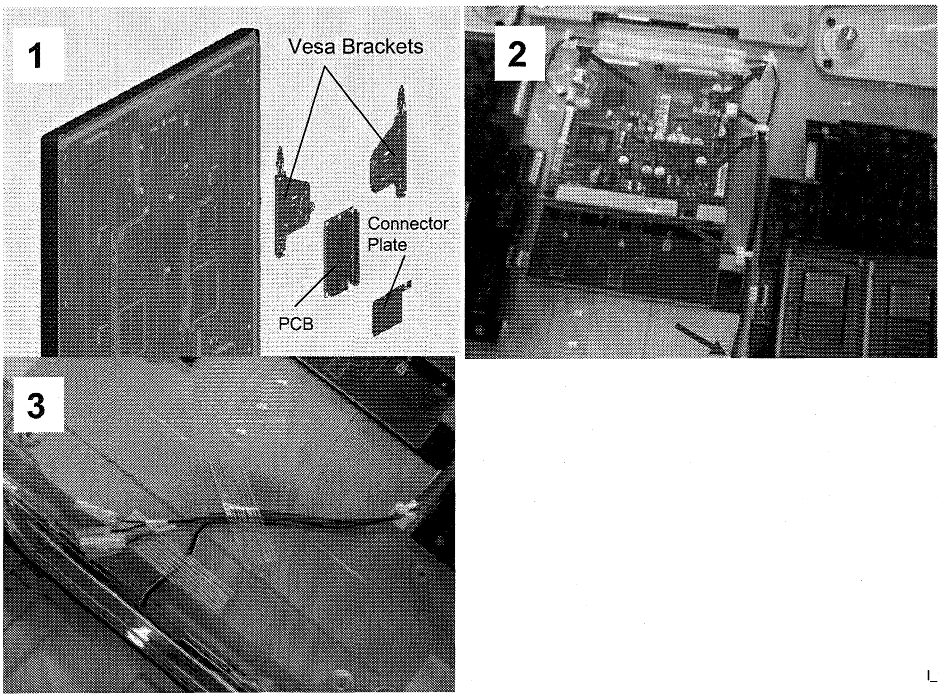
1
Vesa Brackets
Connector Plate
PCB
2
3

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Figure 4-28 LCD Panel -10-

K. Assemble metal Front and LCD Panel (use gloves).

1. Take a **new** metal Front and remove liners of double-sided tapes (four times).
2. Insert LCD Panel as shown in picture: first top side, then cantilever down.
3. Bend down metal lips in each corner (4 times).

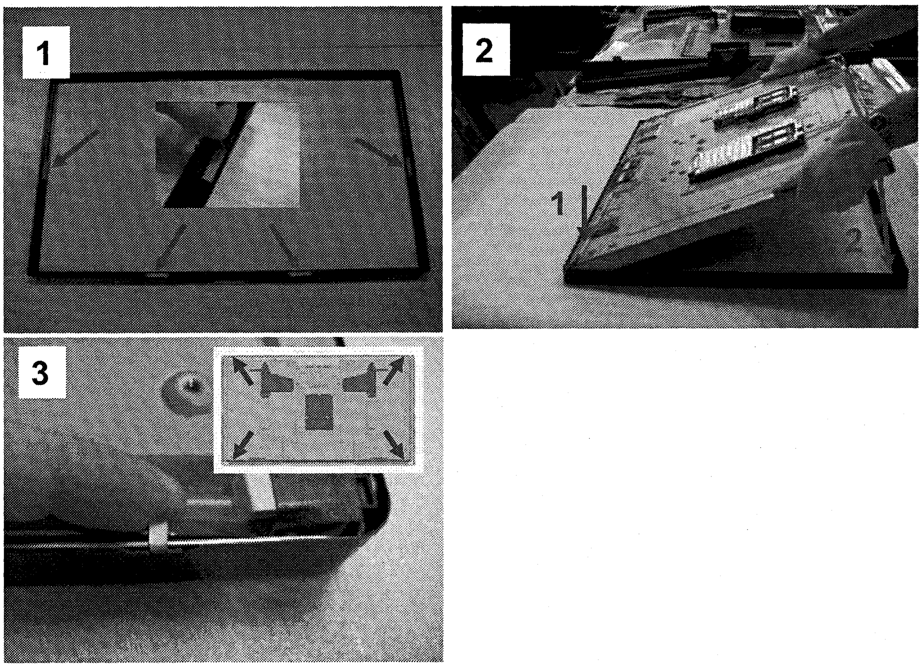

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Figure 4-29 LCD Panel -11-

L. Assemble Leading Edge.

1. Assemble Leading Edge on Front.
2. Glue protective foam across edge of metal Front and LCD Panel with the following specifications:
   1 time foam L × W × T = 55 × 20 × 0.8 mm [A].
3. Glue light-blocking foam upon LED-PCB with the following specifications:
   1 time foam L × W × T = 20 × 43 × 0.5 mm [B].

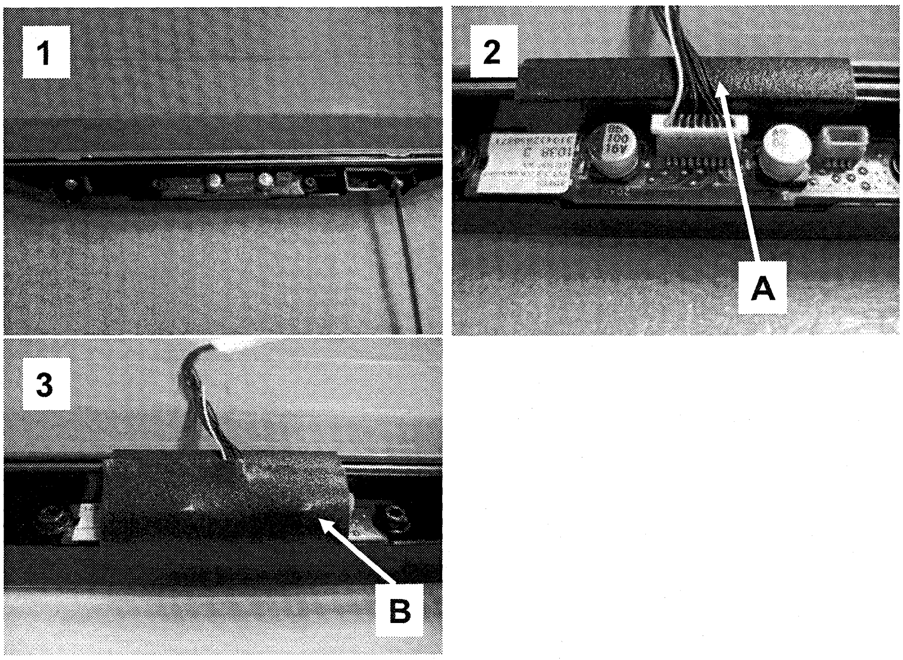

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Figure 4-30 LCD Panel -12-

M. Assemble Flare.

1. Place flare upon LCD Panel as shown in picture: first on top side.
2. Cantilever flare down while pulling it slightly open (to avoid scratches from metal Front).
3. Fix flare on Panel (six screws).

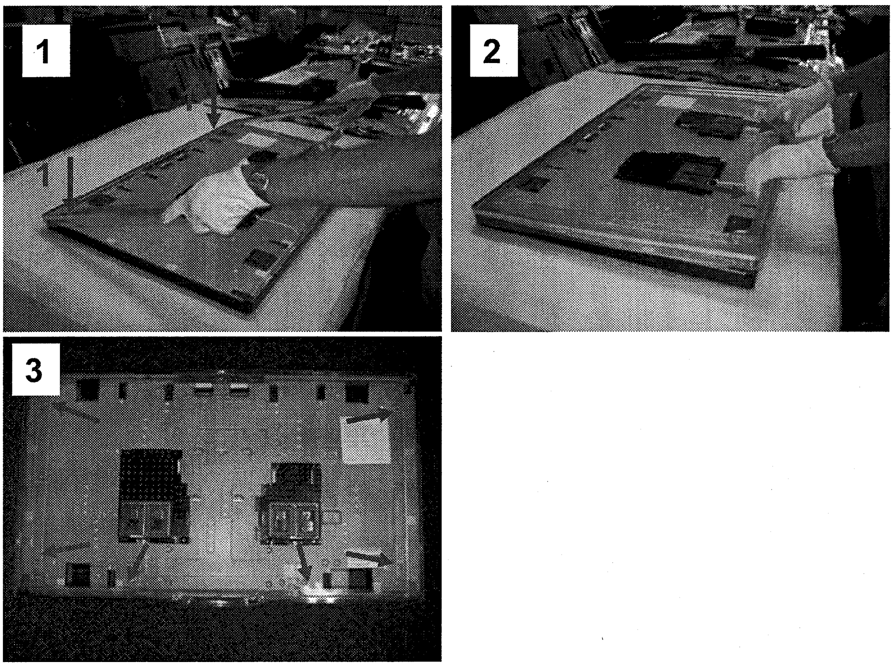

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Figure 4-31 LCD Panel -13-

N. Assemble Stand Bracket, Sound Interface, Back Cover, Soundbar and Stand.

1. Remove protective foils on both sides of Flare.

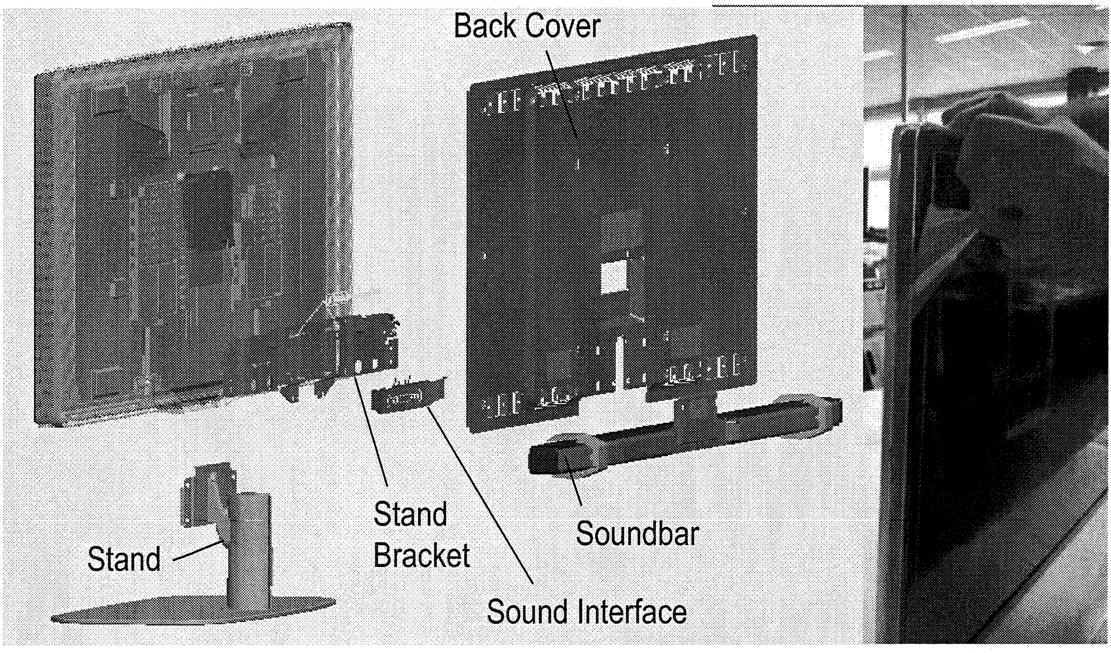
Back Cover
Stand
Stand Bracket
Soundbar
Sound Interface

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Figure 4-32 LCD Panel -14-

4.5 Set Re-assembly

To re-assemble the whole set, execute all processes in reverse order, except for the Monitor. To re-assembly the Monitor, follow the instructions in the applicable section of this Manual.

Notes:
- While re-assembling, make sure that all cables are placed and connected in their original position. See figure “Cable dressing”.
- Pay special attention not to damage the EMC foams on the SSB shields. Ensure that EMC foams are mounted correctly.

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

5.1 Test Points
5.2 Service Modes
5.3 Stepwise Start-up
5.4 Service Tools
5.5 Error Codes
5.6 The Blinking LED Procedure
5.7 Protections
5.8 Fault Finding and Repair Tips
5.9 Software Upgrading

5.1 Test Points

As most signals are digital, it will be difficult to measure waveforms with a standard oscilloscope. However, several key ICs are capable of generating test patterns, which can be controlled via ComPair. In this way it is possible to determine which part is defective.

Perform measurements under the following conditions:

- Service Default Mode.
- Video: Colour bar signal.
- Audio: 3 kHz left, 1 kHz right.

5.2 Service Modes

Service Default mode (SDM) and Service Alignment Mode (SAM) offers several features for the service technician, while the Customer Service Mode (CSM) is used for communication between the call centre and the customer.

This chassis also offers the option of using ComPair, a hardware interface between a computer and the TV chassis. It offers the abilities of structured troubleshooting, error code reading, and software version read-out for all chassis.
(see also section "5.4.1 ComPair").

5.2.1 Service Default Mode (SDM)

Purpose

- To create a pre-defined setting, to get the same measurement results as given in this manual.
- To override SW protections detected by stand-by processor and make the TV start up to the step just before protection (a sort of automatic stepwise start up). See section "5.3 Stepwise Start-up".
- To start the blinking LED procedure where only layer 2 errors are displayed. (see also section "5.5 Error Codes")

Specifications

Table 5-1 SDM default settings

Region	Freq. (MHz)	Default system
Europe, AP(PAL/Multi)	475.25	PAL B/G
Europe, AP DVB-T	546.00 PID Video: 0B 06 PID PCR: 0B 06 PID Audio: 0B 07	DVB-T

- All picture settings at 50% (brightness, colour, contrast).
- All sound settings at 50%, except volume at 25%.
- All service-unfriendly modes (if present) are disabled, like:
  - (Sleep) timer.
  - Child/parental lock.
  - Picture mute (blue mute or black mute).
  - Automatic volume levelling (AVL).
  - Skip/blank of non-favourite pre-sets.

How to Activate SDM

For this chassis there are two kinds of SDM: an **analog SDM** and a **digital SDM**. Tuning will happen according table "SDM Default Settings".

- **Analog SDM**: use the standard RC-transmitter and key in the code "062596", directly followed by the "MENU" button. **Note:** It is possible that, together with the SDM, the main menu will appear. To switch it "off", push the "MENU" button again.
- **Digital SDM**: use the standard RC-transmitter and key in the code "062593", directly followed by the "MENU" button. **Note:** It is possible that, together with the SDM, the main menu will appear. To switch it "off", push the "MENU" button again.
- **Analog SDM** can also be activated by connecting for a moment the solder pad (see figure "Service mode pads") on the SSB with the indication "SDM" [1], to GND.

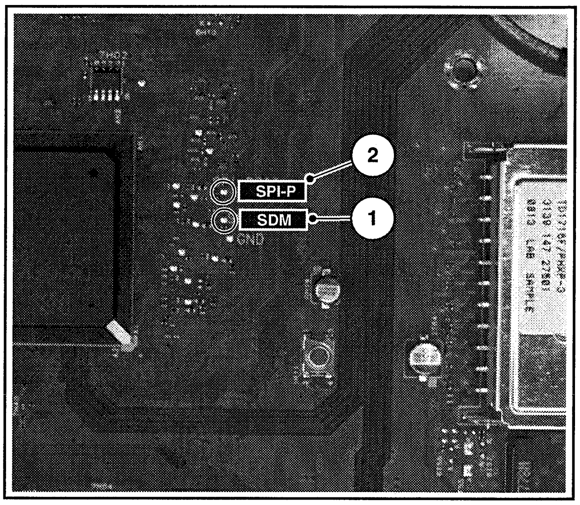

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Figure 5-1 Service mode pads

After activating this mode, "SDM" will appear in the upper right corner of the screen (when a picture is available).

How to Navigate

When the "MENU" button is pressed on the RC transmitter, the set will toggle between the SDM and the normal user menu (with the SDM mode still active in the background).

How to Exit SDM

Use one of the following methods:

- Switch the set to STAND-BY via the RC-transmitter.
- Via a standard customer RC-transmitter: key in "00"-sequence.

5.2.2 Service Alignment Mode (SAM)

Purpose

- To perform (software) alignments.
- To change option settings.
- To easily identify the used software version.
- To view operation hours.
- To display (or clear) the error code buffer.

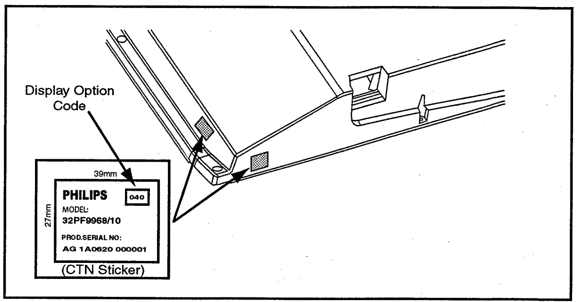
How to Activate SAM

Via a standard RC transmitter: key in the code "062596" directly followed by the "INFO" button. After activating SAM with this method a service warning will appear on the screen, continue by pressing the red button on the RC.

Contents of SAM:

- **Hardware Info.**
  - **A. SW Version.** Displays the software version of the main software (**example:** Q591E-1.2.3.4 = AAAAB_X.Y.W.Z).
    - **AAAA**= the chassis name.
    - **B**= the region: A= AP, E= EU, L= Latam, U = US. For AP sets it is possible that the Europe software version is used.
    - **X.Y.W.Z**= the software version, where X is the main version number (different numbers are not compatible with one another) and Y.W.Z is the sub version number (a higher number is always compatible with a lower number).
  - **B. SBY PROC Version.** Displays the software version of the stand-by processor.
  - **C. Production Code**. Displays the production code of the TV, this is the serial number as printed on the back of the TV set. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- **Operation Hours.** Displays the accumulated total of operation hours (not the stand-by hours). Every time the TV is switched "on/off", 0.5 hours is added to this number.
- **Errors** (followed by maximum 10 errors). The most recent error is displayed at the upper left (for an error explanation see section "5.5 Error Codes").
- **Reset Error Buffer.** When "cursor right" (or the "OK button) is pressed followed by another "OK" button touch, the error buffer is reset.
- **Alignments.** This will activate the "ALIGNMENTS" sub-menu.
- **Dealer Options.** Extra features for the dealers.
- **Options.** Extra features for Service. For more info regarding option codes, see chapter 8 "Alignments". Note that if the option code numbers are changed, these have to be confirmed with pressing the "OK" button before the options are stored. Otherwise changes will be lost.
- **Initialize NVM.** The moment the processor recognizes a corrupted NVM, the "initialize NVM" line will be highlighted. Now, two things can be done (dependent of the service instructions at that moment):
  - Save the content of the NVM via ComPair for development analysis, **before** initializing. This will give the Service department an extra possibility for diagnosis (e.g. when Development asks for this).
  - Initialize the NVM.

Note: When the NVM is corrupted, or replaced, there is a high possibility that no picture appears because the display code is not correct. So, before initializing the NVM via the SAM, a picture is necessary and therefore the correct display option has to be entered. Refer to chapter 8 "Alignments" for details. To adapt this option, it's advised to use ComPair (the correct HEX values for the options can be found in chapter 8 "Alignments") or a method via a standard RC (described below).
Changing the display option via a standard RC: Key in the code "062598" directly followed by the "MENU" button and "XXX" (where XXX is the 3 digit decimal display code as mentioned in table "Option code overview" in chapter 8 "Alignments". Remark : there is only one display option code here "168" used for this chassis). If the above action is successful, the front LED will go out as an indication that the RC sequence was correct. After the display option is changed in the NVM, the TV will go to the Stand-by mode. If the NVM was corrupted or empty before this action, it will be initialized first (loaded with default values). This initializing can take up to 20 seconds.



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240108

Figure 5-2 Location of Display Option Code sticker

- **Store - go right.** All options and alignments are stored when pressing "cursor right" (or the "OK" button) and then the "OK"-button.
- **SW Maintenance.**
  - **SW Events.** Not useful for Service purposes. In case of specific software problems, the development department can ask for this info.
  - **HW Events.** Not useful for Service purposes. In case of specific software problems, the development department can ask for this info.
- **Test settings.** For development purposes only.
- **Upload to USB.** To upload several settings from the TV to an USB stick, which is connected to the SSB. The items are "Channel list", "Personal settings", "Option codes", "Display-related alignments" and "History list". First a directory "repair\" has to be created in the root of the USB stick. To upload the settings select each item separately, press "cursor right" (or the "OK" button), confirm with "OK" and wait until "Done" appears. In case the download to the USB stick was not successful "Failure" will appear. In this case, check if the USB stick is connected properly and if the directory "repair" is present in the root of the USB stick. Now the settings are stored onto the USB stick and can be used to download onto another TV or other SSB. Uploading is of course only possible if the software is running and if a picture is available. This method is created to be able to save the customer's TV settings and to store them into another SSB.
- **Download to USB.** To download several settings from the USB stick to the TV. Same way of working as with uploading. To make sure that the download of the channel list from USB to the TV is executed properly, it is necessary to restart the TV and tune to a valid preset if necessary. **Note**: The "History list item" can not be downloaded from USB to the TV. This is a "read-only" item. In case of specific problems, the development department can ask for this info.
- **Development file versions.** Not useful for Service purposes, this information is only used by the development department.

How to Navigate

- In SAM, the menu items can be selected with the "CURSOR UP/DOWN" key (or the scroll wheel) on the RC-transmitter. The selected item will be highlighted. When not all menu items fit on the screen, move the "CURSOR UP/ DOWN" key to display the next/previous menu items.
- With the "CURSOR LEFT/RIGHT" keys (or the scroll wheel), it is possible to:
  - (De) activate the selected menu item.
  - (De) activate the selected sub menu.
- With the "OK" key, it is possible to activate the selected action.

How to Exit SAM

Use one of the following methods:

- Press the "MENU" button on the RC-transmitter.

- Switch the set to STAND-BY via the RC-transmitter.

5.2.3 Customer Service Mode (CSM)

Purpose

When a customer is having problems with his TV-set, he can call his dealer or the Customer Helpdesk. The service technician can then ask the customer to activate the CSM, in order to identify the status of the set. Now, the service technician can judge the severity of the complaint. In many cases, he can advise the customer how to solve the problem, or he can decide if it is necessary to visit the customer.
The CSM is a read only mode; therefore, modifications in this mode are not possible.
When in this chassis CSM is activated, a test pattern will be displayed during 5 seconds (1 second Blue, 1 second Green and 1 second Red, then again 1 second Blue and 1 second Green). This test pattern is generated by the PNX5100. So if this test pattern is shown, it could be determined that the back end video chain (PNX5100, LVDS, and display) of the SSB is working.
New in this chassis are two test patterns with fixed colours:

- **When the Green key is pushed while in CSM (toggle function)** : a fixed testpattern by the “FPGA transmitter” device located on the LVDS panel will be generated. The selftest of this device is confirmed positive with a fully Green picture displayed on the screen.
- **When the Yellow key is pushed while in CSM (toggle function)** : a fixed testpattern by the “FPGA receiver” device located on the monitor will be generated. The selftest of this device is confirmed positive with a fully Yellow picture displayed on the screen.

When CSM is activated and there is a USB stick connected to the TV, the software will dump the complete CSM content to the USB stick. The file (CSM.txt) will be saved in the root of the USB stick. This info can be handy if no information is displayed.

Also when CSM is activated, the layer 1 error is displayed via blinking LED on the HUB. Only the latest error is displayed. (see also section “5.5 Error Codes”).

How to Activate CSM

Key in the code “123654” via the standard RC transmitter.

Note: Activation of the CSM is only possible if there is no (user) menu on the screen!

How to Navigate

By means of the “CURSOR-DOWN/UP” knob (or the scroll wheel) on the RC-transmitter, can be navigated through the menus.

Contents of CSM

The contents are reduced to 4 pages: General, Software versions/General, Quality items and Addtitional Info. The group names itself are not shown anywhere in the CSM menu.

General

- **Set Type.** This information is very helpful for a helpdesk/ workshop as reference for further diagnosis. In this way, it is not necessary for the customer to look at the rear of the TV-set. Note that if an NVM is replaced or is initialized after corruption, this set type has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- **Production Code.** Displays the production code (the serial number) of the TV. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee a in possibility to do this.
- **Installed date.** Indicates the date of the first installation of the TV. This date is acquired via time extraction.
- **Options 1.** Gives the option codes of option group 1 as set in SAM (Service Alignment Mode).
- **Options 2.** Gives the option codes of option group 2 as set in SAM (Service Alignment Mode).
- **12NC SSB.** Gives an identification of the SSB as stored in NVM. Note that if an NVM is replaced or is initialized after corruption, this identification number has to be re-written to NVM. ComPair will foresee in a possibility to do this. This identification number is the 12nc number of the SSB.
  Remark: the content here can also be a part of the 12NC SSB in combination with the serial number.
- **12NC display.** Shows the 12NC of the display
- **12NC supply.** Shows the 12NC of the supply.
- **12NC “bolt-on”.** Shows the 12NC of the “BOLT-ON”-module.
- **12NC LED dimming panel.** Shows the 12NC of the LED dimming panel.

Software versions/General

- **Current main SW.** Displays the built-in main software version. In case of field problems related to software, software can be upgraded. As this software is consumer upgradeable, it will also be published on the Internet. Example: Q591E_1.2.3.4
- **Standby SW.** Displays the built-in stand-by processor software version. Upgrading this software will be possible via ComPair or via USB (see chapter Software upgrade). Example: STDBY_3.0.1.2.
- **MOP ambient light SW.** Displays the MOP ambient light EPLD SW.
- **MPEG4 software.** Displays the MPEG4 software (optional for sets with MPEG4).
- **PNX5100 boot NVM.** Displays the SW-version that is used in the PNX5100 boot NVM.
- **LED dimming SW.** Displays the SW-version for the LED dimming panel.
- **MPEG4 (blue to toggle).** Displays the activation of MPEG4 reception functionality (on/off).

Quality items

- **Signal quality.** Bad / average /good
- **Child lock.** Not active / active. This is a combined item for locks. If any lock (Preset lock, child lock, lock after or parental lock) is active, the item shall show “active”.
- **Table channel changed.** This item is for development purpose.
- **Key missing.** This is a combined item for keys. The keys have a separate bit and the sum is displayed in decimal value.
  - HDMI key valid = 001
  - MAC key valid = 010
    Important remark here : due to a software bug, the MAC key is missing and not valid when “2” is displayed in CSM.So, if for instance the HDMI and MAC keys are both valid, the decimal value in CSM “1” is displayed and not “3”.
  - BDS key valid = 100
    If 3 keys are valid the value: “5” is displayed (should be “7” but due to the software bug it is not).
    For value:
    “0” in CSM: MAC stored, HDCP invalid.
    “1” in CSM: MAC stored, HDCP valid.
    “2” in CSM: no MAC, HDCP invalid.
    “3” in CSM: no MAC, HDCP valid.
- **CI slot present.** If the common interface module is detected the result will be “YES”, else “NO”.
- **HDMI input format.** The detected input format of the HDMI.
- **HDMI audio input stream.** The HDMI audio input stream is displayed: present / not present.
- **HDMI video input stream.** The HDMI video input stream is displayed: present / not present.

Additional Info

- **12NC LVDS2DP board.** Displays the 12NC of the built-in LVDS-to-DisplayPort software.
- **12NC monitor board.** Displays the 12NC of the monitor board.
- **SW version DPTX.** Displays the built-in DisplayPort TX software version.
- **SW version DPRX.** Displays the built-in DisplayPort RX software version.
- **SW version FPGA e-box.** Displays the built-in FPGA e-box (HUB) software version.
- **SW version FPGA monitor.** Displays the built-in FPGA monitor software version.
- **SW version microP monitor.** Displays the built-in monitor microprocessor software version.
- **SW version NVM monitor.** Displays the built-in monitor NVM software version.

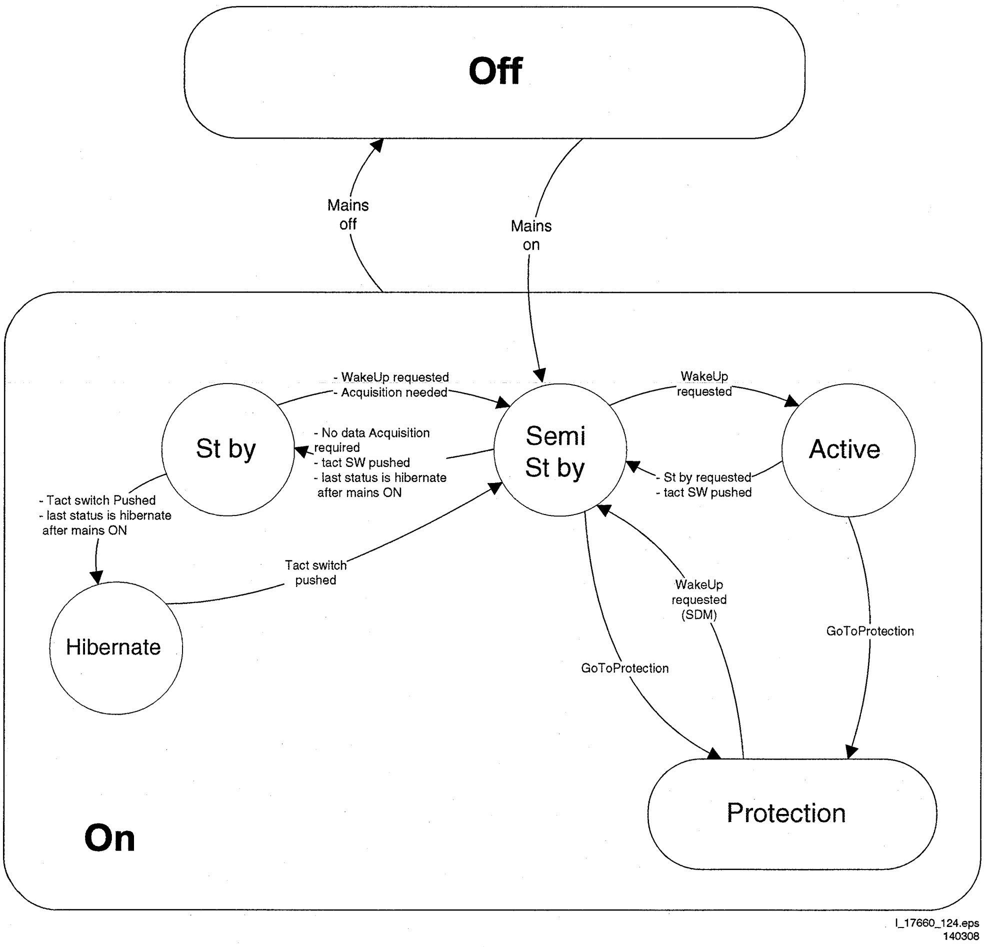
How to Exit CSM
Press “MENU” on the RC-transmitter.

5.3 Stepwise Start-up

When the TV is in a protection state due to an error detected by stand-by software (error blinking is displayed) **and** SDM is activated via shortcutting the pins on the SSB, the TV starts up until it reaches the situation just before protection. So, this is a kind of automatic stepwise start-up. In combination with the start-up diagrams below, you can see which supplies are present at a certain moment. Important to know is, that if e.g. the 3V3 detection fails and thus error layer 2 = 18 is blinking while the TV is restarted via SDM, the Stand-by Processor will enable the 3V3, but the TV set will not go to protection now. The TV will stay in this situation until it is reset (Mains/AC Power supply interrupted). **Caution:** in case the start up in this mode with a faulty FET 7U08 is done, you can destroy all IC’s supplied by the +3V3, due to overvoltage (12V on 3V3-line). It is recommended to measure first the FET 7U08 or other FET’s on shortcircuit before activating SDM via the service pads.

The abbreviations “SP” and “MP” in the figures stand for:

- SP: protection or error detected by the **S**tand-by **P**rocessor.
- MP: protection or error detected by the MIPS **M**ain **P**rocessor.


Off
Mains off
Mains on
- WakeUp requested
- Acquisition needed
St by
- No data Acquisition required
- tact SW pushed
- last status is hibernate after mains ON
Semi St by
WakeUp requested
Active
- St by requested
- tact SW pushed
- Tact switch Pushed
- last status is hibernate after mains ON
Tact switch pushed
Hibernate
WakeUp requested (SDM)
GoToProtection
GoToProtection
Protection
On
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140308

Figure 5-3 Transition diagram

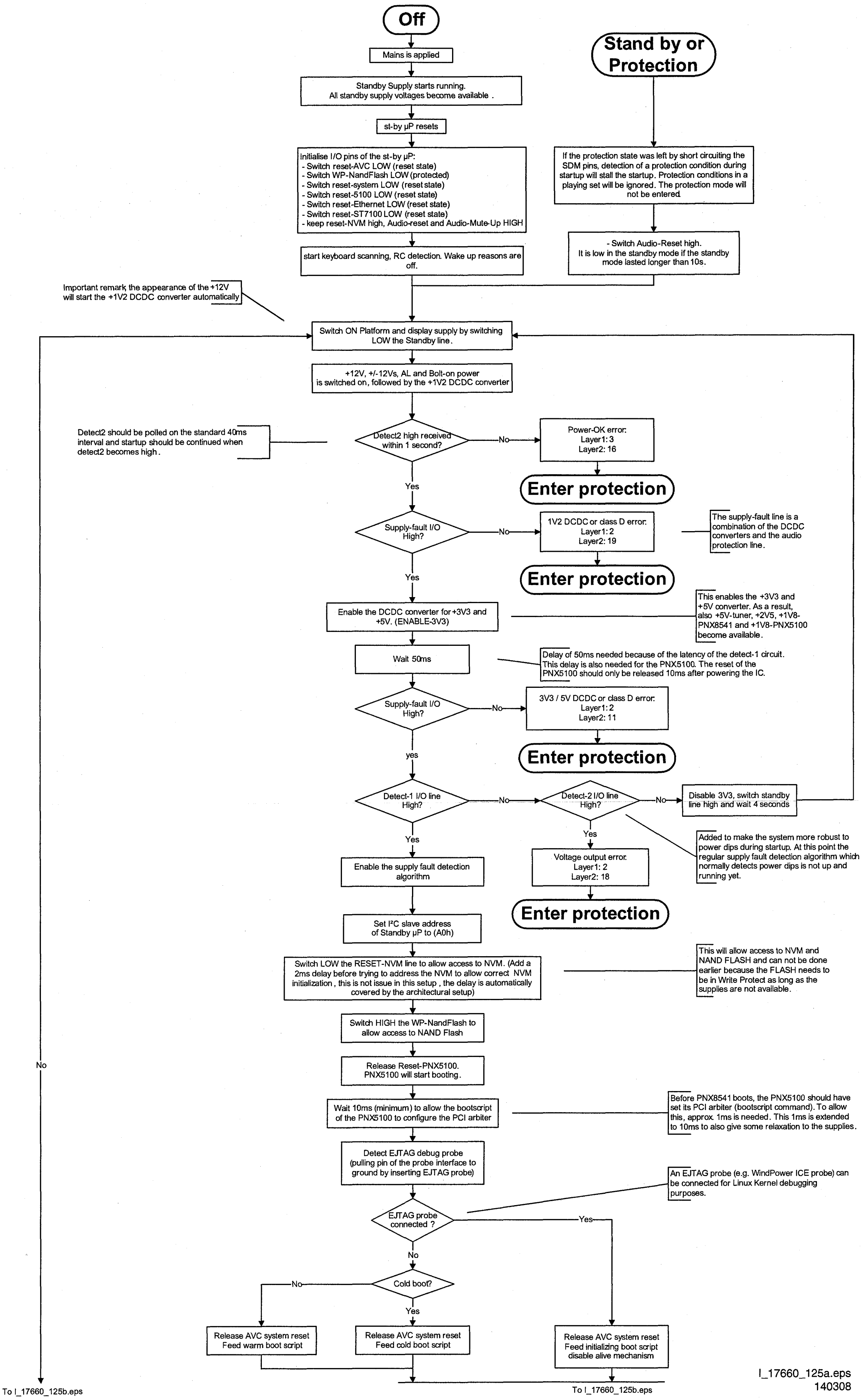
Off
Mains is applied
Standby Supply starts running. All standby supply voltages become available .
st-by µP resets
Initialise I/O pins of the st-by µP:
- Switch reset-AVC LOW (reset state)
- Switch WP-NandFlash LOW (protected)
- Switch reset-system LOW (reset state)
- Switch reset-5100 LOW (reset state)
- Switch reset-Ethernet LOW (reset state)
- Switch reset-ST7100 LOW (reset state)
- keep reset-NVM high, Audio-reset and Audio-Mute-Up HIGH
start keyboard scanning, RC detection. Wake up reasons are off.
Stand by or Protection
If the protection state was left by short circuiting the SDM pins, detection of a protection condition during startup will stall the startup. Protection conditions in a playing set will be ignored. The protection mode will not be entered.
- Switch Audio-Reset high. It is low in the standby mode if the standby mode lasted longer than 10s.
Important remark: the appearance of the +12V will start the +1V2 DCDC converter automatically
Switch ON Platform and display supply by switching LOW the Standby line.
+12V, +/-12Vs, AL and Bolt-on power is switched on, followed by the +1V2 DCDC converter
Detect2 should be polled on the standard 40ms interval and startup should be continued when detect2 becomes high.
Detect2 high received within 1 second?
No
Power-OK error: Layer1: 3 Layer2: 16
Enter protection
Yes
Supply-fault I/O High?
No
1V2 DCDC or class D error: Layer1: 2 Layer2: 19
The supply-fault line is a combination of the DCDC converters and the audio protection line.
Enter protection
Yes
Enable the DCDC converter for +3V3 and +5V. (ENABLE-3V3)
This enables the +3V3 and +5V converter. As a result, also +5V-tuner, +2V5, +1V8-PNX8541 and +1V8-PNX5100 become available.
Wait 50ms
Delay of 50ms needed because of the latency of the detect-1 circuit. This delay is also needed for the PNX5100. The reset of the PNX5100 should only be released 10ms after powering the IC.
Supply-fault I/O High?
No
3V3 / 5V DCDC or class D error: Layer1: 2 Layer2: 11
Enter protection
yes
Detect-1 I/O line High?
No
Detect-2 I/O line High?
No
Disable 3V3, switch standby line high and wait 4 seconds
Yes
Voltage output error: Layer1: 2 Layer2: 18
Enter protection
Added to make the system more robust to power dips during startup. At this point the regular supply fault detection algorithm which normally detects power dips is not up and running yet.
Yes
Enable the supply fault detection algorithm
Set I²C slave address of Standby µP to (A0h)
Switch LOW the RESET-NVM line to allow access to NVM. (Add a 2ms delay before trying to address the NVM to allow correct NVM initialization, this is not issue in this setup, the delay is automatically covered by the architectural setup)
This will allow access to NVM and NAND FLASH and can not be done earlier because the FLASH needs to be in Write Protect as long as the supplies are not available.
Switch HIGH the WP-NandFlash to allow access to NAND Flash
Release Reset-PNX5100. PNX5100 will start booting.
Wait 10ms (minimum) to allow the bootscript of the PNX5100 to configure the PCI arbiter
Before PNX8541 boots, the PNX5100 should have set its PCI arbiter (bootscript command). To allow this, approx. 1ms is needed. This 1ms is extended to 10ms to also give some relaxation to the supplies.
Detect EJTAG debug probe (pulling pin of the probe interface to ground by inserting EJTAG probe)
An EJTAG probe (e.g. WindPower ICE probe) can be connected for Linux Kernel debugging purposes.
EJTAG probe connected ?
Yes
No
Cold boot?
No
Yes
Release AVC system reset Feed warm boot script
Release AVC system reset Feed cold boot script
Release AVC system reset Feed initializing boot script disable alive mechanism
No
To I_17660_125b.eps
To I_17660_125b.eps
I_17660_125a.eps
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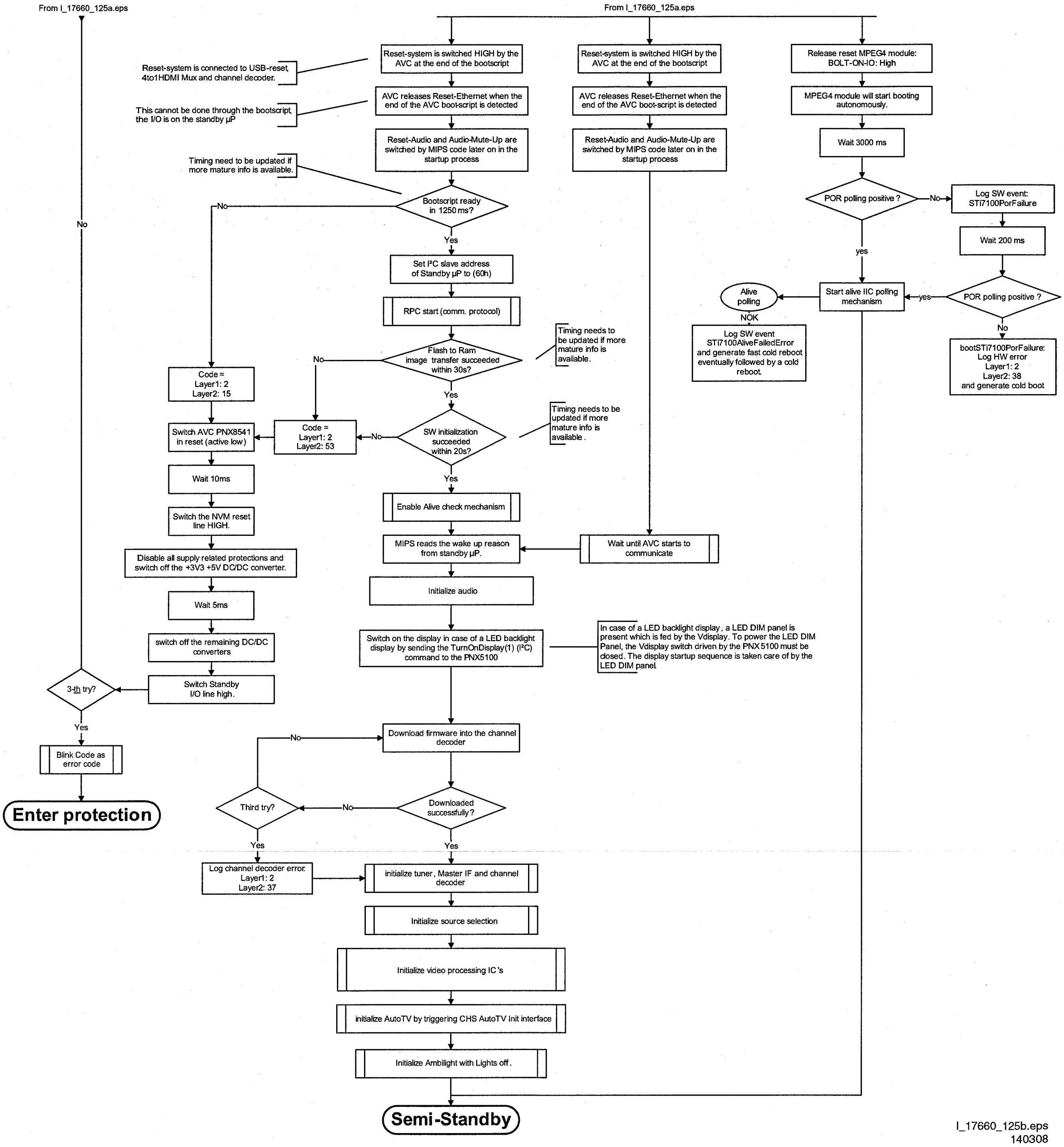
Figure 5-4 “Off” to “Semi Stand-by” flowchart (part 1)


From I_17660_125a.eps
From I_17660_125a.eps
Reset-system is connected to USB-reset, 4to1HDMI Mux and channel decoder.
This cannot be done through the bootscript, the I/O is on the standby µP
Timing need to be updated if more mature info is available.
Reset-system is switched HIGH by the AVC at the end of the bootscript
AVC releases Reset-Ethernet when the end of the AVC boot-script is detected
Reset-Audio and Audio-Mute-Up are switched by MIPS code later on in the startup process
Bootscript ready in 1250ms?
No
Yes
Set I²C slave address of Standby µP to (60h)
RPC start (comm. protocol)
Timing needs to be updated if more mature info is available.
Flash to Ram image transfer succeeded within 30s?
No
Yes
Code = Layer1: 2 Layer2: 15
Code = Layer1: 2 Layer2: 53
SW initialization succeeded within 20s?
No
Timing needs to be updated if more mature info is available.
Yes
Switch AVC PNX8541 in reset (active low)
Wait 10ms
Switch the NVM reset line HIGH.
Disable all supply related protections and switch off the +3V3 +5V DC/DC converter.
Wait 5ms
switch off the remaining DC/DC converters
Switch Standby I/O line high.
3-th try?
No
Yes
Blink Code as error code
Enter protection
Enable Alive check mechanism
MIPS reads the wake up reason from standby µP.
Initialize audio
Switch on the display in case of a LED backlight display by sending the TurnOnDisplay(1) (I²C) command to the PNX5100
In case of a LED backlight display, a LED DIM panel is present which is fed by the Vdisplay. To power the LED DIM Panel, the Vdisplay switch driven by the PNX5100 must be closed. The display startup sequence is taken care of by the LED DIM panel.
Reset-system is switched HIGH by the AVC at the end of the bootscript
AVC releases Reset-Ethernet when the end of the AVC boot-script is detected
Reset-Audio and Audio-Mute-Up are switched by MIPS code later on in the startup process
Wait until AVC starts to communicate
Release reset MPEG4 module: BOLT-ON-IO: High
MPEG4 module will start booting autonomously.
Wait 3000 ms
POR polling positive ?
No
Log SW event: STi7100PorFailure
Wait 200 ms
yes
Start alive IIC polling mechanism
yes
POR polling positive ?
No
bootSTi7100PorFailure: Log HW error Layer1: 2 Layer2: 38 and generate cold boot
Alive polling
NOK
Log SW event STi7100AliveFailedError and generate fast cold reboot eventually followed by a cold reboot
Download firmware into the channel decoder
No
Downloaded successfully?
No
Third try?
Yes
Yes
Log channel decoder error. Layer1: 2 Layer2: 37
initialize tuner, Master IF and channel decoder
Initialize source selection
Initialize video processing IC's
initialize AutoTV by triggering CHS AutoTV Init interface
Initialize Ambilight with Lights off.
Semi-Standby

I_17660_125b.eps
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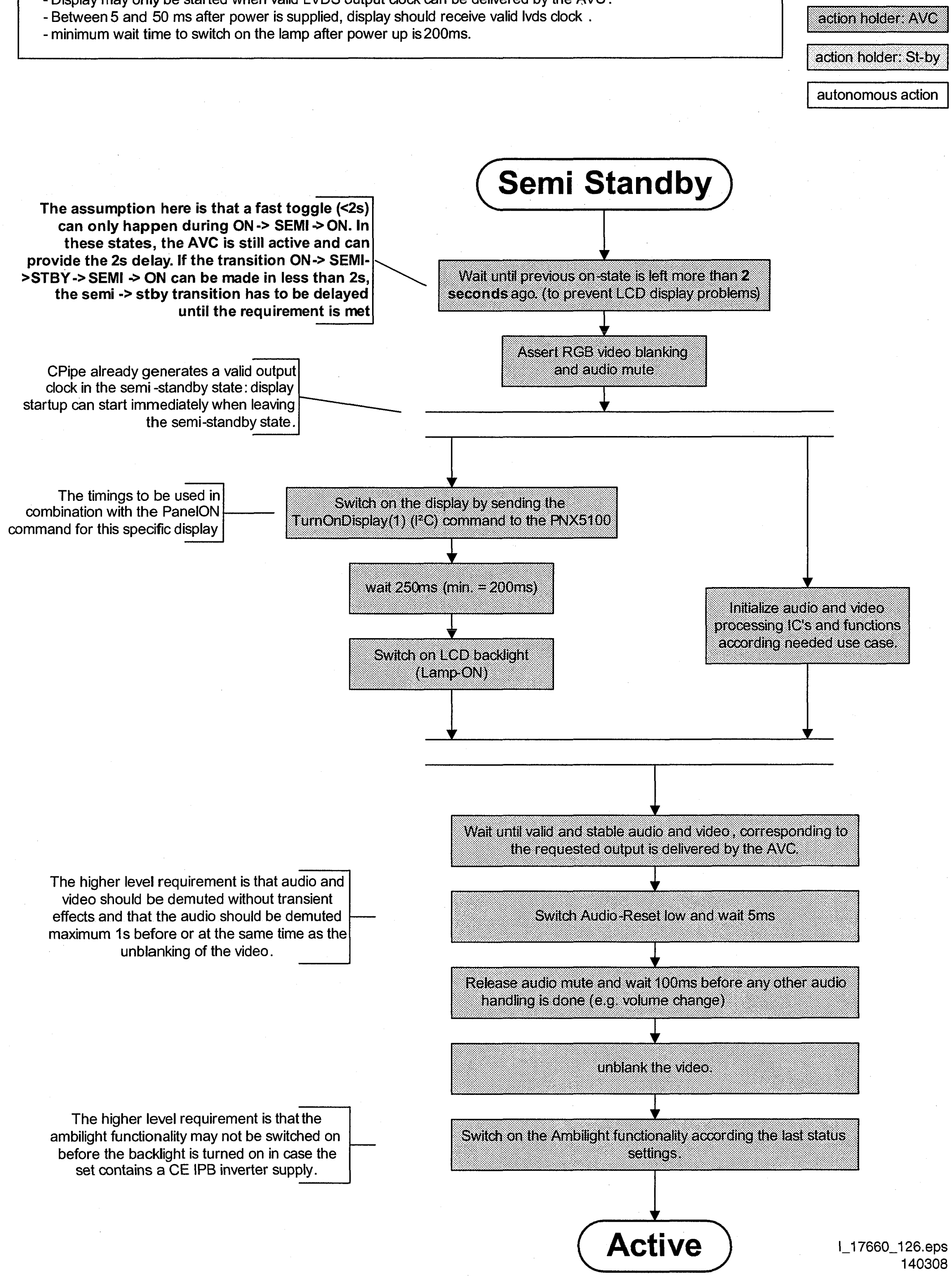
Figure 5-5 “Off” to “Semi Stand-by” flowchart (part 2)

Constraints taken into account:
- Display may only be started when valid LVDS output clock can be delivered by the AVC.
- Between 5 and 50 ms after power is supplied, display should receive valid lvds clock .
- minimum wait time to switch on the lamp after power up is 200ms.


action holder: AVC
action holder: St-by
autonomous action
Semi Standby
Wait until previous on-state is left more than 2 seconds ago. (to prevent LCD display problems)
Assert RGB video blanking and audio mute
Switch on the display by sending the TurnOnDisplay(1) (I²C) command to the PNX5100
wait 250ms (min. = 200ms)
Switch on LCD backlight (Lamp-ON)
Initialize audio and video processing IC's and functions according needed use case.
Wait until valid and stable audio and video, corresponding to the requested output is delivered by the AVC.
Switch Audio-Reset low and wait 5ms
Release audio mute and wait 100ms before any other audio handling is done (e.g. volume change)
unblank the video.
Switch on the Ambilight functionality according the last status settings.
Active

The assumption here is that a fast toggle (<2s) can only happen during ON -> SEMI -> ON. In these states, the AVC is still active and can provide the 2s delay. If the transition ON-> SEMI->STBY -> SEMI -> ON can be made in less than 2s, the semi -> stby transition has to be delayed until the requirement is met

CPipe already generates a valid output clock in the semi-standby state: display startup can start immediately when leaving the semi-standby state.

The timings to be used in combination with the PanelON command for this specific display

The higher level requirement is that audio and video should be demuted without transient effects and that the audio should be demuted maximum 1s before or at the same time as the unblanking of the video.

The higher level requirement is that the ambilight functionality may not be switched on before the backlight is turned on in case the set contains a CE IPB inverter supply.

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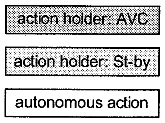
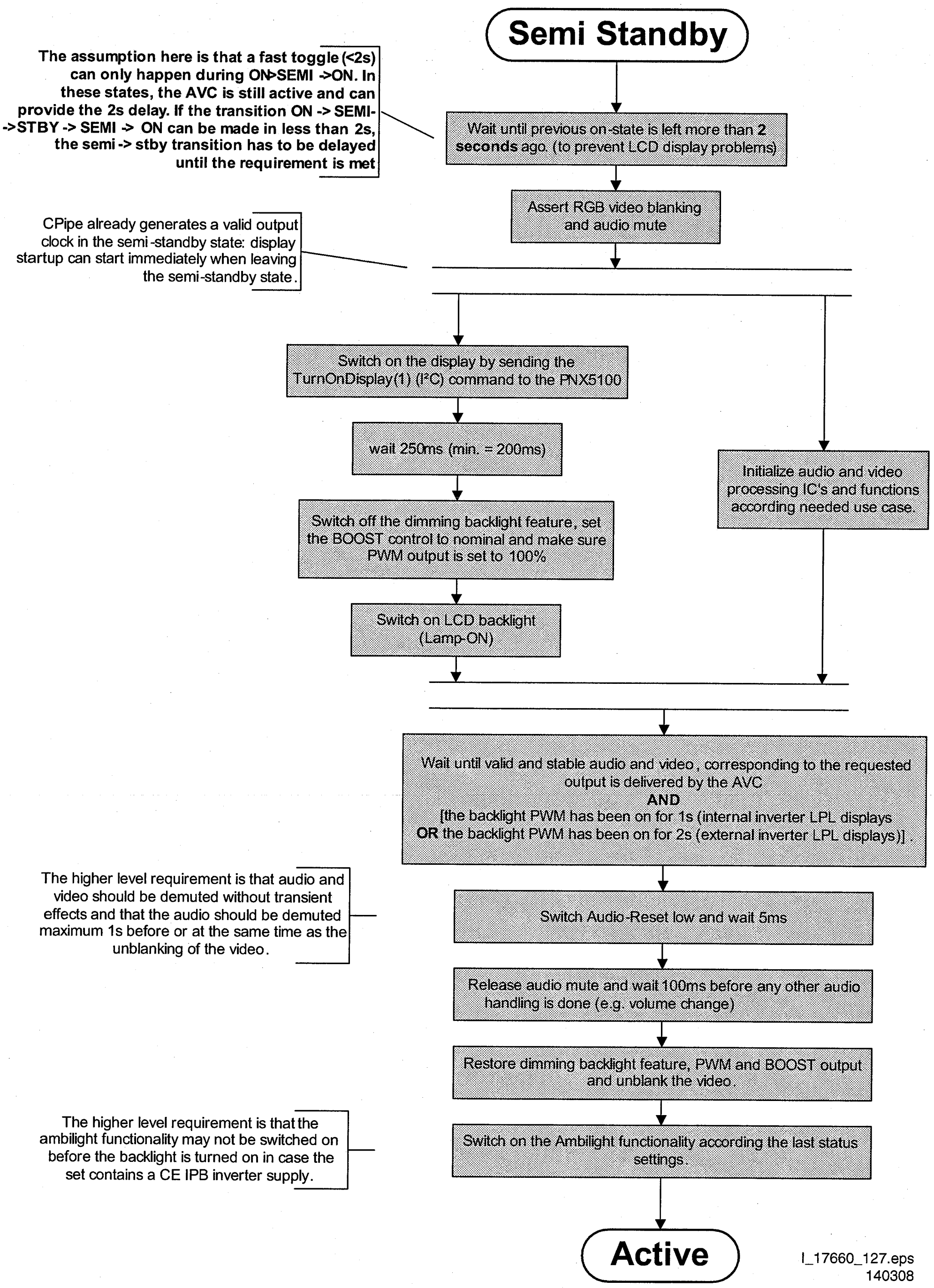
Figure 5-6 “Semi Stand-by” to “Active” flowchart

Constraints taken into account:

- Display may only be started when valid LVDS output clock can be delivered by the AVC.
- Between 5 and 50 ms after power is supplied, display should receive valid lvds clock .
- minimum wait time to switch on the lamp after power up is 200ms.
- To have a reliable operation of the backlight, the backlight should be driven with a PWM duty cycle of 100% during the first second. Only after this first one or two seconds, the PWM may be set to the required output level (Note that the PWM output should be present before the backlight is switched on). To minimize the artefacts, the picture should only be unblanked after these first seconds.


action holder: AVC
action holder: St-by
autonomous action


Semi Standby
Wait until previous on-state is left more than 2 seconds ago. (to prevent LCD display problems)
Assert RGB video blanking and audio mute
Switch on the display by sending the TurnOnDisplay(1) (I²C) command to the PNX5100
wait 250ms (min. = 200ms)
Switch off the dimming backlight feature, set the BOOST control to nominal and make sure PWM output is set to 100%
Switch on LCD backlight (Lamp-ON)
Initialize audio and video processing IC's and functions according needed use case.
Wait until valid and stable audio and video, corresponding to the requested output is delivered by the AVC
AND
[the backlight PWM has been on for 1s (internal inverter LPL displays
OR the backlight PWM has been on for 2s (external inverter LPL displays)].
Switch Audio-Reset low and wait 5ms
Release audio mute and wait 100ms before any other audio handling is done (e.g. volume change)
Restore dimming backlight feature, PWM and BOOST output and unblank the video.
Switch on the Ambilight functionality according the last status settings.
Active

The assumption here is that a fast toggle (<2s) can only happen during ON->SEMI ->ON. In these states, the AVC is still active and can provide the 2s delay. If the transition ON -> SEMI- ->STBY -> SEMI -> ON can be made in less than 2s, the semi -> stby transition has to be delayed until the requirement is met

CPipe already generates a valid output clock in the semi-standby state: display startup can start immediately when leaving the semi-standby state.

The higher level requirement is that audio and video should be demuted without transient effects and that the audio should be demuted maximum 1s before or at the same time as the unblanking of the video.

The higher level requirement is that the ambilight functionality may not be switched on before the backlight is turned on in case the set contains a CE IPB inverter supply.

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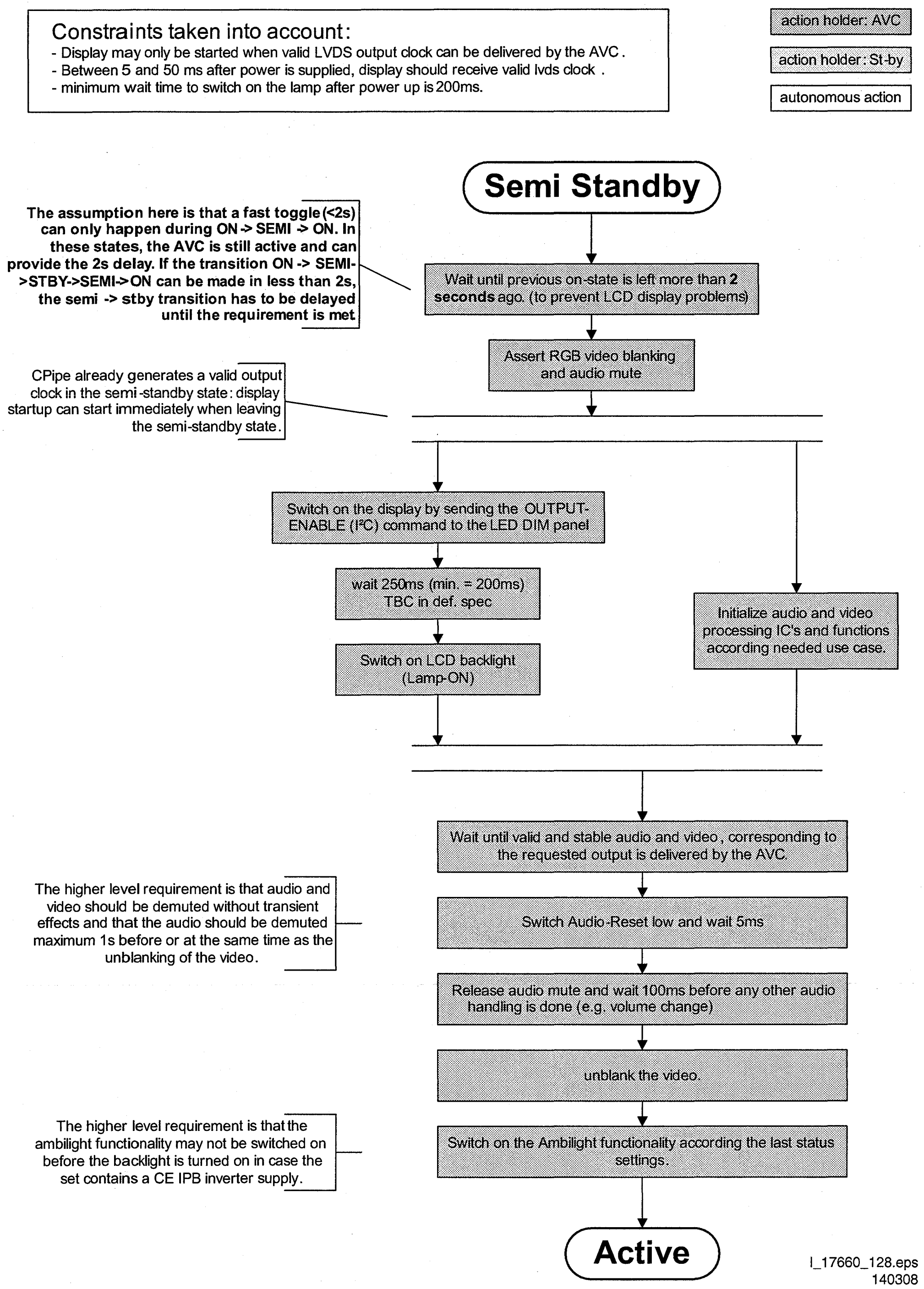
Figure 5-7 “Semi Stand-by” to “Active” flowchart LCD with preheat


action holder: AVC
action holder: St-by
autonomous action
Semi Standby
Wait until previous on-state is left more than 2 seconds ago. (to prevent LCD display problems)
Assert RGB video blanking and audio mute
Switch on the display by sending the OUTPUT-ENABLE (I²C) command to the LED DIM panel
wait 250ms (min. = 200ms) TBC in def. spec
Switch on LCD backlight (Lamp-ON)
Initialize audio and video processing IC's and functions according needed use case.
Wait until valid and stable audio and video, corresponding to the requested output is delivered by the AVC.
Switch Audio-Reset low and wait 5ms
Release audio mute and wait 100ms before any other audio handling is done (e.g. volume change)
unblank the video.
Switch on the Ambilight functionality according the last status settings.
Active

Constraints taken into account:
- Display may only be started when valid LVDS output clock can be delivered by the AVC.
- Between 5 and 50 ms after power is supplied, display should receive valid lvds clock .
- minimum wait time to switch on the lamp after power up is 200ms.

The assumption here is that a fast toggle (<2s) can only happen during ON -> SEMI -> ON. In these states, the AVC is still active and can provide the 2s delay. If the transition ON -> SEMI->STBY->SEMI->ON can be made in less than 2s, the semi -> stby transition has to be delayed until the requirement is met

CPipe already generates a valid output clock in the semi-standby state: display startup can start immediately when leaving the semi-standby state.

The higher level requirement is that audio and video should be demuted without transient effects and that the audio should be demuted maximum 1s before or at the same time as the unblanking of the video.

The higher level requirement is that the ambilight functionality may not be switched on before the backlight is turned on in case the set contains a CE IPB inverter supply.

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Figure 5-8 "Semi Stand-by" to "Active" flowchart (LED backlight)

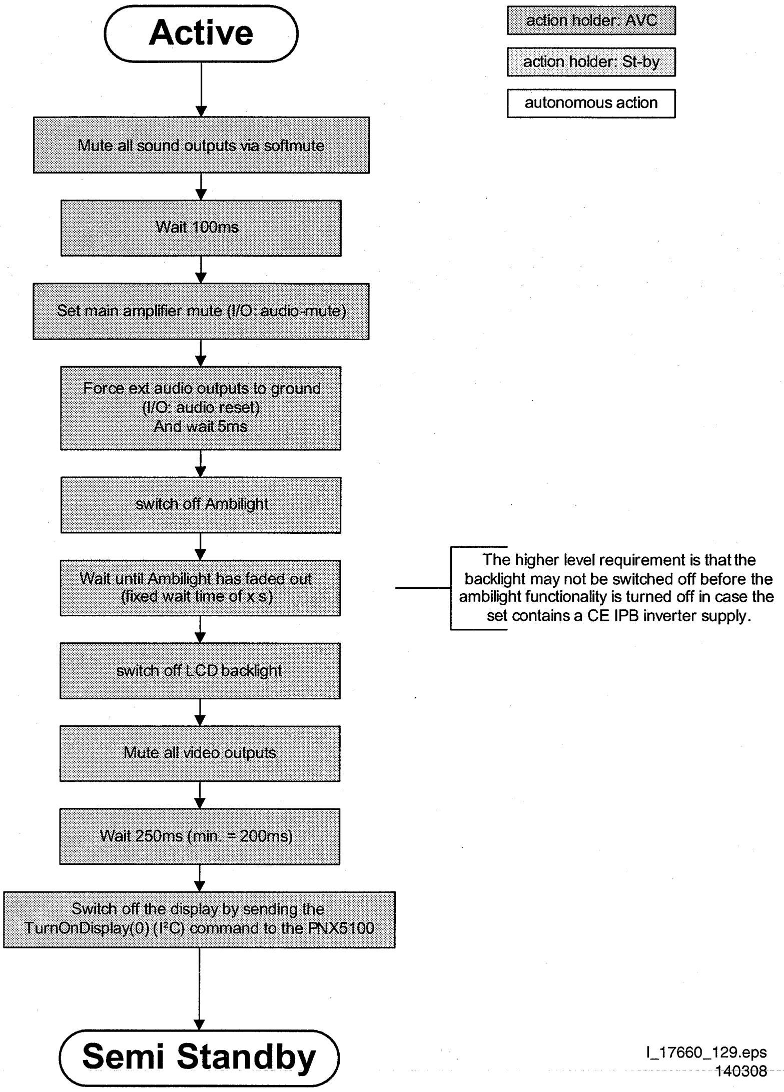
Active
action holder: AVC
action holder: St-by
autonomous action
Mute all sound outputs via softmute
Wait 100ms
Set main amplifier mute (I/O: audio-mute)
Force ext audio outputs to ground
(I/O: audio reset)
And wait 5ms
switch off Ambilight
Wait until Ambilight has faded out
(fixed wait time of x s)
The higher level requirement is that the backlight may not be switched off before the ambilight functionality is turned off in case the set contains a CE IPB inverter supply.
switch off LCD backlight
Mute all video outputs
Wait 250ms (min. = 200ms)
Switch off the display by sending the TurnOnDisplay(0) (I²C) command to the PNX5100
Semi Standby

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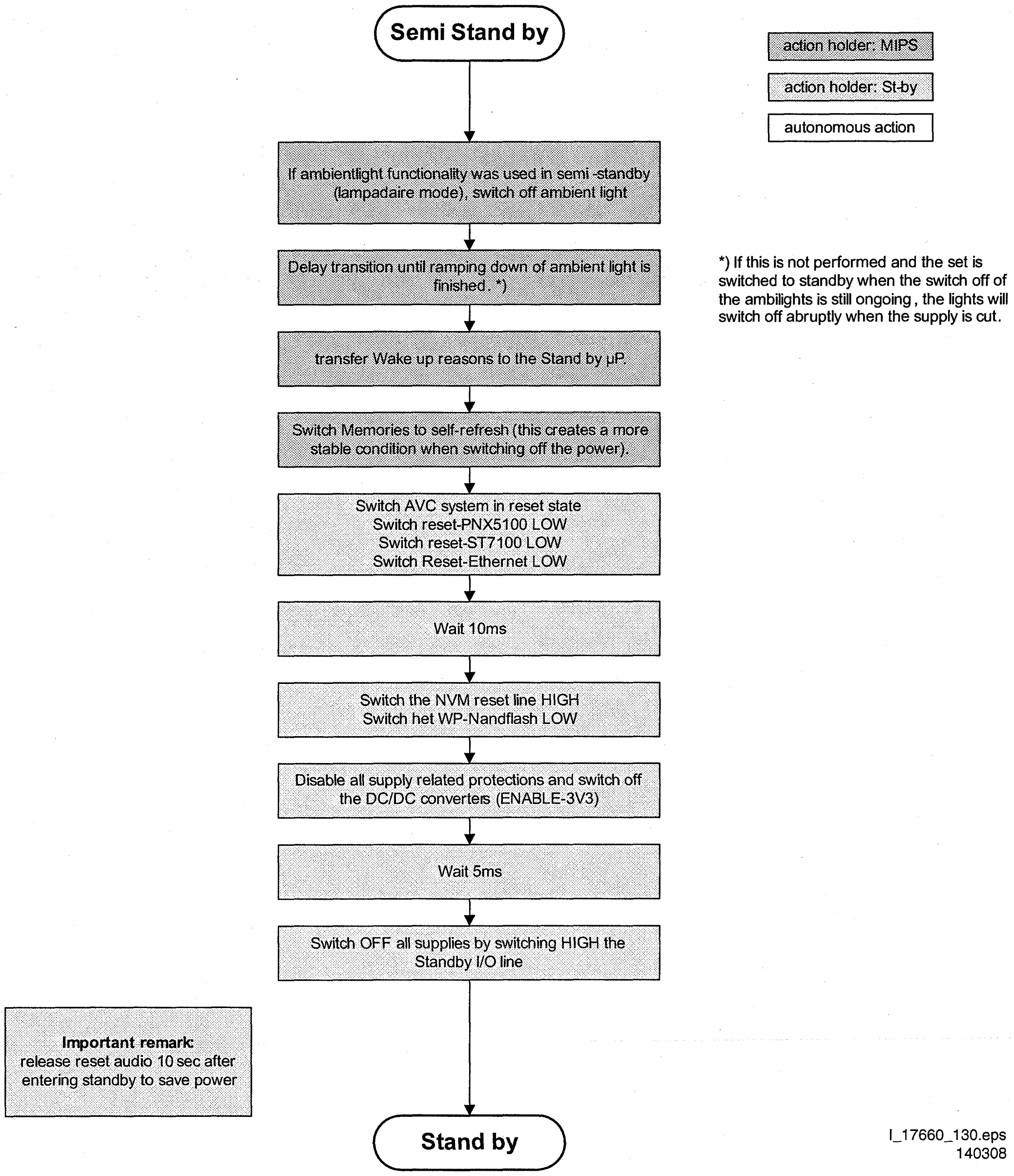
Figure 5-9 “Active” to “Semi Stand-by” flowchart (LCD non DFI)


Semi Stand by
action holder: MIPS
action holder: St-by
autonomous action
If ambientlight functionality was used in semi -standby (lampadaire mode), switch off ambient light
Delay transition until ramping down of ambient light is finished. *)
transfer Wake up reasons to the Stand by µP.
Switch Memories to self-refresh (this creates a more stable condition when switching off the power).
Switch AVC system in reset state
Switch reset-PNX5100 LOW
Switch reset-ST7100 LOW
Switch Reset-Ethernet LOW
Wait 10ms
Switch the NVM reset line HIGH
Switch het WP-Nandflash LOW
Disable all supply related protections and switch off the DC/DC converters (ENABLE-3V3)
Wait 5ms
Switch OFF all supplies by switching HIGH the Standby I/O line
Important remark:
release reset audio 10 sec after entering standby to save power
Stand by

*) If this is not performed and the set is switched to standby when the switch off of the ambilights is still ongoing, the lights will switch off abruptly when the supply is cut.

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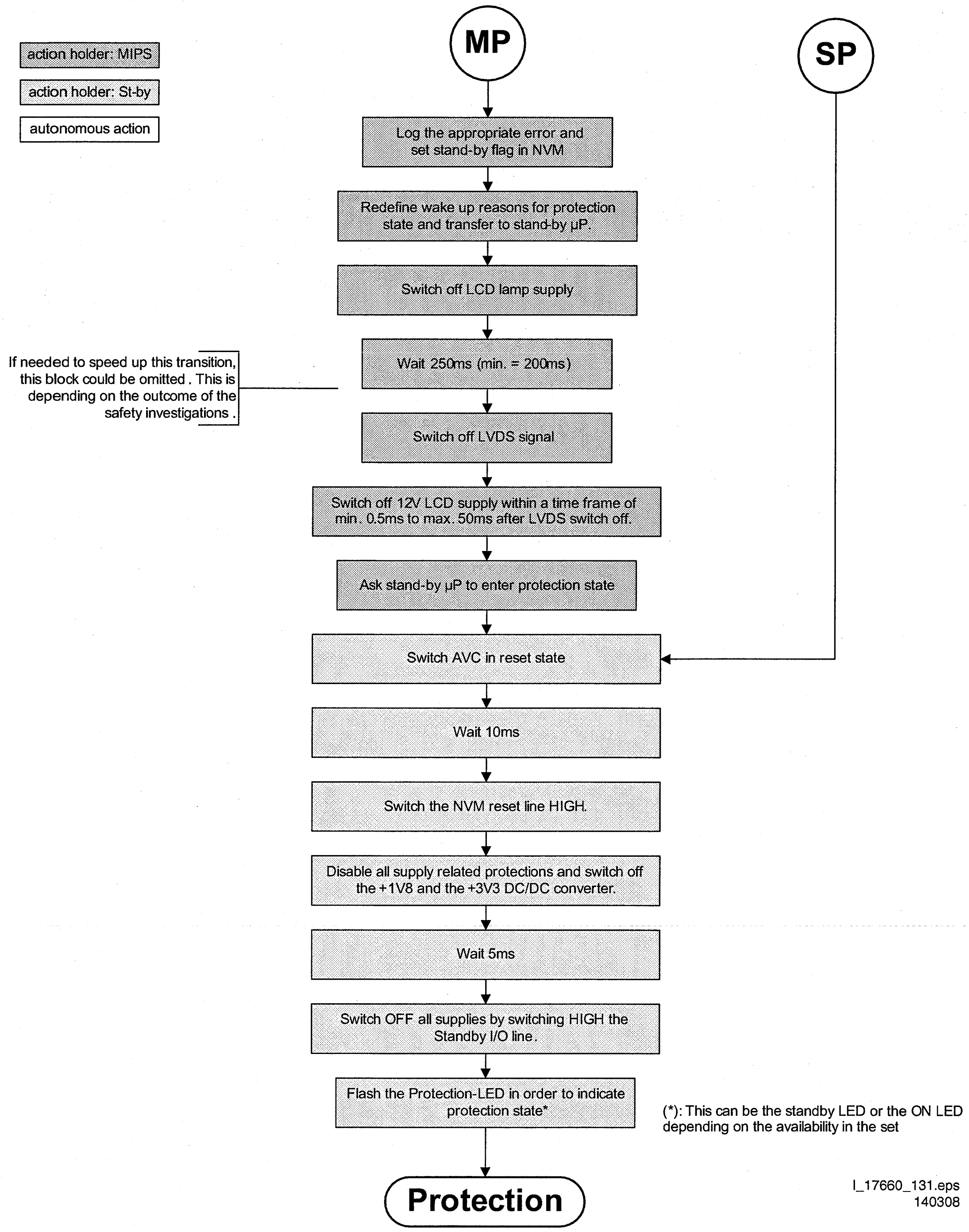
Figure 5-10 “Semi Stand-by” to “Stand-by” flowchart


action holder: MIPS
action holder: St-by
autonomous action
MP
SP
Log the appropriate error and set stand-by flag in NVM
Redefine wake up reasons for protection state and transfer to stand-by µP.
Switch off LCD lamp supply
Wait 250ms (min. = 200ms)
Switch off LVDS signal
Switch off 12V LCD supply within a time frame of min. 0.5ms to max. 50ms after LVDS switch off.
Ask stand-by µP to enter protection state
Switch AVC in reset state
Wait 10ms
Switch the NVM reset line HIGH.
Disable all supply related protections and switch off the +1V8 and the +3V3 DC/DC converter.
Wait 5ms
Switch OFF all supplies by switching HIGH the Standby I/O line.
Flash the Protection-LED in order to indicate protection state*
Protection

If needed to speed up this transition, this block could be omitted. This is depending on the outcome of the safety investigations.

(*): This can be the standby LED or the ON LED depending on the availability in the set

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Figure 5-11 "To Protection State" flowchart

5.4 Service Tools

5.4.1 ComPair

Introduction

ComPair (Computer Aided Repair) is a Service tool for Philips Consumer Electronics products. and offers the following:

1. ComPair helps to quickly get an understanding on how to repair the chassis in a short and effective way.
2. ComPair allows very detailed diagnostics and is therefore capable of accurately indicating problem areas. No knowledge on I^2C or UART commands is necessary, because ComPair takes care of this.
3. ComPair speeds up the repair time since it can automatically communicate with the chassis (when the uP is working) and all repair information is directly available.
4. ComPair features TV software up possibilities.

Specifications

ComPair consists of a Windows based fault finding program and an interface box between PC and the (defective) product. The ComPair II interface box is connected **to the PC** via an USB cable. For the TV chassis, the ComPair interface box and the TV communicate via a bi-directional cable via the service connector(s).

The ComPair fault finding program is able to determine the problem of the defective television, by a combination of automatic diagnostics and an interactive question/answer procedure.

How to Connect

This is described in the chassis fault finding database in ComPair.

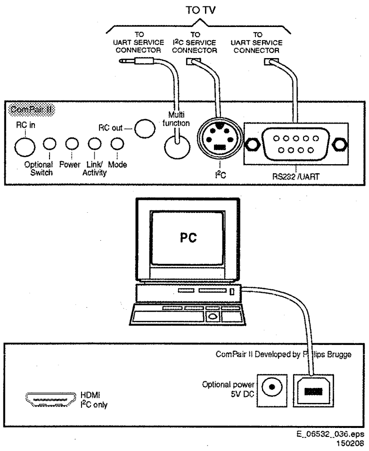


Figure 5-12 ComPair II interface connection

Caution: It is compulsory to connect the TV to the PC as shown in the picture above (with the ComPair interface in between), as the ComPair interface acts as a level shifter. If one connects the TV directly to the PC (via UART), ICs will be blown!

How to Order

ComPair II order codes:

- ComPair II interface: 3122 785 91020.
- Software is available via internet: http://www.atyourservice.ce.philips.com
- ComPair UART interface cable for Q52x.x. (using 3.5 mm Mini Jack connector): 3104 311 12742.

Note: While encounting problems, contact the local support desk.

5.4.2 Memory and Audio Test

With this tool you can test the memory of the PNX8541, as well if the PNX5100 is enabled and audio-testing.

What is needed?

- An USB-stick.
- "TESTSCRIPT Q529" (3104 337 05021). Downloadable from the Philips Service website from the section "Software for Service only".
- A ComPair/service cable (3104 311 12742)

Procedure

Create a directory "JETTFILES" under the root of the USB-stick

- Place "MemoryTestPNX8635.bin" and "autojett.bin" (available in "TESTSCRIPT Q529") under the directory "JETTFILES"
- Install the computer program "BOARDTESTLOGGER" (available in "TESTSCRIPT Q529") on the PC
- Connect a "ComPair/service"-cable from the service-connector in the set to the COM1-port of the PC
- Start-up the program "BOARDTESTLOGGER" and select "COM1"
- Put the USB stick into the TV and startup the TV while pressing the "i+"-button on a Philips DVD RC6 remote control (it's also possible to use a TV remote in "DVD"-mode)
- On the PC the memory test is shown now. This is also visible on the TV screen.
- In "BOARDTESTLOGGER" an option "Send extra UART command" can be found where you can select "AUD1". This command generates hear test tones of 200, 400, 1000, 2000, 3000, 5000, 8000 and 12500Hz.

5.4.3 LVDS Tool

Support of this LVDS Tool has been discontinued.

5.5 Error Codes

5.5.1 Introduction

The error code buffer contains all detected errors since the last time the buffer was erased. The buffer is written from left to right, new errors are logged at the left side, and all other errors shift one position to the right.

When an error occurs, it is added to the list of errors, provided the list is not full. When an error occurs and the error buffer is full, then the new error is not added, and the error buffer stays intact (history is maintained).

To prevent that an occasional error stays in the list forever, the error is removed from the list after more than 50 hrs. of operation.

When multiple errors occur (errors occurred within a short time span), there is a high probability that there is some relation between them.

Below the way errors will be displayed on the HUB:

- There is a simple blinking LED procedure for board level repair (home repair) so called LAYER 1 errors next to the existing errors which are LAYER 2 errors.(see table 5-2 error code overview).
  - LAYER 1 errors are one digit errors.
  - LAYER 2 errors are 2 digit errors.
- In protection mode.
  - From consumer mode: **LAYER 1.**
  - From SDM mode: **LAYER 2.**
- **Fatal errors, if I2C bus is blocked and the set reboots, CSM and SAM are not selectable.**
  - From consumer mode: **LAYER 1.**
  - From SDM mode: **LAYER 2.**

    Important remark:

    For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER error 1 blinking), one should short the solder paths at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.
- In CSM mode
  - When entering CSM: error **LAYER 1** will be displayed by blinking LED. Only the latest error is shown.
- In SDM mode
  - When SDM is entered via Remote Control code or the hardware pins, **LAYER 2** is displayed via blinking LED on the HUB.
- In the ON state
  - In "Display error mode", set with the RC commands "mute_06250X _OK" **LAYER 2** errors are displayed via blinking LED on the HUB.
- Error display on screen.
  - In CSM no error codes are displayed on screen.
  - In SAM the complete error list from the HUB only is shown!

Basically there are three kinds of errors:

- **Errors detected by the Stand-by software which lead to protection.** These errors will always lead to protection and an automatic start of the blinking LED (HUB) LAYER error 1.(see section "5.6 The Blinking LED Procedure").
- **Errors detected by the Stand-by software which not lead to protection.** In this case the LED from the HUB should blink the involved error. See also section "5.5 Error Codes, 5.5.4 Error Buffer, Extra Info". Note that it can take

up several minutes before the TV starts blinking the error (e.g. LAYER error 1 = 2, LAYER error 2 = 15 or 53).
- **Errors detected by main software (MIPS).** In this case the error will be logged into the error buffer and can be read out via ComPair, via blinking LED method LAYER error 1-2, or in case picture is visible, via SAM.

Important remark :
Errors on the monitor are displayed by blinking LED only during the start up.They will be displayed only once or twice.

5.5.2 How to Read the Error Buffer

Use one of the following methods:
- On screen via the SAM (only when a picture is visible). E.g.:
  - **00 00 00 00 00**: No errors detected
  - **23 00 00 00 00**: Error code 23 is the last and only detected error.
  - **37 23 00 00 00**: Error code 23 was first detected and error code 37 is the last detected error.
  - Note that no protection errors can be logged in the error buffer.
- Via the blinking LED procedure. See section 5.5.3 How to Clear the Error Buffer.
- Via ComPair.

5.5.3 How to Clear the Error Buffer

Use one of the following methods:
- By activation of the “RESET ERROR BUFFER” command in the SAM menu.
- With a normal RC, key in sequence “MUTE” followed by “062599” and “OK”.
- If the content of the error buffer has not changed for 50+ hours, it resets automatically.

5.5.4 Error Buffer

In case of non-intermittent faults, clear the error buffer before starting to repair (**before** clearing the buffer, write down the content, as this history can give significant information). This to ensure that old error codes are no longer present.
If possible, check the entire contents of the error buffer. In some situations, an error code is only the result of another error code and not the actual cause (e.g. a fault in the protection detection circuitry can also lead to a protection).
There are several mechanisms of error detection:
- Via error bits in the status registers of ICs.
- Via polling on I/O pins going to the stand-by processor.
- Via sensing of analog values on the stand-by processor or the PNX8541.
- Via a “not acknowledge” of an I^2C communication.

Take notice that some errors need several minutes before they start blinking or before they will be logged. So in case of problems wait 2 minutes from start-up onwards, and then check if the front LED is blinking or if an error is logged.

Table 5-2 Error code overview

Description	Layer 1	Layer 2	Monitored by	Error/ Prot	Error Buffer/ Blinking LED	Device	Defective Board
I^{2}C3	2	13	MIPS	E	BL / EB	SCL/D-SSB	SSB
I^{2}C4	5	14	MIPS	E	BL / EB	SCL/D-DISP	Display (LED back light only)
PNX doesn't boot (HW cause)	2	15	Stby µP	E	BL	PNX8541 I^{2}C blocked	SSB
12V	3	16	Stby µP	P	BL	/	Supply
1V2, 3V3, 5V to low	2	18	Stby µP	P	BL	/	SSB
1V2 or Class D	2	19	Stby µP	P	BL	/	SSB
3V3/5V DCDC to high	2	11	Stby µP	P	BL	/	SSB
Temp protection	3	12	MIPS	P	BL/EB	LM75	SSB
PNX 5100	2	21	MIPS	E	EB	PNX5100	SSB
HDMI mux	2	23	MIPS	E	EB	AD8197A	SSB
I^{2}C switch	2	24	MIPS	E	EB	PCA9540	SSB
Master IF	2	26	MIPS	E	EB	TDA9898	SSB
FPGA Ambilight	2	28	MIPS	E	EB	/	SSB
Tuner	2	34	MIPS	E	EB	UV1783S/TD1716	SSB
Channel Decoder DVB-T	2	37	MIPS	E	EB	TDA10048	SSB
ST7100	2	38	MIPS	E	EB	ST7100	SSB
main NVM	2	/	MIPS	E	X	STM24C128	SSB
Channel decoder DVB-C	2	48	MIPS	E	EB	TDA 10023	SSB
PNX doesn't boot (SW cause)	2	53	Stby µP	E	BL	PNX8541	SSB
DP Tx	6	54	MIPS	E	EB	GM60028	LVDS2DP
FPGA LVDS Rx	6	55	MIPS	E	EB		
DP port not connected	5	56	MIPS	E	EB	DP cable/monitor	/

Extra Info

- **Rebooting.** When a TV is constantly rebooting due to internal problems, most of the time no errors will be logged or blinked. This rebooting can be recognized via a ComPair interface and Hyperterminal (for Hyperterminal settings, see section "5.8 Fault Finding and Repair Tips, 5.8.5 Logging). It's shown that the loggings which are generated by the main software keep continuing. In this case diagnose has to be done via ComPair.
- **Error 11 (3V3/5V too high)**. This protection can occur during start up (LAYER error 1 = 2). Be careful to overrule this protection via SDM for the reason supply related devices can be possibly destroyed here.
- **Error 12 (Temp protection)**. Current situation: when temperature rises above limit inside the HUB, the protection is triggered and the TV set is switched "OFF". No indication will be displayed on the LED of the HUB, yet error layer = 12 is logged and will be displayed when SDM is active.
- **Error 13 (I^{2}C bus 3 blocked)**. At the time of release of this manual, this error was not working as expected. Current situation: when this error occurs, the TV will constantly reboot due to the blocked bus. The best way for further diagnosis here, is to use ComPair.
- **Error 15 (PNX8541 doesn't boot)**. Indicates that the main processor was not able to read his bootscript. This error will point to a hardware problem around the PNX8541 (supplies not OK, PNX 8541 completely dead, I^{2}C link between PNX and Stand-by Processor broken, etc...). When error 15 occurs it is also possible that I^{2}C2 bus is blocked (NVM). I^{2}C2 can be indicated in the schematics as follows: SCL-UP-MIPS, SDA-UP-MIPS, SCL-2 or SDA-2. Other root causes for this error can be due to hardware problems with : NVM PNX5100, PNX5100 itself, DDR's.
- **Error 16 (12V)**. This voltage is made in the power supply of the HUB and results in protection (LAYER error 1 = 3) in case of absence. When SDM is activated we see blinking LED LAYER error 2 = 16.
- **Error 18 (1V2-3V3-5V too low)**. All these supplies are generated by the DC/DC supply on the SSB. If one of these supplies is too low, protection occurs and blinking LED LAYER error 1 = 2 will be displayed automatically. In SDM this gives LAYER error 2 = 18.
- **Error 19 (1V2 or class D)**. If one of the 1V2 supplies is too high or too low in the start up procedure the supply fault becomes low.
- **Error 21 (PNX 5100)**. At the time of release of this manual, this error was not working as expected. Current situation: when there is no I^{2}C communication towards the PNX5100 after startup (power off by disconnection of the mains cord), LAYER error 2 will blink continuously via the blinking LED procedure in SDM. (startup the TV with the solder paths short to activate SDM).
- **Error 23 (HDMI)**. When there is no I^{2}C communication towards the HDMI mux after start up, LAYER error 2 = 23 will be logged and displayed via the blinking LED procedure if SDM is switched on.
- **Error 26 (Master IF)**. When there is no I^{2}C communication towards the Master IF after start up, LAYER error 2 = 26 will be logged and displayed via the blinking LED procedure when SDM is switched on.
- **Error 28 (FPGA ambilight)**. When there is no I^{2}C communication towards the FPGA ambilight after start up, LAYER error 2 = 28 will be logged and displayed via the blinking LED procedure if SDM is switched on. Note that it can take up several minutes before the TV starts blinking LAYER error 1 = 2 in CSM or in SDM, LAYER error 2 = 28.
- **Error 34 (Tuner)**. When there is no I^{2}C communication towards the tuner after start up, LAYER error 2 = 34 will be logged and displayed via the blinking LED procedure when SDM is switched on.
- **Error 37 (Channel decoder DVBT)**. When there is no I^{2}C communication towards the DVBT channel decoder after start up, LAYER error 2 = 37 will be logged and displayed via the blinking LED procedure if SDM is switched on.
- **Error 38 (STI7100)**. When there is no I^{2}C communication towards the STI7100 after startup (power off by disconnection of the mains cord), LAYER error 2 = 38 will be logged and displayed via the blinking LED procedure in SDM (startup the TV with the solder paths short to activate SDM). Remark : if the error occurs during the ON state, the TV will constantly reboot and no LED blinking will be displayed. This rebooting can be recognized via a ComPair interface and Hyperterminal (for Hyperterminal settings, see section "5.8 Fault Finding and Repair Tips, 5.8.5 Logging"). It is shown that the loggings which are

generated by the main software keep continuing. Check in the logging for keywords like e.g. “Device error 38”.

- **Main NVM HUB**. When there is no I^2C communication towards the main NVM, LAYER error 1 = 2 will be displayed via the blinking LED procedure. In SDM, LAYER error 2 can be 19 here. Check the logging for keywords like “I^2C bus blocked”.
- **Error 48 (Channel decoder DVBC)**. When there is no I^2C communication towards the DVBC channel decoder after start up, LAYER error 2 = 48 will be logged and displayed via the blinking LED procedure while SDM is active.
- **Error 53.** This error will indicate that the PNX8541 has read his bootscript (when this would have failed, error 15 would blink) but initialization was never completed because of hardware problems (NAND flash, ...) or software initialization problems. Possible cause could be that there is no valid software loaded (try to upgrade to the latest main software version). Note that it can take up to 2 minutes before the TV starts blinking LAYER error 1 = 2 or in SDM, LAYER error 2 = 53.
- **Error 55 (FPGA LVDS Rx)**. At the time of release of this manual, this error was not working as expected. Current situation: When there is no I2C communication towards the LVDS2DP panel, the TV set will start rebooting and no blinking on the hub will be displayed. The reset-start spacer is displayed on the monitor LED once in a while as start of the error blinking but none are logged. Because no picture is available, the only way to detect failure on the FPGA device is to check in the logging from the hub (via service connector hub) prints as: “setting lvdsrx output enable to 1, was 0”. This betrays the failure of the FPGA LVDS Rx.

5.5.5 Monitor Errors for Essence

When an error of the monitor appears, it is displayed by a blinking LED on the monitor triggered via the acknowledge of the failing device. This is only once or twice. When the error dissappears or when the I2C command is not repeated, the blinking LED stops. Resetting the errors of the monitor is not possible via the item “clear errors” in SAM and can not be read out either in the error buffer, they only will be displayed via blinking LED during start-up.

Table 5-3 Start-up errors Essence

Defect	Action	Error on E-box	Error on monitor
Supply cable and DP cable unplugged	Start up with mains cord or tact switch (HUB)	Blinking LED error 5 Logging error 56 (layer 2)	No LED
Supply cable and DP cable unplugged	Start up from Standby with RC6 (monitor)	No reaction	No LED and no RC6 blinking
Supply cable unplugged	Start up with mains cord or tact switch (HUB)	Blinking LED error 5 Logging error 56 (layer 2)	Standby
Supply cable unplugged	Start up from Standby with RC6 (monitor)	Blinking LED error 5 Logging error 56 (layer 2)	RC6 blinking, Standby LED, no error
DP cable unplugged	Start up with mains cord or tact switch (HUB)	Blinking LED error 5 Logging error 56 (layer 2)	No picture, no error
DP cable unplugged	Start up from Standby with RC6 (monitor)	No RC 6 blinking Standby	No picture, no error
E-box defect	Supply fault	Blinking LED error 3 Logging error layer 2 if possible	if no 24V : Standby 24V=OK : no picture, no error
E-box defect	SSB defect, DP initialized	Blinking LED error 2 Logging error layer 2	No error
E-box defect	SSB defect, DP not initialized	Blinking LED error 2 Logging error layer 2	No picture, no error
E-box defect	DP boar defect	Blinking LED error 6 Logging error layer 2	No picture, no error
Monitor defect	FPGA	No error	Blinking LED error 2 Logging error 2
Monitor defect	3V3 monitor	Blinking LED error 5 Logging error 56 (layer 2)	Blinking LED error 3 Logging error 3
Monitor defect	12V monitor	Blinking LED error 5 Logging error 56 (layer 2)	Blinking LED error 4 Logging error 4
Monitor defect	DP port defect	Blinking LED error 5 Logging error 56 (layer 2)	No picture, no error
Monitor defect	DP RX	Blinking LED error 5 Logging error 56 (layer 2)	Blinking LED error 6 Logging error 6
Monitor defect	NVM	No error	Blinking LED error 7, No logging possible

Extra Info

- At the time of release of this manual, errors as mentioned above in table 5-3 can possibly not fully work as expected due to unresolved software bugs.

5.6 The Blinking LED Procedure

5.6.1 Introduction

The blinking LED procedure can be split up into two situations:
- Blinking LED procedure LAYER error 1. In this case the error is automatically blinked when the TV is put in CSM. This will be only one digit error, namely the one that is referring to the defective board (see table "Table 5-2 Error code overview") which causes the failure of the TV. This approach will especially be used for home repair and call centres. The aim here is to have service diagnosis from a distance.
- Blinking LED procedure LAYER error 2. Via this procedure, the content of the error buffer can be made visible via the front LED of the HUB. In this case the error contains 2 digits (see table "Table 5-2 Error code overview") and will be displayed when SDM (hardware pins) is activated. This is especially useful for fault finding and gives more details regarding the failure of the defective board.

  Important remark:
  For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER error 1 blinking), one should short the solder paths at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.

When one of the blinking LED procedures is activated, the front LED of the HUB will show (blink) the content of the error buffer. Error codes greater then 10 are shown as follows:
1. "n" long blinks (where "n" = 1 to 9) indicating decimal digit
2. A pause of 1.5 s
3. "n" short blinks (where "n"= 1 to 9)
4. A pause of approximately 3 s,
5. When all the error codes are displayed, the sequence finishes with a LED blink of 3 s
6. The sequence starts again.

Example: Error 12 8 6 0 0.
After activation of the SDM, the front LED will show:
1. One long blink of 750 ms (which is an indication of the decimal digit) followed by a pause of 1.5 s
2. Two short blinks of 250 ms followed by a pause of 3 s
3. Eight short blinks followed by a pause of 3 s
4. Six short blinks followed by a pause of 3 s
5. One long blink of 3 s to finish the sequence
6. The sequence starts again.

5.6.2 How to Activate

Use one of the following methods:
- **Activate the CSM.** The blinking front LED of the HUB will show only the latest layer error 1, this works in "normal operation" mode or automatically when the error/protection is monitored by the standby processor. At the time of this release, this layer error 1 blinking was not working as expected.
  In case no picture is shown and there is no LED blinking, read the logging to detect whether "error devices" are mentioned. (see section "5.8 Fault Finding and Repair Tips, 5.8.5 Logging").
- **Activate the SDM.** The blinking front LED of the HUB will show the entire contents of the layer error 2 buffer, this works in "normal operation" mode or when SDM (via hardware pins) is activated when the tv set is in protection.
  Important remark:
  For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER error 1 blinking), one should short the solder paths at start up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.
- **Transmit the commands "MUTE" - "062500" - "OK" with a normal RC.** The complete error buffer is shown. Take notice that it takes some seconds before the blinking LED starts.
- **Transmit the commands "MUTE" - "06250x" - "OK" with a normal RC** (where "x" is a number between 1 and 5). When x = 1 the last detected error is shown, x = 2 the second last error, etc.... Take notice that it takes some seconds before the blinking LED starts.

5.7 Protections

5.7.1 Software Protections

Most of the protections and errors use either the stand-by microprocessor or the MIPS controller as detection device. Since in these cases, checking of observers, polling of ADCs, and filtering of input values are all heavily software based, these protections are referred to as software protections.
There are several types of software related protections, solving a variety of fault conditions:
- **Protections related to supplies:** check of the 12V, +5V, +3V3 and 1V2.
- **Protections related to breakdown of the safety check mechanism.** E.g. since the protection detections are done by means of software, failing of the software will have to initiate a protection mode since safety cannot be guaranteed any more.

Remark on the Supply Errors
The detection of a supply dip or supply loss during the normal playing of the set does not lead to a protection, but to a cold reboot of the set. If the supply is still missing after the reboot, the TV will go to protection.

Protections during Start-up
During TV start-up, some voltages and IC observers are actively monitored to be able to optimize the start up speed, and to assure good operation of all components. If these monitors do not respond in a defined way, this indicates a malfunction of the system and leads to a protection. As the observers are only used during start up, they are described in the start up flow in detail (see section "5.3 Stepwise Start-up").

5.7.2 Hardware Protections

The only real hardware protection in this chassis appears in case of an audio problem e.g. DC voltage on the speakers. The DC check circuit pulls the "A-STBY" line low and will paralize the Class-D audio.

5.7.3 Important remark regarding the blinking LED indication

As for the blinking LED indication, the blinking of error layer 1 can be switched off by pushing the power button on the keyboard.
This condition is not valid after the set was unpowered (via mains interruption). The blinking LED starts again and can only be switched off by unplugging the mains connection.
This can be explained by the fact that the MIPS can not load the keyboard functionality from software during the start up and doesn't recognizes the keyboard commands at this time.

5.8 Fault Finding and Repair Tips

Read also section “5.5 Error Codes, 5.5.4 Error Buffer, Extra Info”.

5.8.1 Audio Amplifier

The Class D-IC 7D10 has a powerpad for cooling. When the IC is replaced it must be ensured that the powerpad is very well pushed to the PCB while the solder is still liquid. This is needed to insure that the cooling is guaranteed, otherwise the Class D-IC could break down in short time.

5.8.2 CSM

When CSM is activated and there is a USB stick connected to the TV, the software will dump the complete CSM content to the USB stick. The file (CSM.txt) will be saved in the root of the USB stick. If this mechanism works it can be concluded that a large part of the operating system is already working (MIPS, USB...)

5.8.3 DC/DC Converter

Introduction

The onboard supply consists of 5 DC/DC converters and 7 linear stabilizers. The DC/DC converters have all +12V input voltage and deliver:

1. +1V2-PNX8541 supply voltage, stabilised close to PNX8541 chip.
2. +1V2-PNX5100 supply voltage, stabilised close to PNX5100 chip.
3. +3V3 (overall 3.3 V for onboard IC’s).
4. +5V for USB and Conditional Access Interface and +5V5-TUN tuner stabilizer.
5. +33VTUN for analogue only tuners **(AP diversity)**.

The linear stabilizers are providing:

1. +1V supply voltage (out of +1V2-PNX8541), stabilized close to ST7101 chip **(MPEG4 diversity)**.
2. +1V8-PNX5100.
3. +1V8-PNX8541 (**reserved** because +1V8-PNX5100 used also for DDR2 interface of PNX8541 via 5FB0).
4. +2V5 (**MPEG4 diversity**).
5. +1V2-STANDBY (out of +3V3-STANDBY).
6. +5V-TUN (out of +5V5-TUN).
7. +3V3-STANDBY (out of +12V, **reserved**).

+3V3-STANDY and +1V2-STANDBY are permanent voltages. Supply voltages +1V2-PNX8541, +1V2-PNX5100 and +1V are started immediately when +12V incoming voltage is available (+12V is enabled by STANDBY signal, active low). Supply voltages +3V3, 2V5, +1V8-PNX5100, +1V8-PNX8541, +5V and +5V-TUN are switched-on directly by signal ENABLE-3V3 (active low) when +12V and previous mentioned voltages are all available.

Debugging

The best way to find a failure in the DC/DC converters is to check their starting-up sequence at power-on via the mains cord, presuming that the standby microprocessor and the external supply are operational. Take STANDBY signal high-to-low transition as reference.
When +12V rises above 10V then +1V2-PNX8541, +1V2-PNX5100 and +1V are started immediately. Then, after ENABLE-3V3 goes low, all the other supply voltages should rise within 10 ms. Boost voltages should be OK when +1V2-PNX8541, +1V2-PNX5100 are available (FU07 and FU8A, around 19V).
SUPPLY-FAULT signal should be high when all supply voltages are started-up.

Tips

- Usually, when supply voltage is short-circuited to GND, the corresponding DC/DC converter is making audible noise.
- The drop voltage across resistors 3U70 and 3U3T is 100 mV to 2000 mV.
- Defective (in short-circuit) power MOS-FET’s lead usually to their controller IC broken; if one or more high-side MOS-FET’s (7U05, 7U08, 7U0D-1 or 7U0H-1) is broken then the platform can be heavily damaged if started in SDM-mode (SUPPLY-FAULT signal is then ignored, while higher than normal supplies will be generated).
- The +33VTUN generator circuit (7U0P + 7U0Q + surrounding components) has low output current capability. In case of too low or no output voltage check transistor 7U0P (gate voltage pulses of about 10 V amplitude and drain voltage pulses of about 35 V amplitude) and the load (not more than 4.5 mA).
- High output ripple voltage of DC/DC converters can be caused by defective (cracked or bad soldered) ceramic capacitors in the feedback (DC or AC) input or output filtering.

5.8.4 Exit “Factory Mode”

When an “F” is displayed in the screen's right corner, this means that the set is in “Factory” mode, and it normally happens after a new SSB has been mounted.
To exit this mode, push the “VOLUME minus” button on the TV's local keyboard control for 10 seconds (this disables the continuous mode).
Now push the “MENU” button for 10 seconds untill the “F” disappears from the screen.

5.8.5 Logging

When something is wrong with the TV set (f.i.the set is rebooting) you can check for more information via the logging in Hyperterminal. The Hyperterminal is available in every Windows application via Programs, Accessories, Communications, Hyperterminal. Connect a “ComPair UART”-cable (3104 311 12742) from the service connector in the TV set to the “COM1”-port of the PC. After start-up of the Hyperterminal, fill in a name (f.i. “logging”) in the “Connection Description” box, then apply the following settings:
1. COM1
2. Bits per second = 38400
3. Data bits = 8
4. Parity = none
5. Stop bits = 1
6. Flow control = none

During the start-up of the TV set, the logging will be displayed. This is also the case during rebooting of the TV set (the same logging appears time after time). Also available in the logging is the “Display Option Code” (useful when there is no picture), look for item “DisplayRawNumber” in the beginning of the logging. Tip: when there is no picture available during rebooting you are able to check for “error devices” in the logging (LAYER 2 error) which can be very helpful to determine the failure cause of the reboot. For protection state, there is no logging.

5.8.6 Loudspeakers

Make sure that the volume is set to minimum during disconnecting the speakers in the ON-state of the TV. The audio amplifier can be damaged by disconnecting the speakers during ON-state of the set! Sometimes the set can go into protection, but that is not always the case.

5.8.7 Tuner

Attention: In case the tuner is replaced, always check the tuner options!

5.8.8 UI over PCI bus

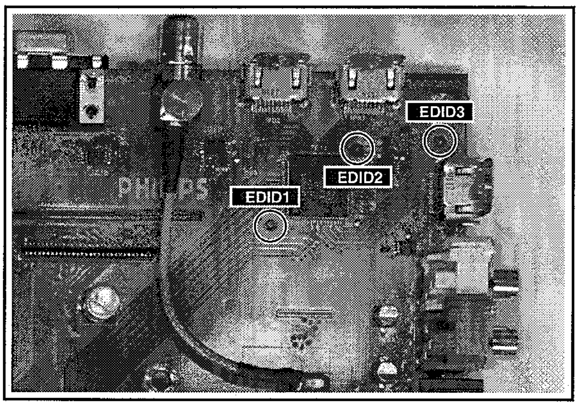
The UI is not integrated in the RGB signal but is send from PNX8541 to PNX5100 via the PCI bus. TXT and MHEG are integrated in the RGB signal. So when TXT signal is available but no UI, check the PCI bus.

5.8.9 Display option code

Attention: In case the SSB is replaced, always check the display option code in SAM, even when picture is available. Performance with the incorrect display option code can lead to unwanted side-effects for certain conditions.

5.8.10 Upgrade EDID NVM

To upgrade the EDID NVM pin 7 of the EDID NVM has to be short circuited to ground. Therefore some test points are foreseen (figure “EDID-NVM pins”). See ComPair for further instructions.



I_18020_145.eps
190908

Figure 5-13 EDID-NVM pins

5.8.11 SSB Replacement

Follow the instructions in the flowchart in case a SSB has to be exchanged. See figure “SSB replacement flowchart”.

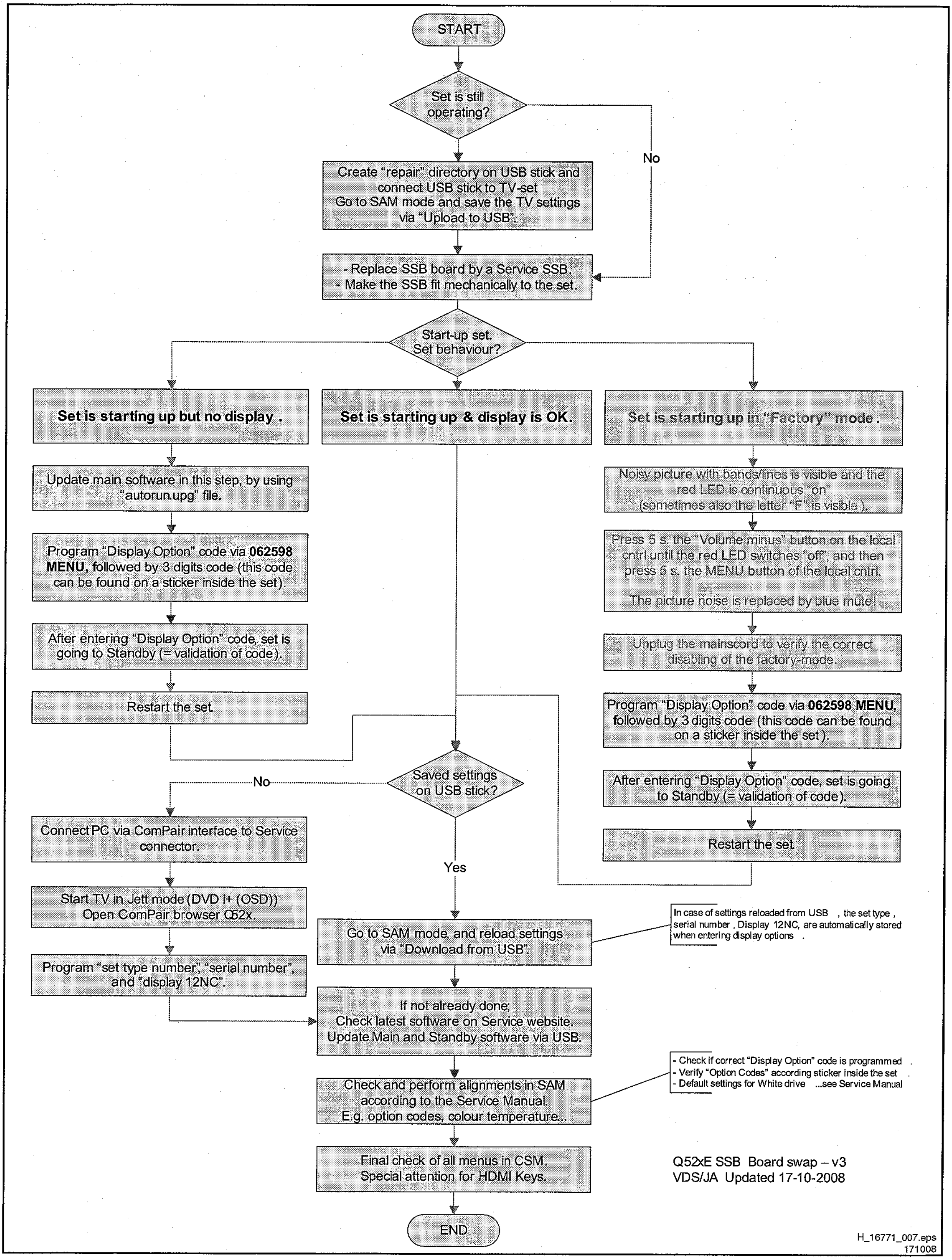

START
Set is still operating?
No
Create "repair" directory on USB stick and connect USB stick to TV-set
Go to SAM mode and save the TV settings via "Upload to USB".
- Replace SSB board by a Service SSB.
- Make the SSB fit mechanically to the set.
Start-up set. Set behaviour?
Set is starting up but no display .
Set is starting up & display is OK.
Set is starting up in "Factory" mode .
Update main software in this step, by using "autorun.upg" file.
Program "Display Option" code via 062598 MENU, followed by 3 digits code (this code can be found on a sticker inside the set).
After entering "Display Option" code, set is going to Standby (= validation of code).
Restart the set.
Noisy picture with bands/lines is visible and the red LED is continuous "on" (sometimes also the letter "F" is visible).
Press 5 s. the "Volume minus" button on the local cntrl until the red LED switches "off", and then press 5 s. the MENU button of the local cntrl.
The picture noise is replaced by blue mute!
Unplug the mainscord to verify the correct disabling of the factory-mode.
Program "Display Option" code via 062598 MENU, followed by 3 digits code (this code can be found on a sticker inside the set).
After entering "Display Option" code, set is going to Standby (= validation of code).
Restart the set.
Saved settings on USB stick?
No
Yes
Connect PC via ComPair interface to Service connector.
Start TV in Jett mode (DVD i+ (OSD)) Open ComPair browser Q52x.
Program "set type number", "serial number", and "display 12NC".
Go to SAM mode, and reload settings via "Download from USB".
In case of settings reloaded from USB , the set type , serial number , Display 12NC, are automatically stored when entering display options .
If not already done; Check latest software on Service website. Update Main and Standby software via USB.
Check and perform alignments in SAM according to the Service Manual. E.g. option codes, colour temperature...
- Check if correct "Display Option" code is programmed .
- Verify "Option Codes" according sticker inside the set .
- Default settings for White drive ...see Service Manual
Final check of all menus in CSM. Special attention for HDMI Keys.
END
Q52xE SSB Board swap – v3
VDS/JA Updated 17-10-2008
H_16771_007.eps
171008

Figure 5-14 SSB replacement flowchart

5.9 Software Upgrading

5.9.1 Introduction

The set software and security keys are stored in a NAND-Flash, which is connected to the PNX8541 via the PCI bus.

It is possible **for the user** to upgrade the **main** software via the USB port. This allows replacement of a software image in a stand alone set, without the need of an E-JTAG debugger. A description on how to upgrade the main software can be found in the DFU.

Important: When the NAND-Flash must be replaced, a new SSB must be ordered, due to the presence of the security keys! (copy protection keys, MAC address, ...). It is however also possible to replace the NAND-Flash with a good one from a scrap-board.
Perform the following actions after SSB replacement:
1. Set the correct option codes (see sticker inside the TV).
2. Update the TV software (see the DFU for instructions).
3. Perform the alignments as described in chapter 8 (section "Reset of Repaired SSB").
4. Check in CSM if the HDMI keys are valid.

For the correct order number of a new SSB, always refer to the Spare Parts list!

5.9.2 Main Software Upgrade

- The "UpgradeAll.upg" file is only used in the factory.
- The "FlashUtils.upg" file is only used by service centra which are allowed to do component level repair on the SSB.

Automatic Software Upgrade
In "normal" conditions, so when there is no major problem with the TV, the main software and the default software upgrade application can be upgraded with the "AUTORUN.UPG" (FUS part of the one-zip file: e.g. 3104 337 04731 _FUS _Q591E_ 1.25.5.0_commercial.zip). This can also be done by the consumers themselves, but they will have to get their software from the commercial Philips website or via the Software Update Assistant in the user menu (see DFU). The "autorun.upg" file must be placed in the root of the USB stick.
How to upgrade:
1. Copy "AUTORUN.UPG" to the root of the USB stick.
2. Insert USB stick in the set while the set is in ON MODE. The set will restart and the upgrading will start automatically. As soon as the programming is finished, a message is shown to remove the USB stick and restart the set.

Manual Software Upgrade
In case that the software upgrade application does not start automatically, it can also be started manually.
How to start the software upgrade application manually:
1. Disconnect the TV from the Mains/AC Power.
2. Press the "OK" button on a Philips TV remote control or a Philips DVD RC-6 remote control (it is also possible to use a TV remote in "DVD" mode). Keep the "OK" button pressed while reconnecting the TV to the Mains/AC Power.
3. The software upgrade application will start.

Attention!
In case the download application has been started **manually**, the "autorun.upg" will maybe not be recognized.
What to do in this case:
1. Create a directory "UPGRADES" on the USB stick.
2. Rename the "autorun.upg" to something else, e.g. to "software.upg". Do not use long or complicated names, keep it simple. Make sure that "AUTORUN.UPG" is no longer present in the root of the USB stick.
3. Copy the renamed "upg" file into this directory.
4. Insert USB stick into the TV.
5. The renamed "upg" file will be visible and selectable in the upgrade application.

Back-up Software Upgrade Application
If the default software upgrade application does not start (could be due to a corrupted boot 2 sector) via the above described method, try activating the "back-up software upgrade application".
How to start the "back-up software upgrade application" manually:
1. Disconnect the TV from the Mains/AC Power.
2. Press the "INFO"-button on a Philips remote control or "CURSOR DOWN" button on a Philips DVD RC-6 remote control (it is also possible to use a TV remote in "DVD" mode). Keep the "INFO"-button (or "cursor down" button) pressed while reconnecting the TV to the Mains/AC Power.
3. The software upgrade application will start.

5.9.3 Stand-by Software Upgrade via USB

In this chassis it is possible to upgrade the Stand-by software via a USB stick. The method is similar to upgrading the main software via USB.
Use the following steps:
1. Create a directory "UPGRADES" on the USB stick.
2. Copy the Stand-by software (part of the one-zip file, e.g. StandbySW_CFT55_35.0.0.0.upg) into this directory.
3. Insert the USB stick into the TV.
4. Start the download application manually (see section " Manual Software Upgrade".
5. Select the appropriate file and press the "red" button to upgrade.

5.9.4 Content and Usage of the One-Zip Software File

Below the content of the One-Zip file is explained, and instructions on how and when to use it.

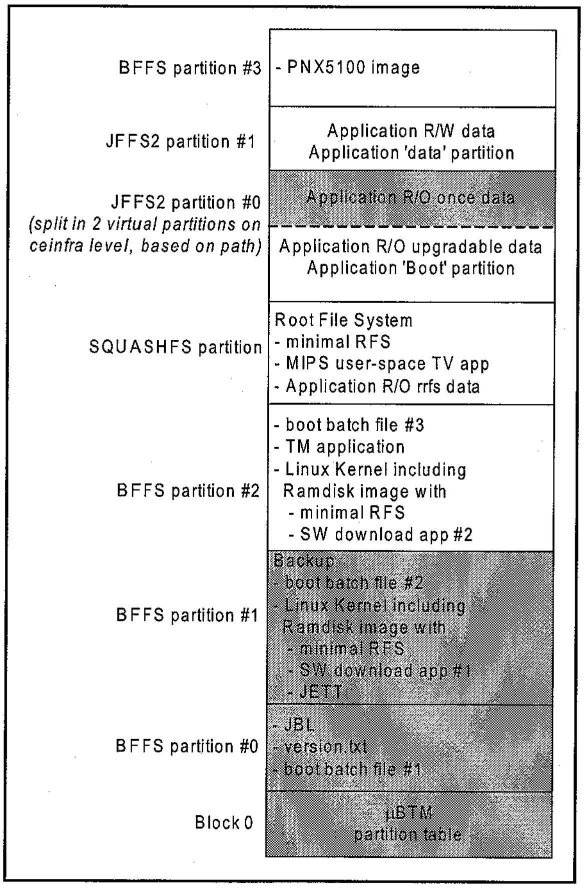
- **1.1 Ambilight_PRFAM_x.x.x.x.zip.** Not to be used for Q529.1E LC sets.
- **1.2 bootProm_PNX5100_Q591X_x.x.x.x.zip.** A programmed device can be ordered via the regional Service organization.
- **1.3 Cabinet_ACOUS_x.x.x.x.zip**. Not to be used by Service technicians.
- **1.4 Ceisp2padll_P2PAD_x.x.x.x.zip.** Not to be used by Service technicians. For ComPair development only.
- **1.5 DDC_Q591X_x.x.x.x.zip.** Contains the content of the VGA NVM. See ComPair for further instruction.
- **1.6 Display_DISPT_x.x.x.x.zip**. Not to be used by Service technicians.
- **1.7 EDID_Q591X_x.x.x.x.zip.** Contains the EDID content of the different EDID NVM's. See ComPair for further instructions.
  For sets with four HDMI connectors.
  - For **HDMI 1** NVM, use "*port 1*.bin"
  - For **HDMI 2** NVM, use "*port 2*.bin"
  - For **HDMI 3** NVM, use "*port 3*.bin"
- **1.8 EJTAGDownload_Q591X_x.x.x.x.zip.** Only used by service centra which are allowed to do component level repair.
- **1.9 Factory_Q591X_x.x.x.x_commercial.zip.** Only for production purposes, not to be used by Service technicians.
- **2.0 FlashUtils_Q591X_x.x.x.x_commercial.zip.** Not to be used by Service technicians.
- **2.1 LightGuide_TV522_x.x.x.x_.zip.** Not to be used by Service Technicians.
- **2.2 FUS_Q591X_x.x.x.x_commercial.zip.** Contains the "autorun.upg" which is needed to upgrade the TV main software and the software download application.
- **2.3 MOP_RXSXX_x.x.x.x.zip.** Not to be used for Q529.1E LC sets.

- **2.4 OAD_Q591X_x.x.x.x.zip.** Not to be used by Service Technicians.
- **2.5OpenSourceFile_Q591X_x.x.x.x.zip.** Not to be used by Service technicians.
- **2.6 PQPrivate_U5228_x.x.x.x.zip.** Not to be used by Service technicians.
- **2.7 PQPublic_U5228_x.x.x.x.zip.** Not to be used by Service technicians.
- **2.8 ProcessNVM_Q591X_x.x.x.x.zip.** Default NVM content. Must be programmed via ComPair.
- **2.9 StandbySW_CFTxx_x.x.x.x_commercial.zip.** Contains the Stand-by software in "upg" and "hex" format.
  - The "StandbySW_xxxxx_prod.upg" file can be used to upgrade the Stand-by software via USB.
  - The "StandbySW_xxxxx.hex" file can be used to upgrade the Stand-by software via ComPair.
  - The files "StandbySW_xxxxx_exhex.hex" and "StandbySW_xxxxx_dev.upg" may not be used by Service technicians (only for development purposes).
- **3.0 stmp4_xxxx.xxxx.xxxx.zip.** This is a separate MPEG4 SW (is also part of the FUS autorun.upg). Not to be used by Service Technicians.
- **3.1 UpgradeAll_Q591X_x.x.x.x_commercial.zip.** Only for production purposes, not to be used by Service technicians.
  Caution: Never try to use this file, because it will overwrite the HDCP keys ! ! !
- **3.2 UpgradeExe_Q591X_x.x.x.x.zip.** Not to be used by Service Technicians.

5.9.5 Explanation UART log

How to log and change settings: see section 5.8.5 Logging.

What's inside the flash of a TV set


BFFS partition #3
- PNX5100 image
JFFS2 partition #1
Application R/W data
Application 'data' partition
JFFS2 partition #0
(split in 2 virtual partitions on ceinfra level, based on path)
Application R/O once data
Application R/O upgradable data
Application 'Boot' partition
SQUASHFS partition
Root File System
- minimal RFS
- MIPS user-space TV app
- Application R/O rrfs data
BFFS partition #2
- boot batch file #3
- TM application
- Linux Kernel including Ramdisk image with
- minimal RFS
- SW download app #2
BFFS partition #1
Backup
- boot batch file #2
- Linux Kernel including Ramdisk image with
- minimal RFS
- SW download app #1
- JETT
BFFS partition #0
- JBL
- version.txt
- boot batch file #1
Block 0
µBTM
partition table

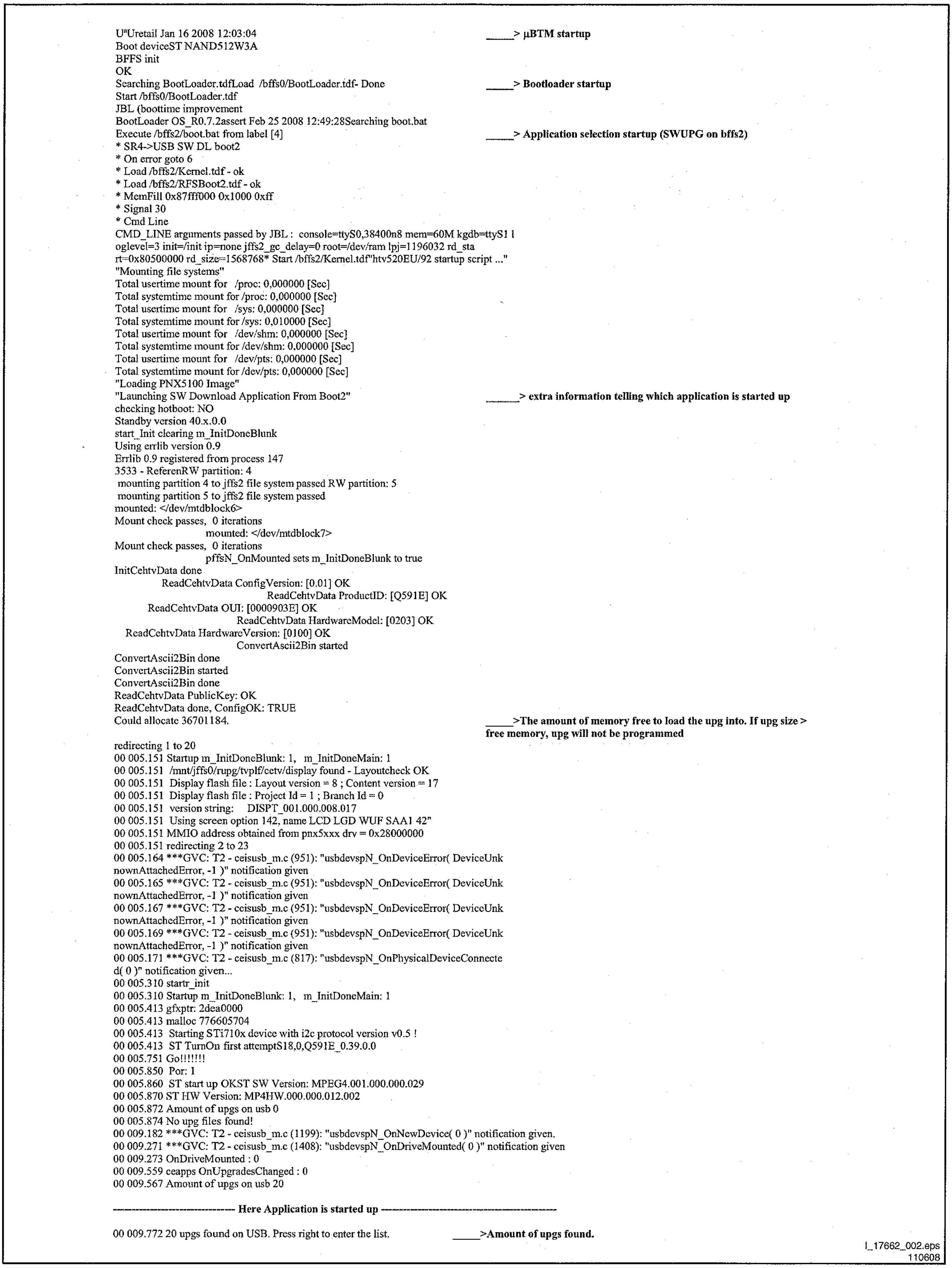
I_17662_001.eps
110608

Figure 5-15 Sections in a flash device

Explanation of the sections
The flash of TV520 sets consists of a boot-block (block 0), a number of BFFS (Boot Flash File System) partitions, one SquashFS (compressed read-only filesystem for Linux. SquashFS is intended for general read-only filesystem use, for archival use) partition and a number of JFFS (Journaling Flash File System) partitions. The BFFS partitions contain the program code and compile-time data. The SquashFS partition contains the Linux rootfs including the standard RFS (Root File System) directory structures (dev,lib, modules, ...) and MIPS executables (elf).
For the purpose of SWUPG (SoftWare UPGrade application) the following points are important:

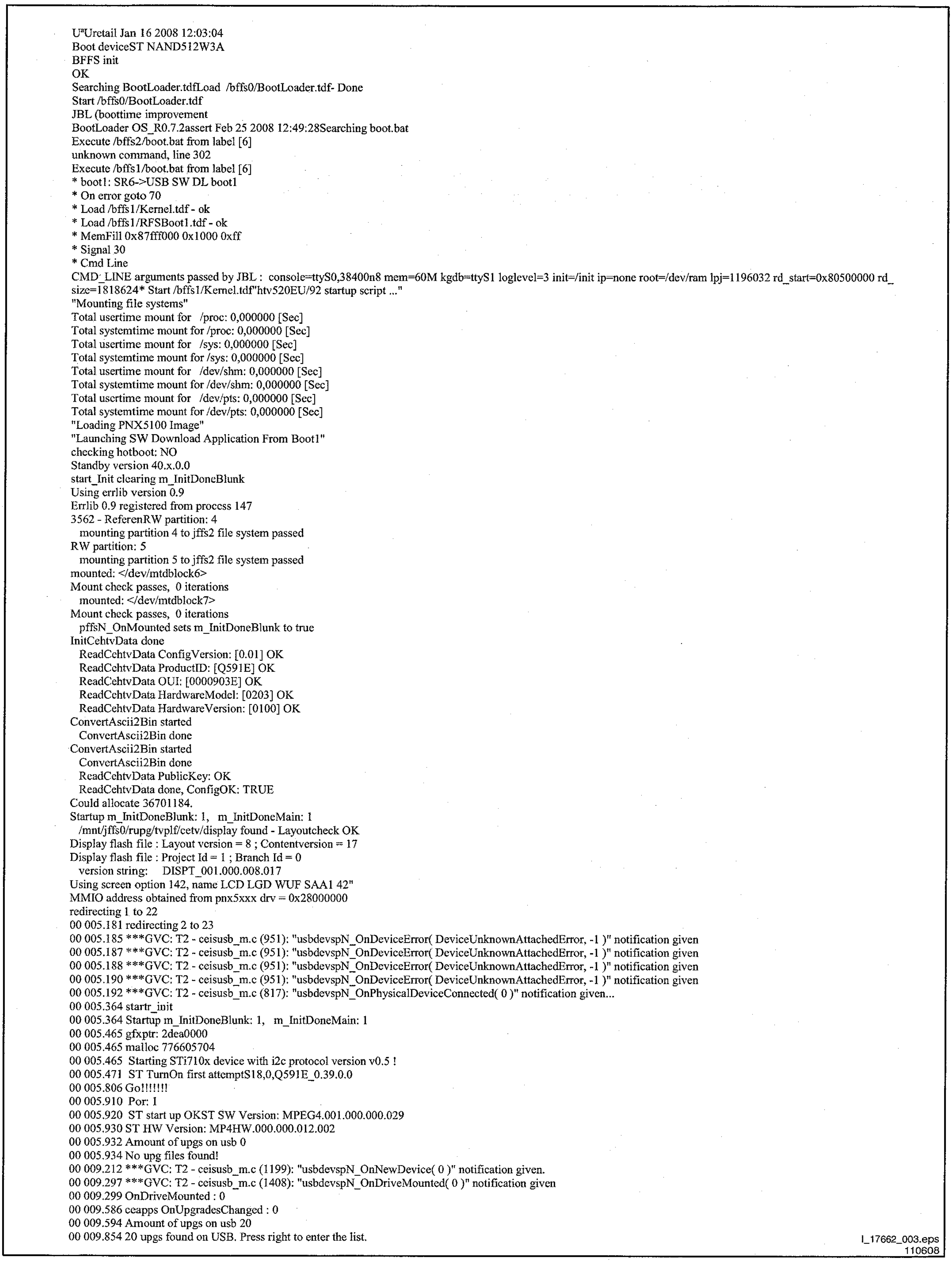
- The boot-block (block 0) contains also the partition table. This table indicates which partitions there are on this system and where they are located on the flash. All programs that want to access the flash contents should use this table.
- At system start-up the BTM (Boot Manager) loads the JBL (Jaguar Boot Loader) from /bffs0. The JBL then starts interpreting the boot.bat file from the highest available BFFS partition. If no boot.bat is found there, the next lower partition is tried.
- /bffs1 partition contains:
  1. kernel image.
  2. ramdisk image of RFS holding bare minimum (no debug tooling), including mod/libs , the SW backup upgrade executable, the Jett executable and the helper executable (init + MTD utils used to flash).
  3. boot batch file.
- The backup SWUPG is stored in the /boot1 BFFS partition in the factory, together with a boot.bat that by defaults loads this SWUPG. This way the set will always load this SWUPG if nothing is in /bffs2.
- /bffs2 partition contains:
  1. kernel image.
  2. ramdisk image of RFS holding bare minimum (no debug tooling), including mod/libs , the SW backup upgrade executable and the helper executable (init + MTD utils used to flash).
  3. TM image.
  4. boot batch file.
- In /boot2 an additional SWUPG shall always be written, either in the factory or by the end-user through an upgrade, which will overrule the one in /boot1. Here also the TM image is stored and a boot.bat which by default loads the main TV application, but falls back on the /boot2/SWUPG if that fails.
- /bffs3 partition contains PNX5100 images.
- In SquashFS, the TV application RFS flashed as a partition image. Content identical to the RAMDISK RFS at the exception that it includes the TV application in stead of SWUPG.
- JFFS2 partition0 contains the R/O once data, which can only written be written in the factory.
- JFFS2 partition1 contains the R/W data.

Startup sequence TV
The UART doesn't show the standby output.



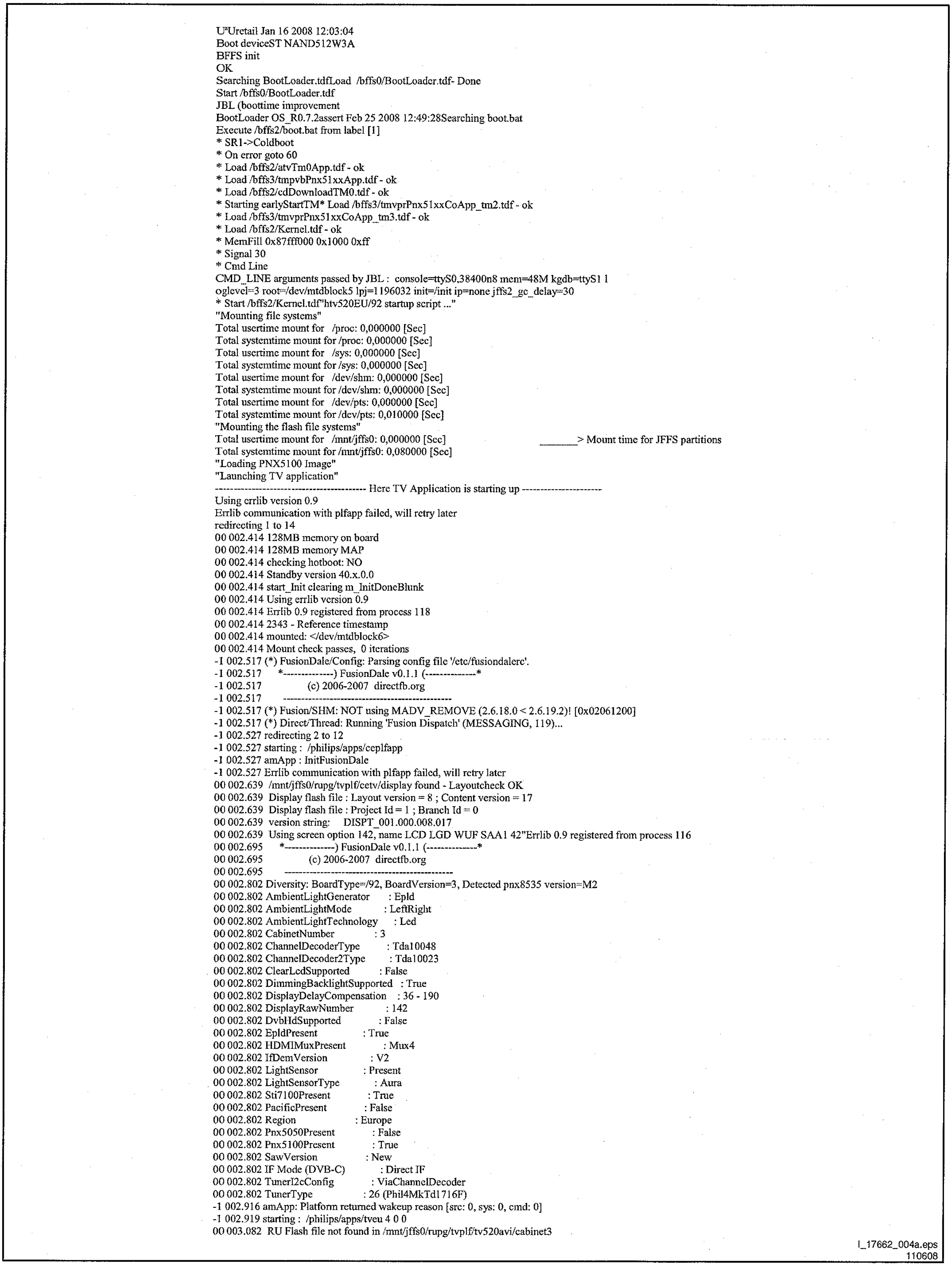
```
UªUretail Jan 16 2008 12:03:04                                        _____> µBTM startup
Boot deviceST NAND512W3A
BFFS init
OK
Searching BootLoader.tdfLoad  /bffs0/BootLoader.tdf- Done             _____> Bootloader startup
Start /bffs0/BootLoader.tdf
JBL (boottime improvement
BootLoader OS_R0.7.2assert Feb 25 2008 12:49:28Searching boot.bat
Execute /bffs2/boot.bat from label [4]                                _____> Application selection startup (SWUPG on bffs2)
* SR4->USB SW DL boot2
* On error goto 6
* Load /bffs2/Kernel.tdf - ok
* Load /bffs2/RFSBoot2.tdf - ok
* MemFill 0x87fff000 0x1000 0xff
* Signal 30
* Cmd Line
CMD_LINE arguments passed by JBL :  console=ttyS0,38400n8 mem=60M kgdb=ttyS1 l
oglevel=3 init=/init ip=none jffs2_gc_delay=0 root=/dev/ram lpj=1196032 rd_sta
rt=0x80500000 rd_size=1568768* Start /bffs2/Kernel.tdf"htv520EU/92 startup script ..."
"Mounting file systems"
Total usertime mount for   /proc: 0,000000 [Sec]
Total systemtime mount for /proc: 0,000000 [Sec]
Total usertime mount for   /sys: 0,000000 [Sec]
Total systemtime mount for /sys: 0,010000 [Sec]
Total usertime mount for   /dev/shm: 0,000000 [Sec]
Total systemtime mount for /dev/shm: 0,000000 [Sec]
Total usertime mount for   /dev/pts: 0,000000 [Sec]
Total systemtime mount for /dev/pts: 0,000000 [Sec]
"Loading PNX5100 Image"
"Launching SW Download Application From Boot2"                        ______> extra information telling which application is started up
checking hotboot: NO
Standby version 40.x.0.0
start_Init clearing m_InitDoneBlunk
Using errlib version 0.9
Errlib 0.9 registered from process 147
3533 - ReferenRW partition: 4
 mounting partition 4 to jffs2 file system passed RW partition: 5
 mounting partition 5 to jffs2 file system passed
mounted: </dev/mtdblock6>
Mount check passes,  0 iterations
                     mounted: </dev/mtdblock7>
Mount check passes,  0 iterations
                     pffsN_OnMounted sets m_InitDoneBlunk to true
InitCehtvData done
           ReadCehtvData ConfigVersion: [0.01] OK
                                   ReadCehtvData ProductID: [Q591E] OK
        ReadCehtvData OUI: [0000903E] OK
                            ReadCehtvData HardwareModel: [0203] OK
   ReadCehtvData HardwareVersion: [0100] OK
                            ConvertAscii2Bin started
ConvertAscii2Bin done
ConvertAscii2Bin started
ConvertAscii2Bin done
ReadCehtvData PublicKey: OK
ReadCehtvData done, ConfigOK: TRUE
Could allocate 36701184.                                              _____>The amount of memory free to load the upg into. If upg size >
                                                                      free memory, upg will not be programmed
redirecting 1 to 20
00 005.151 Startup m_InitDoneBlunk: 1,   m_InitDoneMain: 1
00 005.151  /mnt/jffs0/rupg/tvplf/cetv/display found - Layoutcheck OK
00 005.151  Display flash file : Layout version = 8 ; Content version = 17
00 005.151  Display flash file : Project Id = 1 ; Branch Id = 0
00 005.151  version string:     DISPT_001.000.008.017
00 005.151  Using screen option 142, name LCD LGD WUF SAA1 42"
00 005.151 MMIO address obtained from pnx5xxx drv = 0x28000000
00 005.151 redirecting 2 to 23
00 005.164 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnk
nownAttachedError, -1 )" notification given
00 005.165 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnk
nownAttachedError, -1 )" notification given
00 005.167 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnk
nownAttachedError, -1 )" notification given
00 005.169 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnk
nownAttachedError, -1 )" notification given
00 005.171 ***GVC: T2 - ceisusb_m.c (817): "usbdevspN_OnPhysicalDeviceConnecte
d( 0 )" notification given...
00 005.310 startr_init
00 005.310 Startup m_InitDoneBlunk: 1,   m_InitDoneMain: 1
00 005.413 gfxptr: 2dea0000
00 005.413 malloc 776605704
00 005.413  Starting STi710x device with i2c protocol version v0.5 !
00 005.413  ST TurnOn first attemptS18,0,Q591E_0.39.0.0
00 005.751 Go!!!!!!!
00 005.850  Por: 1
00 005.860  ST start up OKST SW Version: MPEG4.001.000.000.029
00 005.870 ST HW Version: MP4HW.000.000.012.002
00 005.872 Amount of upgs on usb 0
00 005.874 No upg files found!
00 009.182 ***GVC: T2 - ceisusb_m.c (1199): "usbdevspN_OnNewDevice( 0 )" notification given.
00 009.271 ***GVC: T2 - ceisusb_m.c (1408): "usbdevspN_OnDriveMounted( 0 )" notification given
00 009.273 OnDriveMounted : 0
00 009.559 ceapps OnUpgradesChanged : 0
00 009.567 Amount of upgs on usb 20

------------------------------ Here Application is started up ----------------------------------------

00 009.772 20 upgs found on USB. Press right to enter the list.       _____>Amount of upgs found.
```

Figure 5-16 Example UART log during SWUPG startup (DVD OK).



```
UªUretail Jan 16 2008 12:03:04
Boot deviceST NAND512W3A
BFFS init
OK
Searching BootLoader.tdfLoad  /bffs0/BootLoader.tdf- Done
Start /bffs0/BootLoader.tdf
JBL (boottime improvement
BootLoader OS_R0.7.2assert Feb 25 2008 12:49:28Searching boot.bat
Execute /bffs2/boot.bat from label [6]
unknown command, line 302
Execute /bffs1/boot.bat from label [6]
* boot1: SR6->USB SW DL boot1
* On error goto 70
* Load /bffs1/Kernel.tdf - ok
* Load /bffs1/RFSBoot1.tdf - ok
* MemFill 0x87fff000 0x1000 0xff
* Signal 30
* Cmd Line
CMD_LINE arguments passed by JBL :  console=ttyS0,38400n8 mem=60M kgdb=ttyS1 loglevel=3 init=/init ip=none root=/dev/ram lpj=1196032 rd_start=0x80500000 rd_
size=1818624* Start /bffs1/Kernel.tdf"htv520EU/92 startup script ..."
"Mounting file systems"
Total usertime mount for   /proc: 0,000000 [Sec]
Total systemtime mount for /proc: 0,000000 [Sec]
Total usertime mount for   /sys: 0,000000 [Sec]
Total systemtime mount for /sys: 0,000000 [Sec]
Total usertime mount for   /dev/shm: 0,000000 [Sec]
Total systemtime mount for /dev/shm: 0,000000 [Sec]
Total usertime mount for   /dev/pts: 0,000000 [Sec]
Total systemtime mount for /dev/pts: 0,000000 [Sec]
"Loading PNX5100 Image"
"Launching SW Download Application From Boot1"
checking hotboot: NO
Standby version 40.x.0.0
start_Init clearing m_InitDoneBlunk
Using errlib version 0.9
Errlib 0.9 registered from process 147
3562 - ReferenRW partition: 4
  mounting partition 4 to jffs2 file system passed
RW partition: 5
  mounting partition 5 to jffs2 file system passed
mounted: </dev/mtdblock6>
Mount check passes,  0 iterations
  mounted: </dev/mtdblock7>
Mount check passes,  0 iterations
  pffsN_OnMounted sets m_InitDoneBlunk to true
InitCehtvData done
  ReadCehtvData ConfigVersion: [0.01] OK
  ReadCehtvData ProductID: [Q591E] OK
  ReadCehtvData OUI: [0000903E] OK
  ReadCehtvData HardwareModel: [0203] OK
  ReadCehtvData HardwareVersion: [0100] OK
ConvertAscii2Bin started
  ConvertAscii2Bin done
ConvertAscii2Bin started
  ConvertAscii2Bin done
  ReadCehtvData PublicKey: OK
  ReadCehtvData done, ConfigOK: TRUE
Could allocate 36701184.
Startup m_InitDoneBlunk: 1,   m_InitDoneMain: 1
  /mnt/jffs0/rupg/tvplf/cetv/display found - Layoutcheck OK
Display flash file : Layout version = 8 ; Contentversion = 17
Display flash file : Project Id = 1 ; Branch Id = 0
  version string:    DISPT_001.000.008.017
Using screen option 142, name LCD LGD WUF SAA1 42"
MMIO address obtained from pnx5xxx drv = 0x28000000
redirecting 1 to 22
00 005.181 redirecting 2 to 23
00 005.185 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 005.187 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 005.188 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 005.190 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 005.192 ***GVC: T2 - ceisusb_m.c (817): "usbdevspN_OnPhysicalDeviceConnected( 0 )" notification given...
00 005.364 startr_init
00 005.364 Startup m_InitDoneBlunk: 1,   m_InitDoneMain: 1
00 005.465 gfxptr: 2dea0000
00 005.465 malloc 776605704
00 005.465  Starting STi710x device with i2c protocol version v0.5 !
00 005.471  ST TurnOn first attemptS18,0,Q591E_0.39.0.0
00 005.806 Go!!!!!!!
00 005.910  Por: 1
00 005.920  ST start up OKST SW Version: MPEG4.001.000.000.029
00 005.930 ST HW Version: MP4HW.000.000.012.002
00 005.932 Amount of upgs on usb 0
00 005.934 No upg files found!
00 009.212 ***GVC: T2 - ceisusb_m.c (1199): "usbdevspN_OnNewDevice( 0 )" notification given.
00 009.297 ***GVC: T2 - ceisusb_m.c (1408): "usbdevspN_OnDriveMounted( 0 )" notification given
00 009.299 OnDriveMounted : 0
00 009.586 ceapps OnUpgradesChanged : 0
00 009.594 Amount of upgs on usb 20
00 009.854 20 upgs found on USB. Press right to enter the list.
```

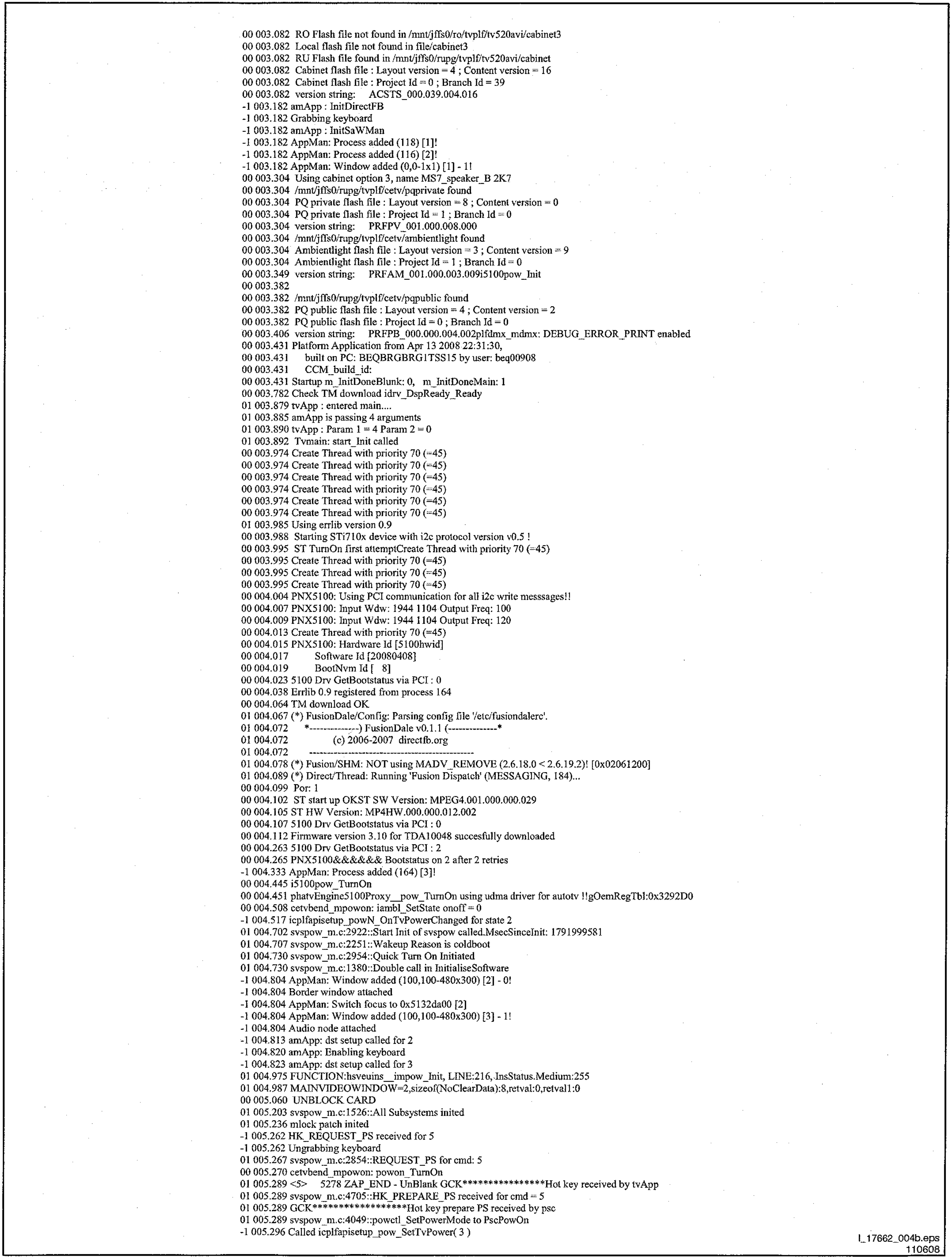
Figure 5-17 Example UART log during SWUPG startup (DVD down).



```
UªUretail Jan 16 2008 12:03:04
Boot deviceST NAND512W3A
BFFS init
OK
Searching BootLoader.tdfLoad  /bffs0/BootLoader.tdf- Done
Start /bffs0/BootLoader.tdf
JBL (boottime improvement
BootLoader OS_R0.7.2assert Feb 25 2008 12:49:28Searching boot.bat
Execute /bffs2/boot.bat from label [1]
* SR1->Coldboot
* On error goto 60
* Load /bffs2/atvTm0App.tdf - ok
* Load /bffs3/tmpvbPnx51xxApp.tdf - ok
* Load /bffs2/cdDownloadTM0.tdf - ok
* Starting earlyStartTM* Load /bffs3/tmvprPnx51xxCoApp_tm2.tdf - ok
* Load /bffs3/tmvprPnx51xxCoApp_tm3.tdf - ok
* Load /bffs2/Kernel.tdf - ok
* MemFill 0x87fff000 0x1000 0xff
* Signal 30
* Cmd Line
CMD_LINE arguments passed by JBL :  console=ttyS0,38400n8 mem=48M kgdb=ttyS1 l
oglevel=3 root=/dev/mtdblock5 lpj=1196032 init=/init ip=none jffs2_gc_delay=30
* Start /bffs2/Kernel.tdf"htv520EU/92 startup script ..."
"Mounting file systems"
Total usertime mount for   /proc: 0,000000 [Sec]
Total systemtime mount for /proc: 0,000000 [Sec]
Total usertime mount for   /sys: 0,000000 [Sec]
Total systemtime mount for /sys: 0,000000 [Sec]
Total usertime mount for   /dev/shm: 0,000000 [Sec]
Total systemtime mount for /dev/shm: 0,000000 [Sec]
Total usertime mount for   /dev/pts: 0,000000 [Sec]
Total systemtime mount for /dev/pts: 0,010000 [Sec]
"Mounting the flash file systems"
Total usertime mount for   /mnt/jffs0: 0,000000 [Sec]                  _______> Mount time for JFFS partitions
Total systemtime mount for /mnt/jffs0: 0,080000 [Sec]
"Loading PNX5100 Image"
"Launching TV application"
----------------------------------------- Here TV Application is starting up ---------------------
Using errlib version 0.9
Errlib communication with plfapp failed, will retry later
redirecting 1 to 14
00 002.414 128MB memory on board
00 002.414 128MB memory MAP
00 002.414 checking hotboot: NO
00 002.414 Standby version 40.x.0.0
00 002.414 start_Init clearing m_InitDoneBlunk
00 002.414 Using errlib version 0.9
00 002.414 Errlib 0.9 registered from process 118
00 002.414 2343 - Reference timestamp
00 002.414 mounted: </dev/mtdblock6>
00 002.414 Mount check passes,  0 iterations
-1 002.517 (*) FusionDale/Config: Parsing config file '/etc/fusiondalerc'.
-1 002.517     *--------------) FusionDale v0.1.1 (--------------*
-1 002.517            (c) 2006-2007  directfb.org
-1 002.517      --------------------------------------------
-1 002.517 (*) Fusion/SHM: NOT using MADV_REMOVE (2.6.18.0 < 2.6.19.2)! [0x02061200]
-1 002.517 (*) Direct/Thread: Running 'Fusion Dispatch' (MESSAGING, 119)...
-1 002.527 redirecting 2 to 12
-1 002.527 starting :  /philips/apps/ceplfapp
-1 002.527 amApp : InitFusionDale
-1 002.527 Errlib communication with plfapp failed, will retry later
00 002.639  /mnt/jffs0/rupg/tvplf/cetv/display found - Layoutcheck OK
00 002.639  Display flash file : Layout version = 8 ; Content version = 17
00 002.639  Display flash file : Project Id = 1 ; Branch Id = 0
00 002.639  version string:    DISPT_001.000.008.017
00 002.639  Using screen option 142, name LCD LGD WUF SAA1 42"Errlib 0.9 registered from process 116
00 002.695     *--------------) FusionDale v0.1.1 (--------------*
00 002.695            (c) 2006-2007  directfb.org
00 002.695      --------------------------------------------
00 002.802 Diversity: BoardType=/92, BoardVersion=3, Detected pnx8535 version=M2
00 002.802 AmbientLightGenerator      : Epld
00 002.802 AmbientLightMode           : LeftRight
00 002.802 AmbientLightTechnology     : Led
00 002.802 CabinetNumber              : 3
00 002.802 ChannelDecoderType         : Tda10048
00 002.802 ChannelDecoder2Type        : Tda10023
00 002.802 ClearLcdSupported          : False
00 002.802 DimmingBacklightSupported  : True
00 002.802 DisplayDelayCompensation   : 36 - 190
00 002.802 DisplayRawNumber           : 142
00 002.802 DvbHdSupported             : False
00 002.802 EpldPresent                : True
00 002.802 HDMIMuxPresent             : Mux4
00 002.802 IfDemVersion               : V2
00 002.802 LightSensor                : Present
00 002.802 LightSensorType            : Aura
00 002.802 Sti7100Present             : True
00 002.802 PacificPresent             : False
00 002.802 Region                     : Europe
00 002.802 Pnx5050Present             : False
00 002.802 Pnx5100Present             : True
00 002.802 SawVersion                 : New
00 002.802 IF Mode (DVB-C)            : Direct IF
00 002.802 TunerI2cConfig             : ViaChannelDecoder
00 002.802 TunerType                  : 26 (Phil4MkTd1716F)
-1 002.916 amApp: Platform returned wakeup reason [src: 0, sys: 0, cmd: 0]
-1 002.919 starting :  /philips/apps/tveu 4 0 0
00 003.082  RU Flash file not found in /mnt/jffs0/rupg/tvplf/tv520avi/cabinet3
```

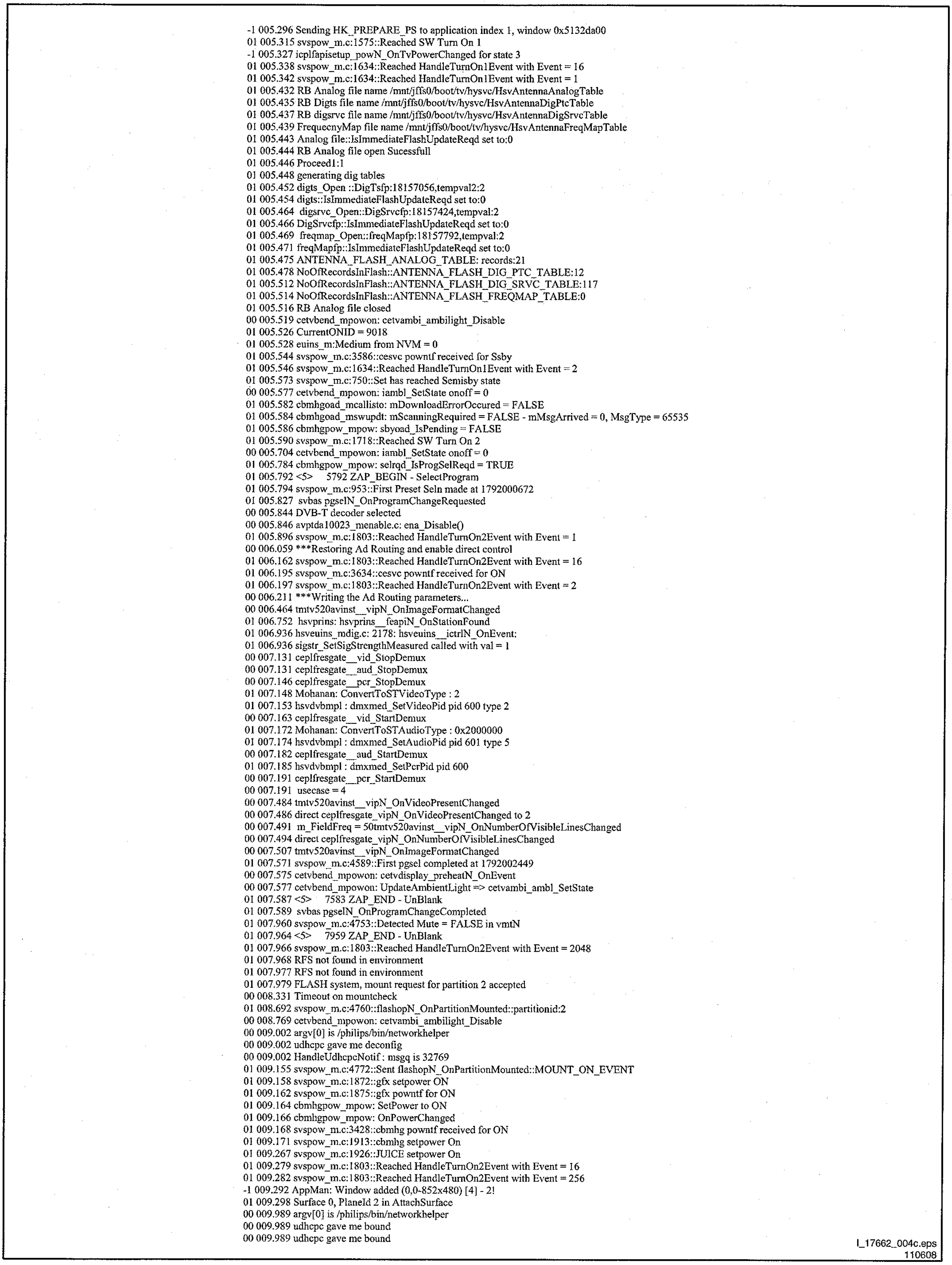
I_17662_004a.eps
110608

Figure 5-18 Example UART log during SWUPG startup (Normal startup) part 1.



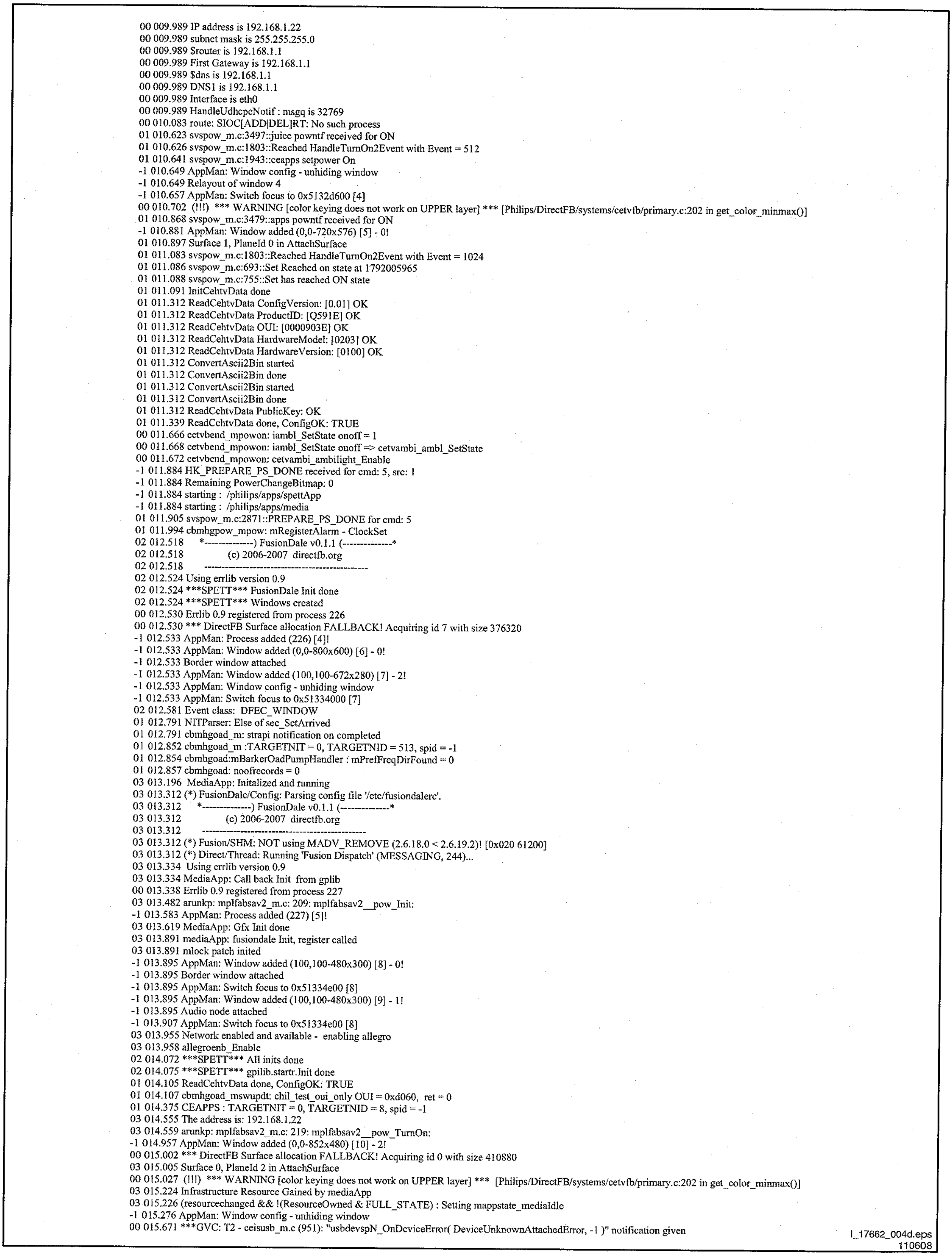
```
00 003.082  RO Flash file not found in /mnt/jffs0/ro/tvplf/tv520avi/cabinet3
00 003.082  Local flash file not found in file/cabinet3
00 003.082  RU Flash file found in /mnt/jffs0/rupg/tvplf/tv520avi/cabinet
00 003.082  Cabinet flash file : Layout version = 4 ; Content version = 16
00 003.082  Cabinet flash file : Project Id = 0 ; Branch Id = 39
00 003.082  version string:     ACSTS_000.039.004.016
-1 003.182 amApp : InitDirectFB
-1 003.182 Grabbing keyboard
-1 003.182 amApp : InitSaWMan
-1 003.182 AppMan: Process added (118) [1]!
-1 003.182 AppMan: Process added (116) [2]!
-1 003.182 AppMan: Window added (0,0-1x1) [1] - 1!
00 003.304  Using cabinet option 3, name MS7_speaker_B 2K7
00 003.304  /mnt/jffs0/rupg/tvplf/cetv/pqprivate found
00 003.304  PQ private flash file : Layout version = 8 ; Content version = 0
00 003.304  PQ private flash file : Project Id = 1 ; Branch Id = 0
00 003.304  version string:     PRFPV_001.000.008.000
00 003.304  /mnt/jffs0/rupg/tvplf/cetv/ambientlight found
00 003.304  Ambientlight flash file : Layout version = 3 ; Content version = 9
00 003.304  Ambientlight flash file : Project Id = 1 ; Branch Id = 0
00 003.349  version string:     PRFAM_001.000.003.009i5100pow_Init
00 003.382
00 003.382  /mnt/jffs0/rupg/tvplf/cetv/pqpublic found
00 003.382  PQ public flash file : Layout version = 4 ; Content version = 2
00 003.382  PQ public flash file : Project Id = 0 ; Branch Id = 0
00 003.406  version string:     PRFPB_000.000.004.002plfdmx_mdmx: DEBUG_ERROR_PRINT enabled
00 003.431 Platform Application from Apr 13 2008 22:31:30,
00 003.431     built on PC: BEQBRGBRG1TSS15 by user: beq00908
00 003.431     CCM_build_id:
00 003.431 Startup m_InitDoneBlunk: 0,   m_InitDoneMain: 1
00 003.782 Check TM download idrv_DspReady_Ready
01 003.879 tvApp : entered main....
01 003.885 amApp is passing 4 arguments
01 003.890 tvApp : Param 1 = 4 Param 2 = 0
01 003.892  Tvmain: start_Init called
00 003.974 Create Thread with priority 70 (=45)
00 003.974 Create Thread with priority 70 (=45)
00 003.974 Create Thread with priority 70 (=45)
00 003.974 Create Thread with priority 70 (=45)
00 003.974 Create Thread with priority 70 (=45)
00 003.974 Create Thread with priority 70 (=45)
01 003.985 Using errlib version 0.9
00 003.988  Starting STi710x device with i2c protocol version v0.5 !
00 003.995  ST TurnOn first attemptCreate Thread with priority 70 (=45)
00 003.995 Create Thread with priority 70 (=45)
00 003.995 Create Thread with priority 70 (=45)
00 003.995 Create Thread with priority 70 (=45)
00 004.004 PNX5100: Using PCI communication for all i2c write messsages!!
00 004.007 PNX5100: Input Wdw: 1944 1104 Output Freq: 100
00 004.009 PNX5100: Input Wdw: 1944 1104 Output Freq: 120
00 004.013 Create Thread with priority 70 (=45)
00 004.015 PNX5100: Hardware Id [5100hwid]
00 004.017         Software Id [20080408]
00 004.019         BootNvm Id [   8]
00 004.023 5100 Drv GetBootstatus via PCI : 0
00 004.038 Errlib 0.9 registered from process 164
00 004.064 TM download OK
01 004.067 (*) FusionDale/Config: Parsing config file '/etc/fusiondalerc'.
01 004.072     *--------------) FusionDale v0.1.1 (--------------*
01 004.072            (c) 2006-2007  directfb.org
01 004.072     ------------------------------------------------
01 004.078 (*) Fusion/SHM: NOT using MADV_REMOVE (2.6.18.0 < 2.6.19.2)! [0x02061200]
01 004.089 (*) Direct/Thread: Running 'Fusion Dispatch' (MESSAGING, 184)...
00 004.099  Por: 1
00 004.102  ST start up OKST SW Version: MPEG4.001.000.000.029
00 004.105 ST HW Version: MP4HW.000.000.012.002
00 004.107 5100 Drv GetBootstatus via PCI : 0
00 004.112 Firmware version 3.10 for TDA10048 succesfully downloaded
00 004.263 5100 Drv GetBootstatus via PCI : 2
00 004.265 PNX5100&&&&&& Bootstatus on 2 after 2 retries
-1 004.333 AppMan: Process added (164) [3]!
00 004.445 i5100pow_TurnOn
00 004.451 phatvEngine5100Proxy__pow_TurnOn using udma driver for autotv !!gOemRegTbl:0x3292D0
00 004.508 cetvbend_mpowon: iambl_SetState onoff = 0
-1 004.517 icplfapisetup_powN_OnTvPowerChanged for state 2
01 004.702 svspow_m.c:2922::Start Init of svspow called.MsecSinceInit: 1791999581
01 004.707 svspow_m.c:2251::Wakeup Reason is coldboot
01 004.730 svspow_m.c:2954::Quick Turn On Initiated
01 004.730 svspow_m.c:1380::Double call in InitialiseSoftware
-1 004.804 AppMan: Window added (100,100-480x300) [2] - 0!
-1 004.804 Border window attached
-1 004.804 AppMan: Switch focus to 0x5132da00 [2]
-1 004.804 AppMan: Window added (100,100-480x300) [3] - 1!
-1 004.804 Audio node attached
-1 004.813 amApp: dst setup called for 2
-1 004.820 amApp: Enabling keyboard
-1 004.823 amApp: dst setup called for 3
01 004.975 FUNCTION:hsveuins__impow_Init, LINE:216,.InsStatus.Medium:255
01 004.987 MAINVIDEOWINDOW=2,sizeof(NoClearData):8,retval:0,retval1:0
00 005.060  UNBLOCK CARD
01 005.203 svspow_m.c:1526::All Subsystems inited
01 005.236 mlock patch inited
-1 005.262 HK_REQUEST_PS received for 5
-1 005.262 Ungrabbing keyboard
01 005.267 svspow_m.c:2854::REQUEST_PS for cmd: 5
00 005.270 cetvbend_mpowon: powon_TurnOn
01 005.289 <5>     5278 ZAP_END - UnBlank GCK***************Hot key received by tvApp
01 005.289 svspow_m.c:4705::HK_PREPARE_PS received for cmd = 5
01 005.289 GCK*****************Hot key prepare PS received by psc
01 005.289 svspow_m.c:4049::powctl_SetPowerMode to PscPowOn
-1 005.296 Called icplfapisetup_pow_SetTvPower( 3 )
```

Figure 5-19 Example UART log during SWUPG startup (Normal startup) part 2.



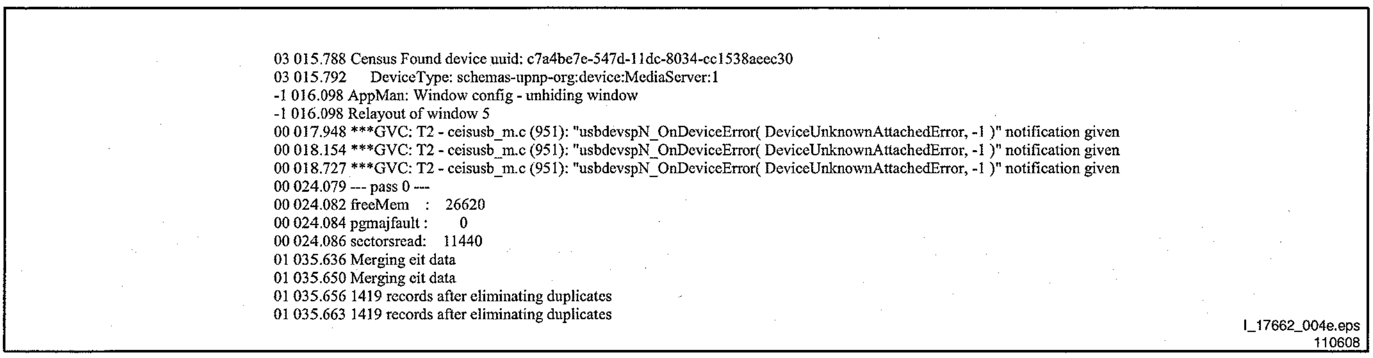
```
-1 005.296 Sending HK_PREPARE_PS to application index 1, window 0x5132da00
01 005.315 svspow_m.c:1575::Reached SW Turn On 1
-1 005.327 icplfapisetup_powN_OnTvPowerChanged for state 3
01 005.338 svspow_m.c:1634::Reached HandleTurnOn1Event with Event = 16
01 005.342 svspow_m.c:1634::Reached HandleTurnOn1Event with Event = 1
01 005.432 RB Analog file name /mnt/jffs0/boot/tv/hysvc/HsvAntennaAnalogTable
01 005.435 RB Digts file name /mnt/jffs0/boot/tv/hysvc/HsvAntennaDigPtcTable
01 005.437 RB digsrvc file name /mnt/jffs0/boot/tv/hysvc/HsvAntennaDigSrvcTable
01 005.439 FrequecnyMap file name /mnt/jffs0/boot/tv/hysvc/HsvAntennaFreqMapTable
01 005.443 Analog file::IsImmediateFlashUpdateReqd set to:0
01 005.444 RB Analog file open Sucessfull
01 005.446 Proceed1:1
01 005.448 generating dig tables
01 005.452 digts_Open ::DigTsfp:18157056,tempval2:2
01 005.454 digts::IsImmediateFlashUpdateReqd set to:0
01 005.464  digsrvc_Open::DigSrvcfp:18157424,tempval:2
01 005.466 DigSrvcfp::IsImmediateFlashUpdateReqd set to:0
01 005.469  freqmap_Open::freqMapfp:18157792,tempval:2
01 005.471 freqMapfp::IsImmediateFlashUpdateReqd set to:0
01 005.475 ANTENNA_FLASH_ANALOG_TABLE: records:21
01 005.478 NoOfRecordsInFlash::ANTENNA_FLASH_DIG_PTC_TABLE:12
01 005.512 NoOfRecordsInFlash::ANTENNA_FLASH_DIG_SRVC_TABLE:117
01 005.514 NoOfRecordsInFlash::ANTENNA_FLASH_FREQMAP_TABLE:0
01 005.516 RB Analog file closed
00 005.519 cetvbend_mpowon: cetvambi_ambilight_Disable
01 005.526 CurrentONID = 9018
01 005.528 euins_m:Medium from NVM = 0
01 005.544 svspow_m.c:3586::cesvc powntf received for Ssby
01 005.546 svspow_m.c:1634::Reached HandleTurnOn1Event with Event = 2
01 005.573 svspow_m.c:750::Set has reached Semisby state
00 005.577 cetvbend_mpowon: iambl_SetState onoff = 0
01 005.582 cbmhgoad_mcallisto: mDownloadErrorOccured = FALSE
01 005.584 cbmhgoad_mswupdt: mScanningRequired = FALSE - mMsgArrived = 0, MsgType = 65535
01 005.586 cbmhgpow_mpow: sbyoad_IsPending = FALSE
01 005.590 svspow_m.c:1718::Reached SW Turn On 2
00 005.704 cetvbend_mpowon: iambl_SetState onoff = 0
01 005.784 cbmhgpow_mpow: selrqd_IsProgSelReqd = TRUE
01 005.792 <5>     5792 ZAP_BEGIN - SelectProgram
01 005.794 svspow_m.c:953::First Preset Seln made at 1792000672
01 005.827  svbas pgselN_OnProgramChangeRequested
00 005.844 DVB-T decoder selected
00 005.846 avptda10023_menable.c: ena_Disable()
01 005.896 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 1
00 006.059 ***Restoring Ad Routing and enable direct control
01 006.162 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 16
01 006.195 svspow_m.c:3634::cesvc powntf received for ON
01 006.197 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 2
00 006.211 ***Writing the Ad Routing parameters...
00 006.464 tmtv520avinst__vipN_OnImageFormatChanged
01 006.752  hsvprins: hsvprins__feapiN_OnStationFound
01 006.936 hsveuins_mdig.c: 2178: hsveuins__ictrlN_OnEvent:
01 006.936 sigstr_SetSigStrengthMeasured called with val = 1
00 007.131 ceplfresgate__vid_StopDemux
00 007.131 ceplfresgate__aud_StopDemux
00 007.146 ceplfresgate__pcr_StopDemux
01 007.148 Mohanan: ConvertToSTVideoType : 2
01 007.153 hsvdvbmpl : dmxmed_SetVideoPid pid 600 type 2
00 007.163 ceplfresgate__vid_StartDemux
01 007.172 Mohanan: ConvertToSTAudioType : 0x2000000
01 007.174 hsvdvbmpl : dmxmed_SetAudioPid pid 601 type 5
00 007.182 ceplfresgate__aud_StartDemux
01 007.185 hsvdvbmpl : dmxmed_SetPcrPid pid 600
00 007.191 ceplfresgate__pcr_StartDemux
00 007.191  usecase = 4
00 007.484 tmtv520avinst__vipN_OnVideoPresentChanged
00 007.486 direct ceplfresgate_vipN_OnVideoPresentChanged to 2
00 007.491  m_FieldFreq = 50tmtv520avinst__vipN_OnNumberOfVisibleLinesChanged
00 007.494 direct ceplfresgate_vipN_OnNumberOfVisibleLinesChanged
00 007.507 tmtv520avinst__vipN_OnImageFormatChanged
01 007.571 svspow_m.c:4589::First pgsel completed at 1792002449
00 007.575 cetvbend_mpowon: cetvdisplay_preheatN_OnEvent
00 007.577 cetvbend_mpowon: UpdateAmbientLight => cetvambi_ambl_SetState
01 007.587 <5>     7583 ZAP_END - UnBlank
01 007.589  svbas pgselN_OnProgramChangeCompleted
01 007.960 svspow_m.c:4753::Detected Mute = FALSE in vmtN
01 007.964 <5>     7959 ZAP_END - UnBlank
01 007.966 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 2048
01 007.968 RFS not found in environment
01 007.977 RFS not found in environment
01 007.979 FLASH system, mount request for partition 2 accepted
00 008.331 Timeout on mountcheck
01 008.692 svspow_m.c:4760::flashopN_OnPartitionMounted::partitionid:2
00 008.769 cetvbend_mpowon: cetvambi_ambilight_Disable
00 009.002 argv[0] is /philips/bin/networkhelper
00 009.002 udhcpc gave me deconfig
00 009.002 HandleUdhcpcNotif : msgq is 32769
01 009.155 svspow_m.c:4772::Sent flashopN_OnPartitionMounted::MOUNT_ON_EVENT
01 009.158 svspow_m.c:1872::gfx setpower ON
01 009.162 svspow_m.c:1875::gfx powntf for ON
01 009.164 cbmhgpow_mpow: SetPower to ON
01 009.166 cbmhgpow_mpow: OnPowerChanged
01 009.168 svspow_m.c:3428::cbmhg powntf received for ON
01 009.171 svspow_m.c:1913::cbmhg setpower On
01 009.267 svspow_m.c:1926::JUICE setpower On
01 009.279 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 16
01 009.282 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 256
-1 009.292 AppMan: Window added (0,0-852x480) [4] - 2!
01 009.298 Surface 0, PlaneId 2 in AttachSurface
00 009.989 argv[0] is /philips/bin/networkhelper
00 009.989 udhcpc gave me bound
00 009.989 udhcpc gave me bound
```

Figure 5-20 Example UART log during SWUPG startup (Normal startup) part 3.



```
00 009.989 IP address is 192.168.1.22
00 009.989 subnet mask is 255.255.255.0
00 009.989 $router is 192.168.1.1
00 009.989 First Gateway is 192.168.1.1
00 009.989 $dns is 192.168.1.1
00 009.989 DNS1 is 192.168.1.1
00 009.989 Interface is eth0
00 009.989 HandleUdhcpcNotif : msgq is 32769
00 010.083 route: SIOC[ADD|DEL]RT: No such process
01 010.623 svspow_m.c:3497::juice powntf received for ON
01 010.626 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 512
01 010.641 svspow_m.c:1943::ceapps setpower On
-1 010.649 AppMan: Window config - unhiding window
-1 010.649 Relayout of window 4
-1 010.657 AppMan: Switch focus to 0x5132d600 [4]
00 010.702  (!!!)  *** WARNING [color keying does not work on UPPER layer] *** [Philips/DirectFB/systems/cetvfb/primary.c:202 in get_color_minmax()]
01 010.868 svspow_m.c:3479::apps powntf received for ON
-1 010.881 AppMan: Window added (0,0-720x576) [5] - 0!
01 010.897 Surface 1, PlaneId 0 in AttachSurface
01 011.083 svspow_m.c:1803::Reached HandleTurnOn2Event with Event = 1024
01 011.086 svspow_m.c:693::Set Reached on state at 1792005965
01 011.088 svspow_m.c:755::Set has reached ON state
01 011.091 InitCehtvData done
01 011.312 ReadCehtvData ConfigVersion: [0.01] OK
01 011.312 ReadCehtvData ProductID: [Q591E] OK
01 011.312 ReadCehtvData OUI: [0000903E] OK
01 011.312 ReadCehtvData HardwareModel: [0203] OK
01 011.312 ReadCehtvData HardwareVersion: [0100] OK
01 011.312 ConvertAscii2Bin started
01 011.312 ConvertAscii2Bin done
01 011.312 ConvertAscii2Bin started
01 011.312 ConvertAscii2Bin done
01 011.312 ReadCehtvData PublicKey: OK
01 011.339 ReadCehtvData done, ConfigOK: TRUE
00 011.666 cetvbend_mpowon: iambl_SetState onoff = 1
00 011.668 cetvbend_mpowon: iambl_SetState onoff => cetvambi_ambl_SetState
00 011.672 cetvbend_mpowon: cetvambi_ambilight_Enable
-1 011.884 HK_PREPARE_PS_DONE received for cmd: 5, src: 1
-1 011.884 Remaining PowerChangeBitmap: 0
-1 011.884 starting :  /philips/apps/spettApp
-1 011.884 starting :  /philips/apps/media
01 011.905 svspow_m.c:2871::PREPARE_PS_DONE for cmd: 5
01 011.994 cbmhgpow_mpow: mRegisterAlarm - ClockSet
02 012.518     *--------------) FusionDale v0.1.1 (--------------*
02 012.518             (c) 2006-2007  directfb.org
02 012.518      ---------------------------------------------
02 012.524 Using errlib version 0.9
02 012.524 ***SPETT*** FusionDale Init done
02 012.524 ***SPETT*** Windows created
00 012.530 Errlib 0.9 registered from process 226
00 012.530 *** DirectFB Surface allocation FALLBACK! Acquiring id 7 with size 376320
-1 012.533 AppMan: Process added (226) [4]!
-1 012.533 AppMan: Window added (0,0-800x600) [6] - 0!
-1 012.533 Border window attached
-1 012.533 AppMan: Window added (100,100-672x280) [7] - 2!
-1 012.533 AppMan: Window config - unhiding window
-1 012.533 AppMan: Switch focus to 0x51334000 [7]
02 012.581 Event class:  DFEC_WINDOW
01 012.791 NITParser: Else of sec_SctArrived
01 012.791 cbmhgoad_m: strapi notification on completed
01 012.852 cbmhgoad_m :TARGETNIT = 0, TARGETNID = 513, spid = -1
01 012.854 cbmhgoad:mBarkerOadPumpHandler : mPrefFreqDirFound = 0
01 012.857 cbmhgoad: noofrecords = 0
03 013.196  MediaApp: Initalized and running
03 013.312 (*) FusionDale/Config: Parsing config file '/etc/fusiondalerc'.
03 013.312     *--------------) FusionDale v0.1.1 (--------------*
03 013.312             (c) 2006-2007  directfb.org
03 013.312      ---------------------------------------------
03 013.312 (*) Fusion/SHM: NOT using MADV_REMOVE (2.6.18.0 < 2.6.19.2)! [0x020 61200]
03 013.312 (*) Direct/Thread: Running 'Fusion Dispatch' (MESSAGING, 244)...
03 013.334  Using errlib version 0.9
03 013.334 MediaApp: Call back Init  from gplib
00 013.338 Errlib 0.9 registered from process 227
03 013.482 arunkp: mplfabsav2_m.c: 209: mplfabsav2__pow_Init:
-1 013.583 AppMan: Process added (227) [5]!
03 013.619 MediaApp: Gfx Init done
03 013.891 mediaApp: fusiondale Init, register called
03 013.891 mlock patch inited
-1 013.895 AppMan: Window added (100,100-480x300) [8] - 0!
-1 013.895 Border window attached
-1 013.895 AppMan: Switch focus to 0x51334e00 [8]
-1 013.895 AppMan: Window added (100,100-480x300) [9] - 1!
-1 013.895 Audio node attached
-1 013.907 AppMan: Switch focus to 0x51334e00 [8]
03 013.955 Network enabled and available -  enabling allegro
03 013.958 allegroenb_Enable
02 014.072 ***SPETT*** All inits done
02 014.075 ***SPETT*** gpilib.startr.Init done
01 014.105 ReadCehtvData done, ConfigOK: TRUE
01 014.107 cbmhgoad_mswupdt: chil_test_oui_only OUI = 0xd060,  ret = 0
01 014.375 CEAPPS : TARGETNIT = 0, TARGETNID = 8, spid = -1
03 014.555 The address is: 192.168.1.22
03 014.559 arunkp: mplfabsav2_m.c: 219: mplfabsav2__pow_TurnOn:
-1 014.957 AppMan: Window added (0,0-852x480) [10] - 2!
00 015.002 *** DirectFB Surface allocation FALLBACK! Acquiring id 0 with size 410880
03 015.005 Surface 0, PlaneId 2 in AttachSurface
00 015.027  (!!!)  *** WARNING [color keying does not work on UPPER layer] ***  [Philips/DirectFB/systems/cetvfb/primary.c:202 in get_color_minmax()]
03 015.224 Infrastructure Resource Gained by mediaApp
03 015.226 (resourcechanged && !(ResourceOwned & FULL_STATE) : Setting mappstate_mediaIdle
-1 015.276 AppMan: Window config - unhiding window
00 015.671 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
```

Figure 5-21 Example UART log during SWUPG startup (Normal startup) part 4.



```
03 015.788 Census Found device uuid: c7a4be7e-547d-11dc-8034-cc1538aeec30
03 015.792     DeviceType: schemas-upnp-org:device:MediaServer:1
-1 016.098 AppMan: Window config - unhiding window
-1 016.098 Relayout of window 5
00 017.948 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 018.154 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 018.727 ***GVC: T2 - ceisusb_m.c (951): "usbdevspN_OnDeviceError( DeviceUnknownAttachedError, -1 )" notification given
00 024.079 --- pass 0 ---
00 024.082 freeMem   :   26620
00 024.084 pgmajfault :      0
00 024.086 sectorsread:   11440
01 035.636 Merging eit data
01 035.650 Merging eit data
01 035.656 1419 records after eliminating duplicates
01 035.663 1419 records after eliminating duplicates
```

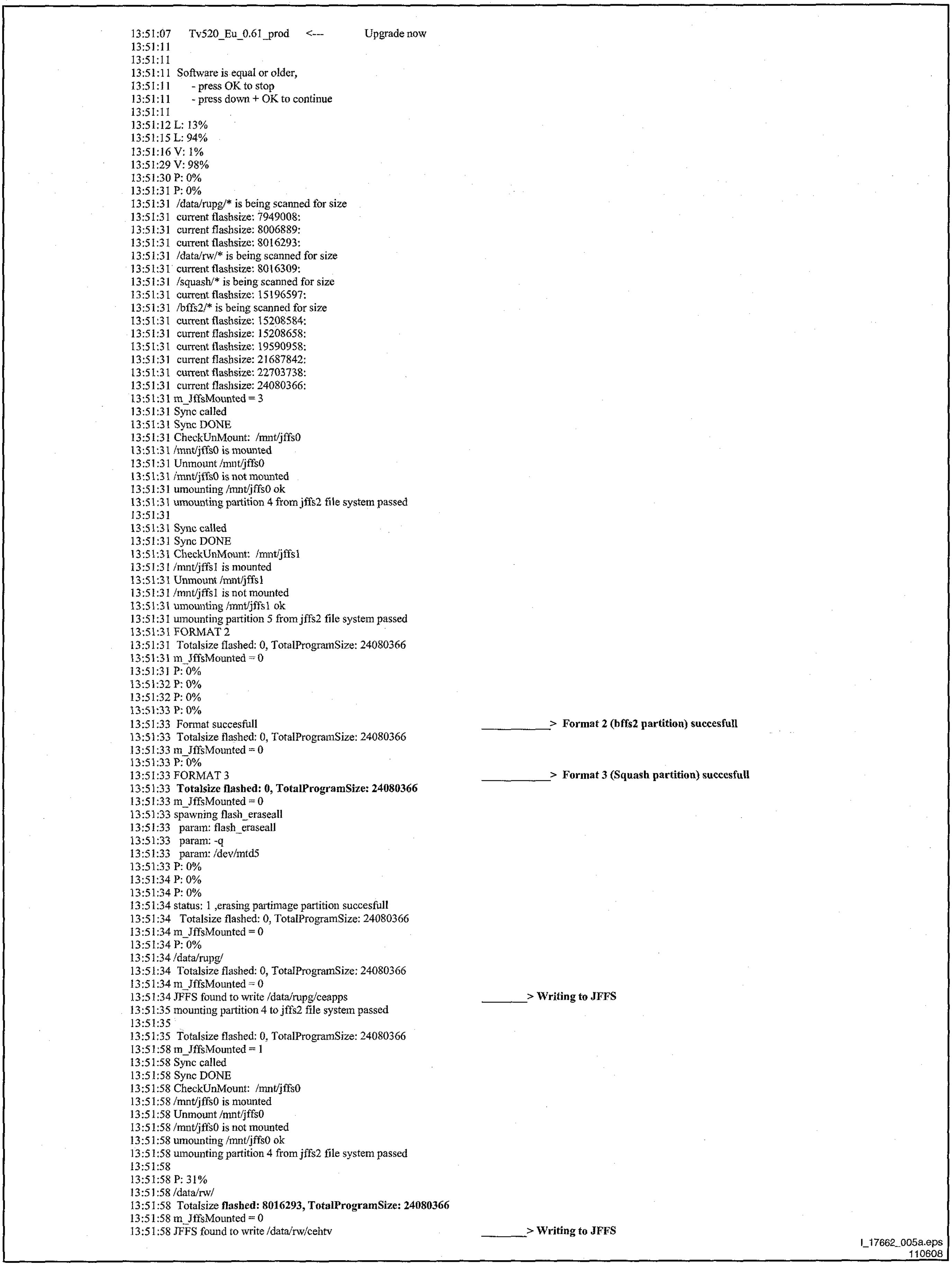
Figure 5-22 Example UART log during SWUPG startup (Normal startup) part 5.

- The “Application selection startup” part in the logs shows which application is being started up: backup SWUPG, normal SWUPG, TV application, ...
- In the TV application (Normal startup) case, there is no print on the UART which shows the software has started up completely. When startup issues arise, the best way to tackle them is by comparing the bad UART print with a correct print of the same release.

Upgrade of a TV set.

Following cannot be seen during industrial mode!

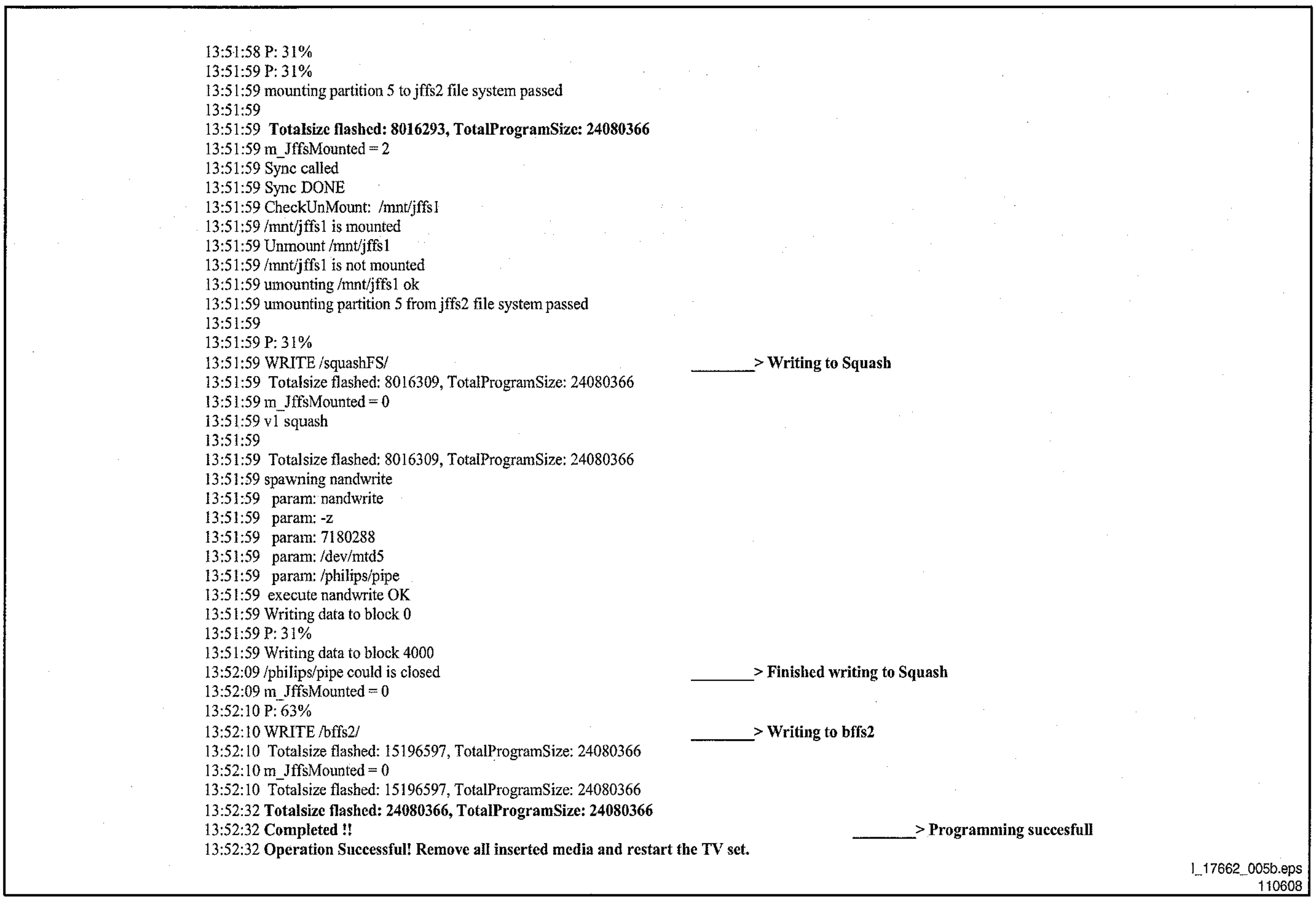
- When the Industrial Mode is enabled with command 203, no prints can be seen anymore on the UART. This is to not interfere with the P2P protocol.
- When in normal mode, the UART will show what the actions are during the upgrade.
- At certain periods in time during programming, the total size currently flashed (Totalsize flashed) and the size which should be finally flashed (TotalProgramSize) will be printed.



```
13:51:07    Tv520_Eu_0.61_prod    <---         Upgrade now
13:51:11
13:51:11
13:51:11  Software is equal or older,
13:51:11      - press OK to stop
13:51:11      - press down + OK to continue
13:51:11
13:51:12 L: 13%
13:51:15 L: 94%
13:51:16 V: 1%
13:51:29 V: 98%
13:51:30 P: 0%
13:51:31 P: 0%
13:51:31  /data/rupg/* is being scanned for size
13:51:31  current flashsize: 7949008:
13:51:31  current flashsize: 8006889:
13:51:31  current flashsize: 8016293:
13:51:31  /data/rw/* is being scanned for size
13:51:31  current flashsize: 8016309:
13:51:31  /squash/* is being scanned for size
13:51:31  current flashsize: 15196597:
13:51:31  /bffs2/* is being scanned for size
13:51:31  current flashsize: 15208584:
13:51:31  current flashsize: 15208658:
13:51:31  current flashsize: 19590958:
13:51:31  current flashsize: 21687842:
13:51:31  current flashsize: 22703738:
13:51:31  current flashsize: 24080366:
13:51:31 m_JffsMounted = 3
13:51:31 Sync called
13:51:31 Sync DONE
13:51:31 CheckUnMount:  /mnt/jffs0
13:51:31 /mnt/jffs0 is mounted
13:51:31 Unmount /mnt/jffs0
13:51:31 /mnt/jffs0 is not mounted
13:51:31 umounting /mnt/jffs0 ok
13:51:31 umounting partition 4 from jffs2 file system passed
13:51:31
13:51:31 Sync called
13:51:31 Sync DONE
13:51:31 CheckUnMount:  /mnt/jffs1
13:51:31 /mnt/jffs1 is mounted
13:51:31 Unmount /mnt/jffs1
13:51:31 /mnt/jffs1 is not mounted
13:51:31 umounting /mnt/jffs1 ok
13:51:31 umounting partition 5 from jffs2 file system passed
13:51:31 FORMAT 2
13:51:31  Totalsize flashed: 0, TotalProgramSize: 24080366
13:51:31 m_JffsMounted = 0
13:51:31 P: 0%
13:51:32 P: 0%
13:51:32 P: 0%
13:51:33 P: 0%
13:51:33  Format succesfull                                 __________> Format 2 (bffs2 partition) succesfull
13:51:33  Totalsize flashed: 0, TotalProgramSize: 24080366
13:51:33 m_JffsMounted = 0
13:51:33 P: 0%
13:51:33 FORMAT 3                                          __________> Format 3 (Squash partition) succesfull
13:51:33  Totalsize flashed: 0, TotalProgramSize: 24080366
13:51:33 m_JffsMounted = 0
13:51:33 spawning flash_eraseall
13:51:33   param: flash_eraseall
13:51:33   param: -q
13:51:33   param: /dev/mtd5
13:51:33 P: 0%
13:51:34 P: 0%
13:51:34 P: 0%
13:51:34 status: 1 ,erasing partimage partition succesfull
13:51:34   Totalsize flashed: 0, TotalProgramSize: 24080366
13:51:34 m_JffsMounted = 0
13:51:34 P: 0%
13:51:34 /data/rupg/
13:51:34  Totalsize flashed: 0, TotalProgramSize: 24080366
13:51:34 m_JffsMounted = 0
13:51:34 JFFS found to write /data/rupg/ceapps             _______> Writing to JFFS
13:51:35 mounting partition 4 to jffs2 file system passed
13:51:35
13:51:35  Totalsize flashed: 0, TotalProgramSize: 24080366
13:51:58 m_JffsMounted = 1
13:51:58 Sync called
13:51:58 Sync DONE
13:51:58 CheckUnMount:  /mnt/jffs0
13:51:58 /mnt/jffs0 is mounted
13:51:58 Unmount /mnt/jffs0
13:51:58 /mnt/jffs0 is not mounted
13:51:58 umounting /mnt/jffs0 ok
13:51:58 umounting partition 4 from jffs2 file system passed
13:51:58
13:51:58 P: 31%
13:51:58 /data/rw/
13:51:58  Totalsize flashed: 8016293, TotalProgramSize: 24080366
13:51:58 m_JffsMounted = 0
13:51:58 JFFS found to write /data/rw/cehtv                _______> Writing to JFFS
```

I_17662_005a.eps
110608

Figure 5-23 Example UART log during normal user upgrade part 1.



```
13:51:58 P: 31%
13:51:59 P: 31%
13:51:59 mounting partition 5 to jffs2 file system passed
13:51:59
13:51:59  Totalsize flashed: 8016293, TotalProgramSize: 24080366
13:51:59 m_JffsMounted = 2
13:51:59 Sync called
13:51:59 Sync DONE
13:51:59 CheckUnMount:  /mnt/jffs1
13:51:59 /mnt/jffs1 is mounted
13:51:59 Unmount /mnt/jffs1
13:51:59 /mnt/jffs1 is not mounted
13:51:59 umounting /mnt/jffs1 ok
13:51:59 umounting partition 5 from jffs2 file system passed
13:51:59
13:51:59 P: 31%
13:51:59 WRITE /squashFS/                                    _______> Writing to Squash
13:51:59  Totalsize flashed: 8016309, TotalProgramSize: 24080366
13:51:59 m_JffsMounted = 0
13:51:59 v1 squash
13:51:59
13:51:59  Totalsize flashed: 8016309, TotalProgramSize: 24080366
13:51:59 spawning nandwrite
13:51:59   param: nandwrite
13:51:59   param: -z
13:51:59   param: 7180288
13:51:59   param: /dev/mtd5
13:51:59   param: /philips/pipe
13:51:59  execute nandwrite OK
13:51:59 Writing data to block 0
13:51:59 P: 31%
13:51:59 Writing data to block 4000
13:52:09 /philips/pipe could is closed                       _______> Finished writing to Squash
13:52:09 m_JffsMounted = 0
13:52:10 P: 63%
13:52:10 WRITE /bffs2/                                       _______> Writing to bffs2
13:52:10  Totalsize flashed: 15196597, TotalProgramSize: 24080366
13:52:10 m_JffsMounted = 0
13:52:10  Totalsize flashed: 15196597, TotalProgramSize: 24080366
13:52:32 Totalsize flashed: 24080366, TotalProgramSize: 24080366
13:52:32 Completed !!                                                    _______> Programming succesfull
13:52:32 Operation Successful! Remove all inserted media and restart the TV set.
```

Figure 5-24 Example UART log during normal user upgrade part 2.

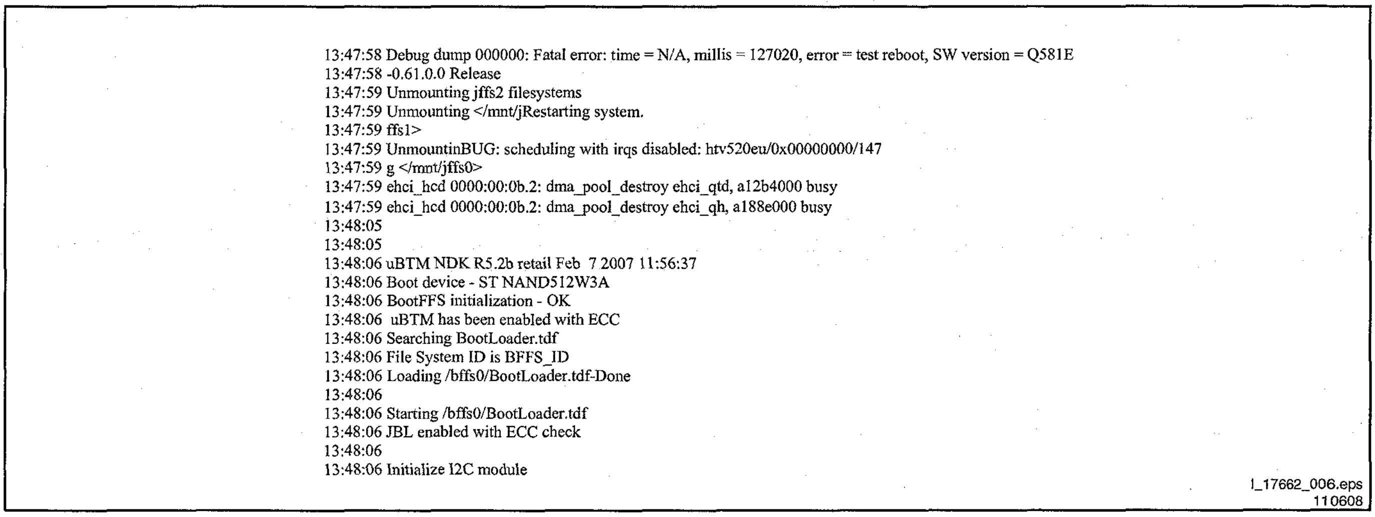
Problem analysis of a TV set.

During programming:

- The amount of Bad Blocks is bigger then promised by the flash manufacture. This is checked on virgin boards.
- Bad blocks have been created during programming and there is not enough good block anymore in the partition to write data into. This can happen on boards which are being reprogrammed.
- Mounting of the JFFS partitions take to long.
- When the flashutil UPG is being programmed on a boards which already contains a different Partition Table, the writing of the bootblock (µBTM and partitionTable) will fail. This can only happen on non virgin boards.
- When the power drops the programming will be stop. Depending on when the power drop is the result will be different.
  1. FUS UPG. The SWUPG will try to reprogram the UPG once the power is back.
  2. Flashutil UPG. Cannot recover anymore, because nothing is in flash anymore. Has to be reprogrammed on the line again.
  3. Upgrade All. Depending when the power drop happens. When it happens in the beginning, the board will only be reprogrammable on the line.
- If a development UPG is used on a production SWUPG or visa versa. Validation will fail.
- If loading fails (cannot read file error), it is mostly due to a long USB cable or a bad USB stick.
- If the UPG size is bigger then the memory allocated by the software upgrade application, then the UPG will not be programmed. See the prints fo the SWUPG at startup.

During startup:

- Compare the UART logging on the problem board/set with a normal startup behaviour. Identify till which point the logging reaches.
- If a crash happens, it will be outputted on the UART. In the background the information of the dump will be written into JFFS0. The UPG to copy the dump content out of flash should be available for everybody.



```
13:47:58 Debug dump 000000: Fatal error: time = N/A, millis = 127020, error = test reboot, SW version = Q581E
13:47:58 -0.61.0.0 Release
13:47:59 Unmounting jffs2 filesystems
13:47:59 Unmounting </mnt/jRestarting system.
13:47:59 ffs1>
13:47:59 UnmountinBUG: scheduling with irqs disabled: htv520eu/0x00000000/147
13:47:59 g </mnt/jffs0>
13:47:59 ehci_hcd 0000:00:0b.2: dma_pool_destroy ehci_qtd, a12b4000 busy
13:47:59 ehci_hcd 0000:00:0b.2: dma_pool_destroy ehci_qh, a188e000 busy
13:48:05
13:48:05
13:48:06 uBTM NDK R5.2b retail Feb  7 2007 11:56:37
13:48:06 Boot device - ST NAND512W3A
13:48:06 BootFFS initialization - OK
13:48:06  uBTM has been enabled with ECC
13:48:06 Searching BootLoader.tdf
13:48:06 File System ID is BFFS_ID
13:48:06 Loading /bffs0/BootLoader.tdf-Done
13:48:06
13:48:06 Starting /bffs0/BootLoader.tdf
13:48:06 JBL enabled with ECC check
13:48:06
13:48:06 Initialize I2C module
```

Figure 5-25 Example UART log during problem.

Problem solution.

When programming fails:

- Check in the NVM at address 0x1D02 (BadBlocksAmount). This items is 2 bytes.
  1. If, after programming the flashutil UPG, this value is still the same as the one of the process NVM, then the amount of bad blocks was bigger then described by the flash manufacturer.
  2. If the value is filled in, it has to be checked if it's not to close the maximum amount possible.
  3. If the value is low, no problem.
- If mounting fails, it will be shown on the UART. This can only be seen when industrial mode is disabled.
- As the UART logs are disabled when in industrial mode, it is always good to have a set (or minimal setup) where the problem board can be tested in. In this way the problem can be reproduced in the normal mode of the SWUPG and the prints will be visible!

When startup fails:

- When a crash happens (only in the TV application!) and is followed by debug dump UART output, then a copy of the dump can put on a USB stick
  1. This can only be done in the TV application, so if the TV application keeps on crashing there is no way to copy the dump of the flash to a USB stick.
  2. When the TV application has started up completely, CSM can be entered by pressing 1, 2, 3, 6, 5, 4.
  3. Then put the remote in DVD mode and press 2, 6, 7, 9.
  4. The file Dump_seetypeplate_seetypeplate.bin can be found now on the USB storage device. The seetypeplate_seetypeplate will be filled in depending on the type of set.
  5. This .bin file can only be interpreted in a Philips development centre. Please give this input to your Philips Service contact person.
- Compare the UART logging on the problem board/set with a normal startup behaviour. Identify till which point the logging reaches.

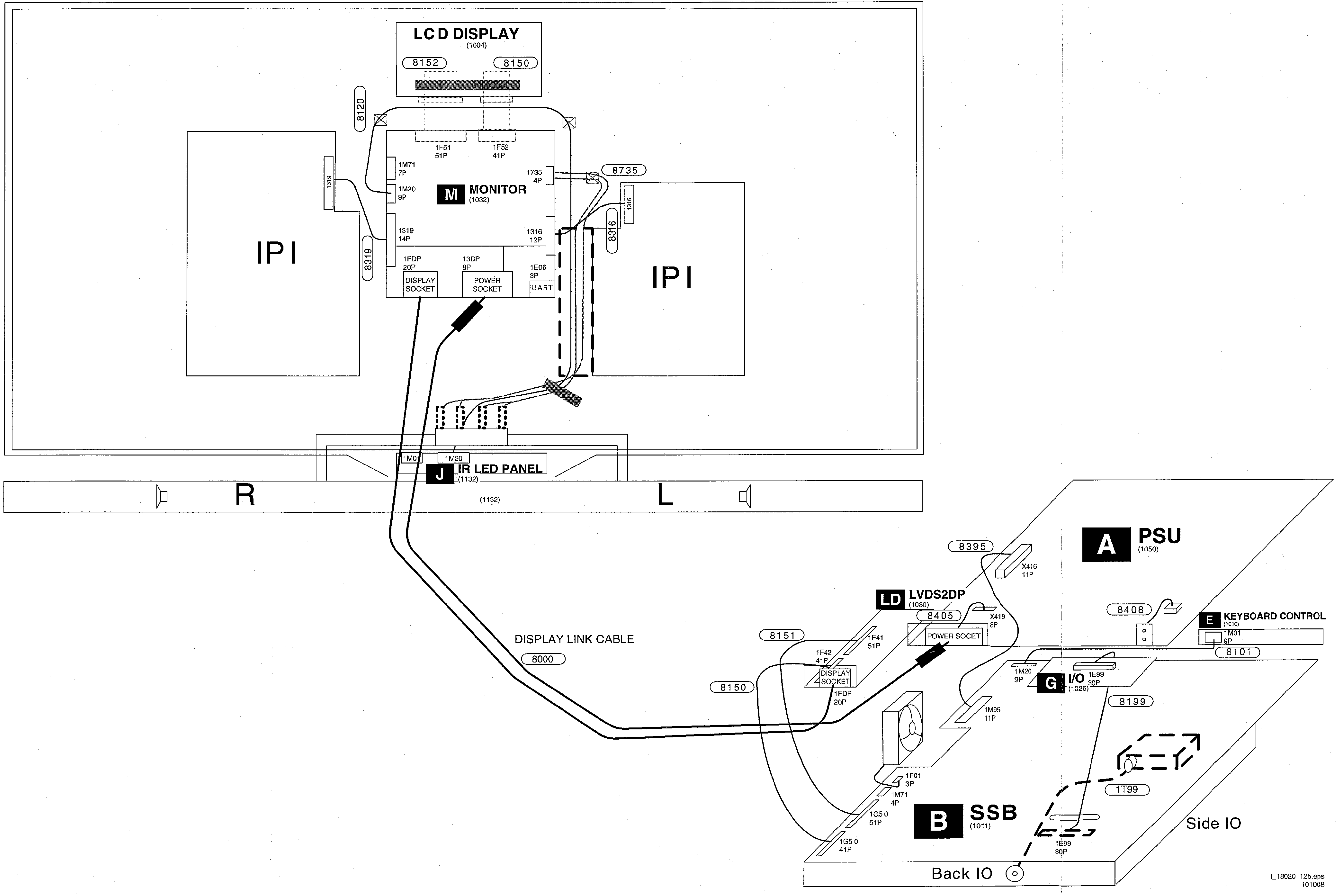
Personal Notes:

E_06532_012.eps
131004

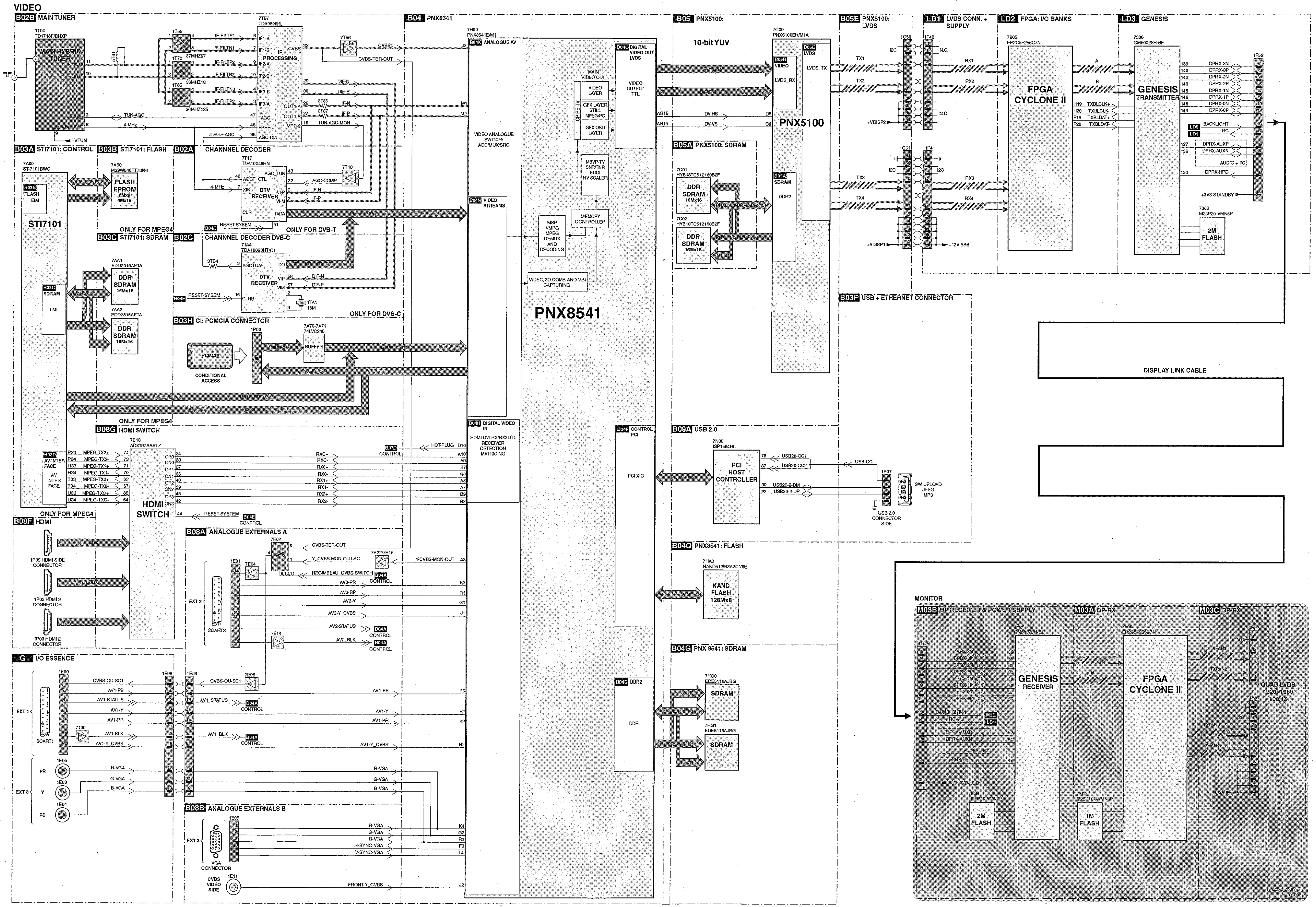
6. Block Diagrams, Test Point Overview, and Waveforms

Wiring Diagram Essence

WIRING E SSENCE


LC D DISPLAY
(1004)
8152
8150
8120
1F51
51P
1F52
41P
1M71
7P
1M20
9P
M MONITOR
(1032)
1735
4P
8735
1319
1319
14P
1316
12P
1316
8316
8319
1FDP
20P
13DP
8P
1E06
3P
DISPLAY SOCKET
POWER SOCKET
UART
IPI
IPI
1M01
1M20
J IR LED PANEL
(1132)
R
L
(1132)
DISPLAY LINK CABLE
8000
A PSU
(1050)
8395
X416
11P
LD LVDS2DP
(1030)
8405
X419
8P
POWER SOCET
8408
E KEYBOARD CONTROL
(1010)
1M01
9P
8101
8151
1F41
51P
1F42
41P
DISPLAY SOCKET
1FDP
20P
8150
1M20
9P
G I/O
(1026)
1E99
30P
8199
1M95
11P
1F01
3P
1M71
4P
1G5 0
51P
1G5 0
41P
B SSB
(1011)
1T99
1E99
30P
Side IO
Back IO
I_18020_125.eps
101008

Block Diagram Video


VIDEO
B02B MAIN TUNER
1T04
TD1716F/BHXP
MAIN HYBRID TUNER
IF-OUT2
IF-OUT1
SF-AGC
5V XTAL OUT
+VTUN
5T61
1T55
37MHZ67
1T70
36MHZ18
1T65
36MHZ125
IF-FILTP1
IF-FILTN1
IF-FILTP2
IF-FILTN2
IF-FILTN3
IF-FILTP3
TUN-AGC
4-MHz
7T57
TDA9898HL
IF1-A
IF1-B
IF2-A
IF2-B
IF3-B
IF3-A
TAGC
FREF
AGC-DIN
IF PROCESSING
CVBS
OUT1-A
OUT1-B
MPP-2
TDA-IF-AGC
7T56
EF
CVBS4
CVBS-TER-OUT
DIF-N
DIF-P
3T86
3T87
IF-N
IF-P
TUN-AGC-MON
B03A STI7101: CONTROL
7A00
ST-7101BWC
B03B FLASH EMI
STI7101
B03B STI7101: FLASH
7A50
M29W640FT70N6
EMI-D(0-15)
EMI-A(1-22)
FLASH EPROM 8Mx8 4Mx16
ONLY FOR MPEG4
B03C STI7101: SDRAM
B03C SDRAM LMI
7AA1
EDD2516AETA
DDR SDRAM 16Mx16
7AA2
EDD2516AETA
DDR SDRAM 16Mx16
LMI-D(0-31)
LMI-A(0-12)
B02A CHANNNEL DECODER
7T17
TDA10048HN
AGC_TUN
AGCT_CTL
XIN
DTV RECEIVER
VI-P
VI-M
CLR
DATA
7T18
AGC-COMP
B04E RESET-SYSEM
ONLY FOR DVB-T
B02C CHANNEL DECODER DVB-C
7TA4
TDA10023HT/C1
3TB4
AGCTUN
DO
DTV RECEIVER
VIP
VIM
CLRB
1TA1
16M
ONLY FOR DVB-C
B03H CI: PCMCIA CONNECTOR
1P00
7A70-7A71
74LVC245
PCMCIA
CONDITIONAL ACCESS
BUFFER
MDO(0-7)
CA-MDI(0-7)
ONLY FOR MPEG4
B08G HDMI SWITCH
7E13
AD8197AASTZ
B03D AV-INTER FACE
AV INTER FACE
MPEG-TX2+
MPEG-TX2-
MPEG-TX1+
MPEG-TX1-
MPEG-TX0+
MPEG-TX0-
MPEG-TXC+
MPEG-TXC-
HDMI SWITCH
OP0
ON0
OP1
ON1
OP2
ON2
OP3
ON3
RXC+
RXC-
RX0+
RX0-
RX1+
RX1-
RX2+
RX2-
B07D CONTROL
HOT-PLUG
RESET-SYSTEM
B04E CONTROL
ONLY FOR MPEG4
B08F HDMI
1P05 HDMI SIDE CONNECTOR
1P02 HDMI 3 CONNECTOR
1P03 HDMI 2 CONNECTOR
B08A ANALOGUE EXTERNALS A
7E02
7E22/7E16
Y-CVBS-MON-OUT
Y_CVBS-MON-OUT-SC
REGIMBEAU_CVBS-SWITCH
B04A CONTROL
1E01
7E04
EXT 2
SCART2
AV3-PR
AV3-BP
AV3-Y
AV2-Y_CVBS
AV2-STATUS
7E14
AV2_BLK
G I/O ESSENCE
1E00
1E99
EXT 1
SCART1
7100
CVBS-OU-SC1
AV1-PB
AV1-STATUS
AV1-Y
AV1-PR
AV1-BLK
AV1-Y_CVBS
7E05
AV1_STATUS
AV1_BLK
EXT 3
1E05
PR
1E03
Y
1E04
PB
R-VGA
G-VGA
B-VGA
B08B ANALOGUE EXTERNALS B
VGA CONNECTOR
H-SYNC-VGA
V-SYNC-VGA
CVBS VIDEO SIDE
1E11
FRONT-Y_CVBS
B04 PNX8541
7H00
PNX8541E/M1
B04K ANALOGUE AV
VIDEO ANALOGUE SWITCH/ ADC/MUX/SRC
B04N VIDEO STREAMS
B04H DIGITAL VIDEO IN
HDMI-DVI RX/RX2DTL RECEIVER DETECTION MATRICING
B04O DIGITAL VIDEO OUT LVDS
MAIN VIDEO OUT
VIDEO LAYER
GFX LAYER STILL MPEG/PC
GFX OSD LAYER
CPIPE-TV
VIDEO OUTPUT TTL
MBVP-TV SNR/TNR EDDI HV SCALER
MEMORY CONTROLLER
MSP VMPG MPEG DEMUX AND DECODING
VIDEC, 3D COMB AND VBI CAPTURING
PNX8541
B04F CONTROL PCI
PCI XIO
B04G DDR2
DDR
B05 PNX5100:
10-bit YUV
DV-HS
DV-VS
7C00
PNX5100EH/M1A
B05B VIDEO LVDS_RX
B05E LVDS
LVDS_TX
PNX5100
B05A SDRAM DDR2
B05A PNX5100: SDRAM
7C01
HYB18TC512160B2F
DDR SDRAM 16Mx16
7C02
HYB18TC512160B2F
DDR SDRAM 16Mx16
B09A USB 2.0
7N00
ISP1564HL
PCI HOST CONTROLLER
USB20-OC1
USB20-OC2
USB20-2-DM
USB20-2-DP
USB-OC
1P07
SW UPLOAD JPEG MP3
USB 2.0 CONNECTOR SIDE
B04Q PNX8541: FLASH
7HA0
NAND512W3A2CN6E
NAND FLASH 128Mx8
B04G PNX 8541: SDRAM
7HG0
EDE5116AJBG
SDRAM
7HG1
EDE5116AJBG
SDRAM
B05E PNX5100: LVDS
TX1
TX2
TX3
TX4
1G50
1G51
I2C
+VDISP2
+VDISP1
LD1 LVDS CONN. + SUPPLY
1F42
1F41
N.C.
RX1
RX2
RX3
RX4
+12V-SSB
LD2 FPGA: I/O BANKS
7205
EP2C5F256C7N
FPGA CYCLONE II
TXBLCLK+
TXBLCLK-
TXBLDAT+
TXBLDAT-
LD3 GENESIS
7300
GM60028H-BF
GENESIS TRANSMITTER
A
B
DPRX-3N
DPRX-3P
DPRX-2N
DPRX-2P
DPRX-1N
DPRX-1P
DPRX-0N
DPRX-0P
LD5 BACKLIGHT
LD1 RC
DPRX-AUXP
DPRX-AUXN
AUDIO + I²C
DPRX-HPD
+3V3-STANDBY
1F52
7302
M25P20-VMN6P
2M FLASH
B03F USB + ETHERNET CONNECTOR
DISPLAY LINK CABLE
MONITOR
M03B DP RECEIVER & POWER SUPPLY
1FDP
BACKLIGHT-IN
RC-OUT
M3B
LD1
+3V3-STANDBY
7F0A
GM68020H-BE
GENESIS RECEIVER
7F0B
M25P20-VMN6P
2M FLASH
M03A DP-RX
7F02
M25P10-AVMN6P
1M FLASH
7F00
EP2C5F256C7N
FPGA CYCLONE II
M03C DP-RX
TXPAN1
TXPAN2
TXPAN3
TXPAN4
1F52
1F51
QUAD LVDS 1920x1080 100HZ
+12V
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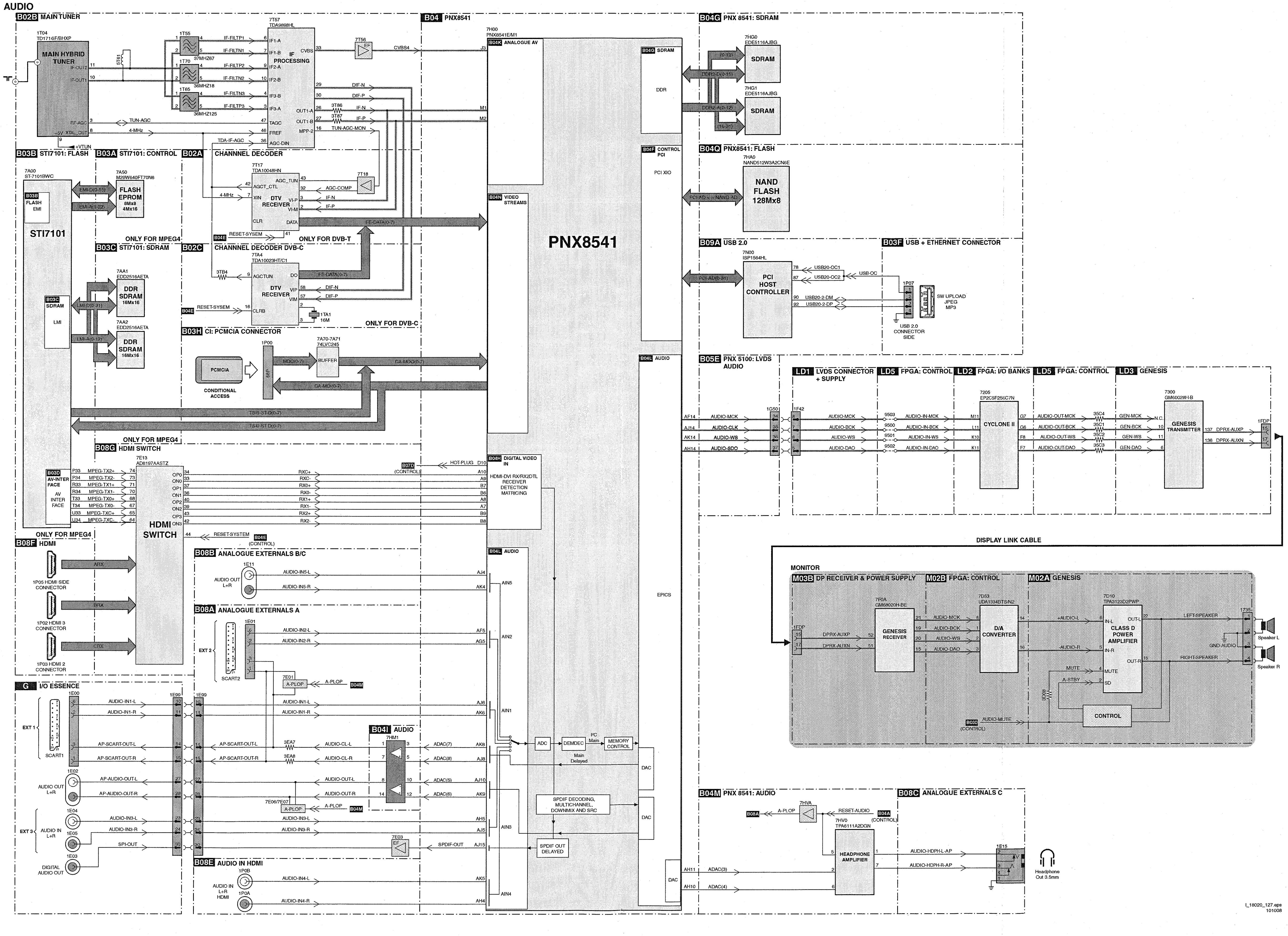
Block Diagram Audio


AUDIO
B02B MAIN TUNER
1T04 TD1716F/SHXP
MAIN HYBRID TUNER
IF-OUT2
IF-OUT1
RF-AGC
+5V XTAL_OUT
+VTUN
TUN-AGC
4-MHz
1T55
1T70 37MHZ67
1T65 36MHZ18
36MHZ125
IF-FILTP1
IF-FILTN1
IF-FILTP2
IF-FILTN2
IF-FILTN3
IF-FILTP3
7T57 TDA9898HL
IF PROCESSING
CVBS
TAGC
FREF
AGC-DIN
OUT1-A
OUT1-B
MPP-2
TDA-IF-AGC
7T56
EF
CVBS4
DIF-N
DIF-P
3T86
3T87
IF-N
IF-P
TUN-AGC-MON
B03B STI7101: FLASH
B03A STI7101: CONTROL
B02A CHANNEL DECODER
7A00 ST-7101BWC
FLASH EMI
STI7101
7A50 M29W640FT70N6
FLASH EPROM 8Mx8 4Mx16
EMI-D(0-15)
EMI-A(1-22)
7T17 TDA10048HN
DTV RECEIVER
AGC_TUN
AGC_CTL
XIN
VI-P
VI-M
CLR
DATA
7T18
AGC-COMP
IF-N
IF-P
FE-DATA(0-7)
RESET-SYSEM
ONLY FOR MPEG4
ONLY FOR DVB-T
B03C STI7101: SDRAM
B02C CHANNEL DECODER DVB-C
7TA4 TDA10023HT/C1
3TB4
AGCTUN
DTV RECEIVER
DO
VIP
VIM
CLRB
FE-DATA(0-7)
DIF-N
DIF-P
RESET-SYSEM
1TA1 16M
ONLY FOR DVB-C
SDRAM
LMI
7AA1 EDD2516AETA
DDR SDRAM 16Mx16
7AA2 EDD2516AETA
DDR SDRAM 16Mx16
LMI-D(0-31)
LMI-A(0-12)
B03H CI: PCMCIA CONNECTOR
1P00
7A70-7A71 74LVC245
BUFFER
PCMCIA
CONDITIONAL ACCESS
MDO(0-7)
CA-MOO(0-7)
CA-MDI(0-7)
TSI1-ST-D(0-7)
TSI0-ST-D(0-7)
ONLY FOR MPEG4
B08G HDMI SWITCH
7E13 AD8197AASTZ
B03D AV-INTERFACE
AV INTERFACE
MPEG-TX2+
MPEG-TX2-
MPEG-TX1+
MPEG-TX1-
MPEG-TX0+
MPEG-TX0-
MPEG-TXC+
MPEG-TXC-
HDMI SWITCH
RXC+
RXC-
RX0+
RX0-
RX1+
RX1-
RX2+
RX2-
B07D (CONTROL)
HOT-PLUG
RESET-SYSTEM
B04E (CONTROL)
ONLY FOR MPEG4
B08F HDMI
ARX
BRX
CRX
1P05 HDMI SIDE CONNECTOR
1P02 HDMI 3 CONNECTOR
1P03 HDMI 2 CONNECTOR
B04 PNX8541
7H00 PNX8541E/M1
B04K ANALOGUE AV
B04N VIDEO STREAMS
PNX8541
B04G SDRAM
DDR
B04F CONTROL PCI
PCI XIO
B04H DIGITAL VIDEO IN
HDMI-DVI RX/RX2DTL RECEIVER DETECTION MATRICING
B04L AUDIO
EPICS
AIN5
AIN2
AIN1
AIN3
AIN4
ADC
DEMDEC
I²C Main
MEMORY CONTROL
Main Delayed
DAC
SPDIF DECODING, MULTICHANNEL, DOWNMIX AND SRC
SPDIF OUT DELAYED
B04G PNX 8541: SDRAM
7HG0 EDE5116AJBG
SDRAM
7HG1 EDE5116AJBG
SDRAM
DDR2-D(0-15)
DDR2-A(0-12)
B04Q PNX8541: FLASH
7HA0 NAND512W3A2CN6E
NAND FLASH 128Mx8
PCI-AD<->NAND-AD
B09A USB 2.0
7N00 ISP1564HL
PCI HOST CONTROLLER
PCI-AD(0-31)
USB20-OC1
USB20-OC2
USB-OC
USB20-2-DM
USB20-2-DP
B03F USB + ETHERNET CONNECTOR
1P07
SW UPLOAD JPEG MP3
USB 2.0 CONNECTOR SIDE
B05E PNX 5100: LVDS AUDIO
LD1 LVDS CONNECTOR + SUPPLY
LD5 FPGA: CONTROL
LD2 FPGA: I/O BANKS
LD5 FPGA: CONTROL
LD3 GENESIS
AUDIO-MCK
AUDIO-CLK
AUDIO-WS
AUDIO-SDO
1G50
1F42
AUDIO-BCK
AUDIO-DAO
AUDIO-IN-MCK
AUDIO-IN-BCK
AUDIO-IN-WS
AUDIO-IN-DAO
7205 EP2C5F256C7N
CYCLONE II
AUDIO-OUT-MCK
AUDIO-OUT-BCK
AUDIO-OUT-WS
AUDIO-OUT-DAO
GEN-MCK
GEN-BCK
GEN-WS
GEN-DAO
7300 GM60028H-B
GENESIS TRANSMITTER
DPRX-AUXP
DPRX-AUXN
1FDP
DISPLAY LINK CABLE
MONITOR
M03B DP RECEIVER & POWER SUPPLY
M02B FPGA: CONTROL
M02A GENESIS
7F0A GM68020H-BE
GENESIS RECEIVER
7D53 UDA1334BTS/N2
D/A CONVERTER
7D10 TPA3123D2PWP
CLASS D POWER AMPLIFIER
+AUDIO-L
-AUDIO-R
IN-L
IN-R
OUT-L
OUT-R
MUTE
A-STBY
SD
LEFT-SPEAKER
RIGHT-SPEAKER
GND-AUDIO
1735
Speaker L
Speaker R
CONTROL
B03D (CONTROL)
AUDIO-MUTE
B04M PNX 8541: AUDIO
B08C ANALOGUE EXTERNALS C
7HVA
A-PLOP
B08A
RESET-AUDIO
B04A (CONTROL)
7HV0 TPA6111A2DGN
HEADPHONE AMPLIFIER
AUDIO-HDPH-L-AP
AUDIO-HDPH-R-AP
1E15
Headphone Out 3.5mm
ADAC(3)
ADAC(4)
B08B ANALOGUE EXTERNALS B/C
1E11
AUDIO OUT L+R
AUDIO-IN5-L
AUDIO-IN5-R
B08A ANALOGUE EXTERNALS A
1E01
EXT 2
SCART2
AUDIO-IN2-L
AUDIO-IN2-R
7E01 A-PLOP
B04M
G I/O ESSENCE
1E00
EXT 1
SCART1
AUDIO-IN1-L
AUDIO-IN1-R
AP-SCART-OUT-L
AP-SCART-OUT-R
1E02
AUDIO OUT L+R
AP-AUDIO-OUT-L
AP-AUDIO-OUT-R
1E04
EXT 3
AUDIO IN L+R
1E05
AUDIO-IN3-L
AUDIO-IN3-R
SPI-OUT
1E03
DIGITAL AUDIO OUT
1E99
B04I AUDIO
7HM1
3EA7
3EA8
AUDIO-CL-L
AUDIO-CL-R
AUDIO-OUT-L
AUDIO-OUT-R
ADAC(7)
ADAC(8)
ADAC(5)
ADAC(6)
7E06/7E07
7E03
EF
SPDIF-OUT
B08E AUDIO IN HDMI
1P0B
1P0A
AUDIO IN L+R HDMI
AUDIO-IN4-L
AUDIO-IN4-R
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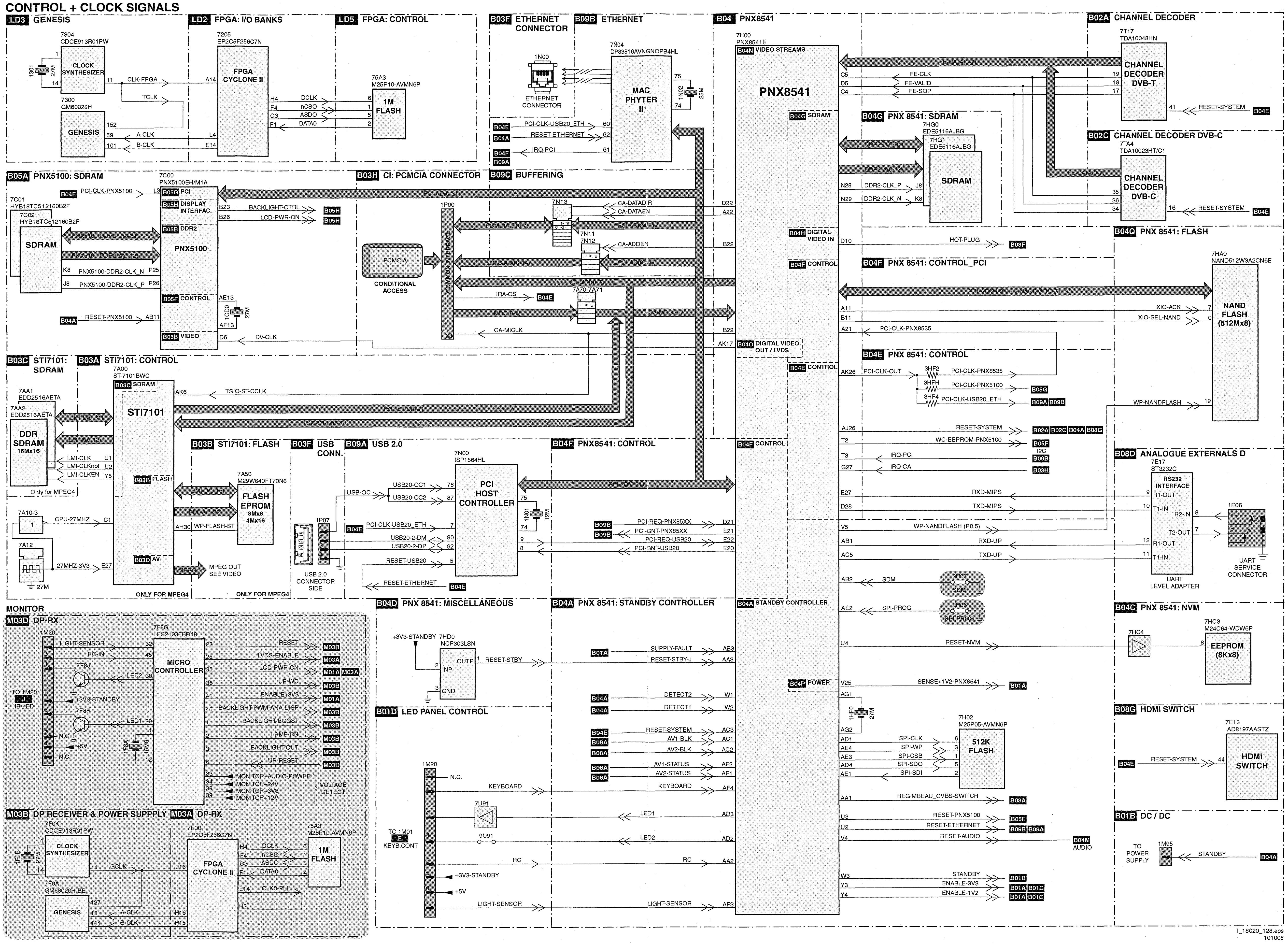
Block Diagram Control & Clock Signals

CONTROL + CLOCK SIGNALS


LD3 GENESIS
7304
CDCE913R01PW
CLOCK SYNTHESIZER
1301
27M
1
14
11
CLK-FPGA
TCLK
7300
GM60028H
GENESIS
152
59
101
A-CLK
B-CLK
LD2 FPGA: I/O BANKS
7205
EP2C5F256C7N
FPGA CYCLONE II
A14
L4
E14
H4
F4
C3
F1
DCLK
nCSO
ASDO
DATA0
LD5 FPGA: CONTROL
75A3
M25P10-AVMN6P
1M FLASH
6
1
5
2
B03F ETHERNET CONNECTOR
1N00
ETHERNET CONNECTOR
B09B ETHERNET
7N04
DP83816AVNGNOPB4HL
MAC PHYTER II
75
74
1N02
25M
B04E
PCI-CLK-USB20_ETH
60
B04A
RESET-ETHERNET
62
B04E
B09A
IRQ-PCI
61
B04 PNX8541
7H00
PNX8541E
B04N VIDEO STREAMS
PNX8541
B04G SDRAM
B04H DIGITAL VIDEO IN
B04F CONTROL
B04O DIGITAL VIDEO OUT / LVDS
B04E CONTROL
B04F CONTROL
B04A STANDBY CONTROLLER
B04P POWER
FE-DATA(0-7)
C5
D5
C4
FE-CLK
FE-VALID
FE-SOP
B02A CHANNEL DECODER
7T17
TDA10048HN
CHANNEL DECODER DVB-T
19
18
17
41
RESET-SYSTEM
B04E
B02C CHANNEL DECODER DVB-C
7TA4
TDA10023HT/C1
CHANNEL DECODER DVB-C
FE-DATA(0-7)
35
36
34
16
RESET-SYSTEM
B04E
B04G PNX 8541: SDRAM
7HG0
EDE5116AJBG
7HG1
EDE5116AJBG
SDRAM
DDR2-D(0-31)
DDR2-A(0-12)
N28
DDR2-CLK_P
J8
N29
DDR2-CLK_N
K8
D10
HOT-PLUG
B08F
B04Q PNX 8541: FLASH
7HA0
NAND512W3A2CN6E
NAND FLASH (512Mx8)
B04F PNX 8541: CONTROL_PCI
PCI-AD(24-31) -> NAND-AD(0-7)
A11
XIO-ACK
7
B11
XIO-SEL-NAND
0
A21
PCI-CLK-PNX8535
B04E PNX 8541: CONTROL
AK26
PCI-CLK-OUT
3HF2
PCI-CLK-PNX8535
3HFH
PCI-CLK-PNX5100
B05G
3HF4
PCI-CLK-USB20_ETH
B09A B09B
WP-NANDFLASH
19
AJ26
RESET-SYSTEM
B02A B02C B04A B08G
T2
WC-EEPROM-PNX5100
B05F
I2C
T3
IRQ-PCI
B09B
G27
IRQ-CA
B03H
E27
RXD-MIPS
D28
TXD-MIPS
V5
WP-NANDFLASH (P0.5)
AB1
RXD-UP
AC5
TXD-UP
AB2
SDM
2H07
SDM
AE2
SPI-PROG
2H06
SPI-PROG
B08D ANALOGUE EXTERNALS D
7E17
ST3232C
RS232 INTERFACE
9
R1-OUT
10
T1-IN
R2-IN
8
T2-OUT
7
12
R1-OUT
11
T1-IN
UART LEVEL ADAPTER
1E06
3
2
UART SERVICE CONNECTOR
B04C PNX 8541: NVM
U4
RESET-NVM
7HC4
7HC3
M24C64-WDW6P
8
EEPROM (8Kx8)
V25
SENSE+1V2-PNX8541
B01A
AG1
1HF0
27M
AG2
7H02
M25P05-AVMN6P
512K FLASH
AD1
SPI-CLK
6
AE4
SPI-WP
3
AE3
SPI-CSB
1
AD4
SPI-SDO
5
AE1
SPI-SDI
2
B08G HDMI SWITCH
7E13
AD8197AASTZ
B04E
RESET-SYSTEM
44
HDMI SWITCH
AA1
REGIMBEAU_CVBS-SWITCH
B08A
U3
RESET-PNX5100
B05F
U2
RESET-ETHERNET
B09B B09A
V4
RESET-AUDIO
B04M AUDIO
B01B DC / DC
TO POWER SUPPLY
1M95
2
STANDBY
B04A
W3
STANDBY
B01B
Y3
ENABLE-3V3
B01A B01C
Y4
ENABLE-1V2
B01A B01C
B05A PNX5100: SDRAM
7C00
PNX5100EH/M1A
B04E
PCI-CLK-PNX5100
L3
B05G PCI
B05H DISPLAY INTERFAC.
B23
BACKLIGHT-CTRL
B05H
B26
LCD-PWR-ON
B05H
B05B DDR2
PNX5100
B05F CONTROL
B05B VIDEO
7C01
HYB18TC512160B2F
7C02
HYB18TC512160B2F
SDRAM
PNX5100-DDR2-D(0-31)
PNX5100-DDR2-A(0-12)
K8
PNX5100-DDR2-CLK_N
P25
J8
PNX5100-DDR2-CLK_P
P26
B04A
RESET-PNX5100
AB11
AE13
1CD0
27M
AF13
D6
DV-CLK
PCI-AD(0-31)
B03H CI: PCMCIA CONNECTOR
1P00
1
COMMON INTERFACE
68
PCMCIA
CONDITIONAL ACCESS
PCMCIA-D(0-7)
PCMCIA-A(0-14)
IRA-CS
B04E
MDO(0-7)
CA-MICLK
B09C BUFFERING
7N13
CA-DATADIR
CA-DATAEN
PCI-AD(24-31)
7N11
7N12
CA-ADDEN
PCI-AD(0-14)
CA-MDI(0-7)
7A70-7A71
CA-MDO(0-7)
D22
A22
B22
B22
AK17
B03C STI7101: SDRAM
7AA1
EDD2516AETA
7AA2
EDD2516AETA
DDR SDRAM 16Mx16
LMI-D(0-31)
LMI-A(0-12)
LMI-CLK
U1
LMI-CLKnot
U2
LMI-CLKEN
Y5
Only for MPEG4
B03A STI7101: CONTROL
7A00
ST-7101BWC
B03C SDRAM
STI7101
B03B FLASH
B03D AV
AK6
TSIO-ST-CCLK
TSI1-ST-D(0-7)
TSI0-ST-D(0-7)
7A10-3
1
CPU-27MHZ
C1
7A12
27MHZ-3V3
E27
27M
ONLY FOR MPEG4
B03B STI7101: FLASH
7A50
M29W640FT70N6
FLASH EPROM 8Mx8 4Mx16
EMI-D(0-15)
EMI-A(1-22)
AH30
WP-FLASH-ST
MPEG
MPEG OUT SEE VIDEO
ONLY FOR MPEG4
B03F USB CONN.
1P07
1
2
3
4
USB 2.0 CONNECTOR SIDE
B09A USB 2.0
7N00
ISP1564HL
PCI HOST CONTROLLER
USB-OC
USB20-OC1
78
USB20-OC2
87
B04E
PCI-CLK-USB20_ETH
7
USB20-2-DM
90
USB20-2-DP
92
RESET-USB20
5
RESET-ETHERNET
B04E
75
1N01
12M
74
9
8
B04F PNX8541: CONTROL
PCI-AD(0-31)
B09B
PCI-REQ-PNX85XX
D21
B09B
PCI-GNT-PNX85XX
E21
PCI-REQ-USB20
E22
PCI-GNT-USB20
E20
MONITOR
M03D DP-RX
1M20
1
3
4
5
6
7
8
9
LIGHT-SENSOR
RC-IN
7F8J
LED2
30
TO 1M20
J
IR/LED
+3V3-STANDBY
7F8H
LED1
29
N.C.
+5V
N.C.
7F8G
LPC2103FBD48
MICRO CONTROLLER
32
45
11
1F8A
16M9
12
23
RESET
M03B
28
LVDS-ENABLE
M03A
35
LCD-PWR-ON
M01A M03A
36
UP-WC
M03B
41
ENABLE+3V3
M01A
46
BACKLIGHT-PWM-ANA-DISP
M03B
1
BACKLIGHT-BOOST
M03B
2
LAMP-ON
M03B
3
BACKLIGHT-OUT
M03B
6
UP-RESET
M03D
33
MONITOR+AUDIO-POWER
34
MONITOR+24V
38
MONITOR+3V3
39
MONITOR+12V
VOLTAGE DETECT
M03B DP RECEIVER & POWER SUPPPLY
7F0K
CDCE913R01PW
CLOCK SYNTHESIZER
1F0E
27M
1
14
11
GCLK
7F0A
GM68020H-BE
GENESIS
127
13
A-CLK
101
B-CLK
M03A DP-RX
7F00
EP2C5F256C7N
FPGA CYCLONE II
J16
H16
H15
H4
F4
C3
F1
DCLK
nCSO
ASDO
DATA0
E14
CLK0-PLL
H2
75A3
M25P10-AVMN6P
1M FLASH
6
1
5
2
B04D PNX 8541: MISCELLANEOUS
+3V3-STANDBY
7HD0
NCP303LSN
2
INP
OUTP
1
RESET-STBY
3
GND
B04A PNX 8541: STANDBY CONTROLLER
B01A
SUPPLY-FAULT
AB3
RESET-STBY-J
AA3
B04A
DETECT2
W1
B04A
DETECT1
W2
B04E
RESET-SYSTEM
AC3
B08A
AV1-BLK
AC1
B08A
AV2-BLK
AC2
B08A
AV1-STATUS
AF2
B08A
AV2-STATUS
AF1
KEYBOARD
AF4
LED1
AD3
LED2
AD2
RC
AA2
LIGHT-SENSOR
AF3
B01D LED PANEL CONTROL
1M20
9
N.C.
7
KEYBOARD
7U91
6
4
9U91
TO 1M01
E
KEYB.CONT
3
RC
5
+3V3-STANDBY
8
+5V
1
LIGHT-SENSOR
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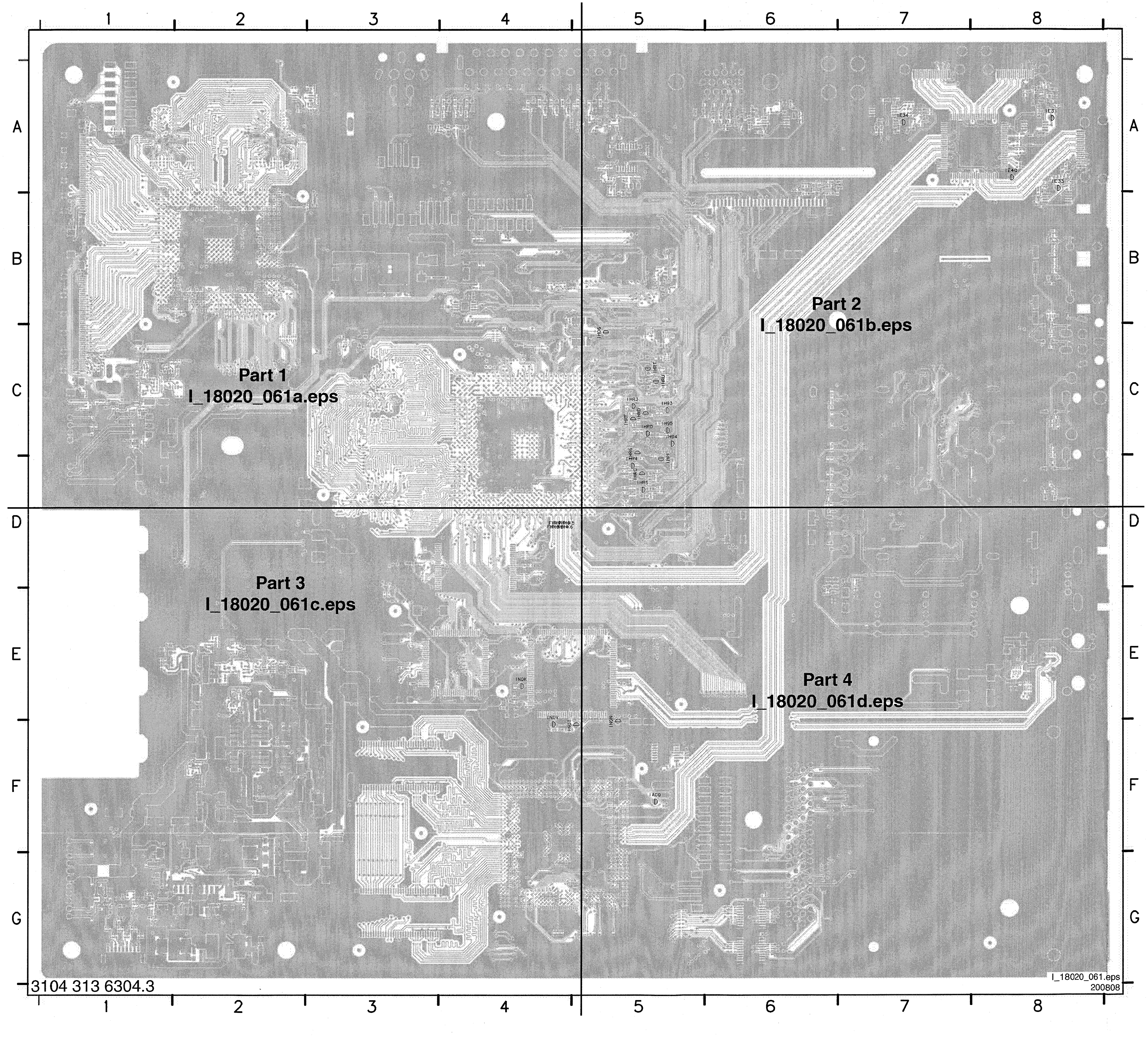
SSB: Test Points (Overview Top Side)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8
A
B
C
D
E
F
G
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Part 2
I_18020_061b.eps
Part 3
I_18020_061c.eps
Part 4
I_18020_061d.eps
3104 313 6304.3
I_18020_061.eps
200808

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I551	C5
I552	C5
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I554	C5
I556	C5
I557	C5
I558	C5
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IHRC	D5
IHRD	C5
IHRF	C5
IHRT	C5
IHRU	C5
IN0K	E4
IN0K	E4
IN0N	F5
IN0N	F5
IN0T	F4
IN0V	E4
IN0V	F4

SSB: Test Points (Overview Bottom Side)

A1	D3
A2	D3
A3	D2
A4	D2
A5	C4
F1	B5
F2	A5
F3	B6
F4	A3
F5	A6
F6	A3
F7	B5
F8	A5
F9	B6
I1	A4
I2	A4
I3	C1
I4	B1
I5	B1
I6	C1
I7	A4
I8	A4
I9	A5
F10	B5
F11	A5
F12	A6
F13	A1
F14	A2
F15	B1
F16	A3
F17	A5
F18	B3
F19	A2
F20	A3
F21	B3
F22	A1
F23	A2
F24	A2
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F26	A4
F27	A4
F28	A4
F29	B3
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F32	A1
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F35	B1
F36	A5
F37	A5
F38	B3
F39	A5
F40	A5
F41	A3
F42	A5
F43	A5
F44	A6
F45	A6
F46	A2
F47	A4
F48	B3
F49	A3
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F79	C1
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F83	C1
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F94	B3
F95	B3
F96	B3
F97	B3
F98	A4
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I12	A5
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I14	A5
I15	A6
I16	A5
I17	A5
I18	A1
I19	A4
I20	A4
I21	A6
I22	B6
I23	B6
I24	B6
I25	A6
I26	A6
I27	A5
I28	A4
I29	B5
I30	B4
I31	B6
I32	A6
I33	A4
I34	B1
I35	A3
I36	B1
I37	A4
I38	A3
I39	A2
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I64	A2
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I66	A2
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I72	A5
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I81	E7
I82	E7
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I94	E7
I95	E7
I96	F7
I97	F7
I98	F7
I99	E7
AHF0	C4
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AT51	D2
AT62	D3
AT63	D3
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F103	B3
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F169	C2
F170	D1
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F172	D2
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F176	C2
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F180	D3
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F228	C6
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F236	C4
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F252	B7
F253	C7
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FE99	B6
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FEB3	A3
FEB9	A5
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FH02	C4
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FHPE	C4
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FHR4	D5
FHR5	D4
FHR6	D4
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FN0A	E5
FN0B	E5
FN0C	E4
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FT12	D2
FT13	D1
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FT17	D1
FT18	C3
FT19	C3
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I252	D1
I253	D1
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I327	D4
I328	D4
I329	D4
I330	C4
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I332	C4
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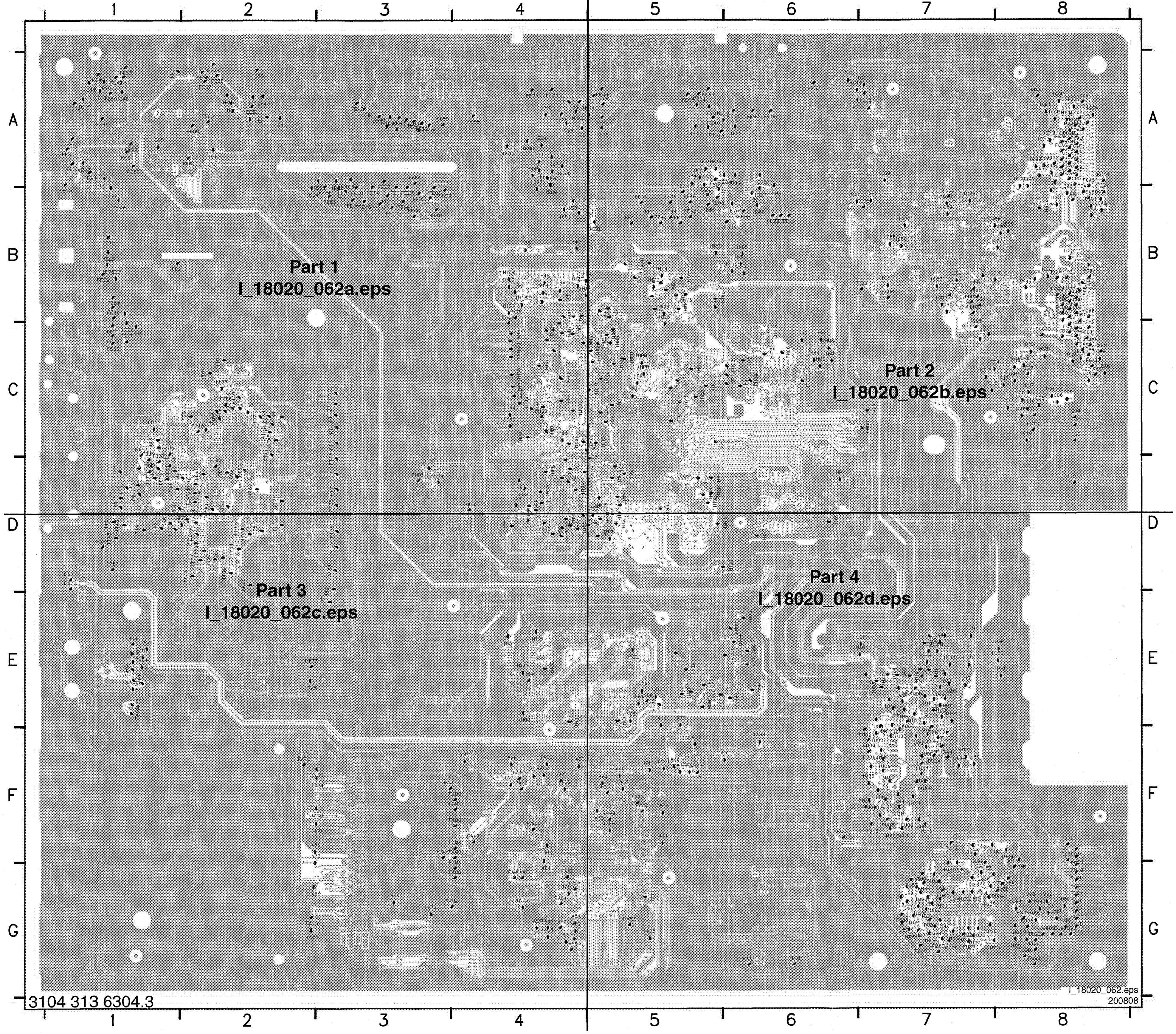
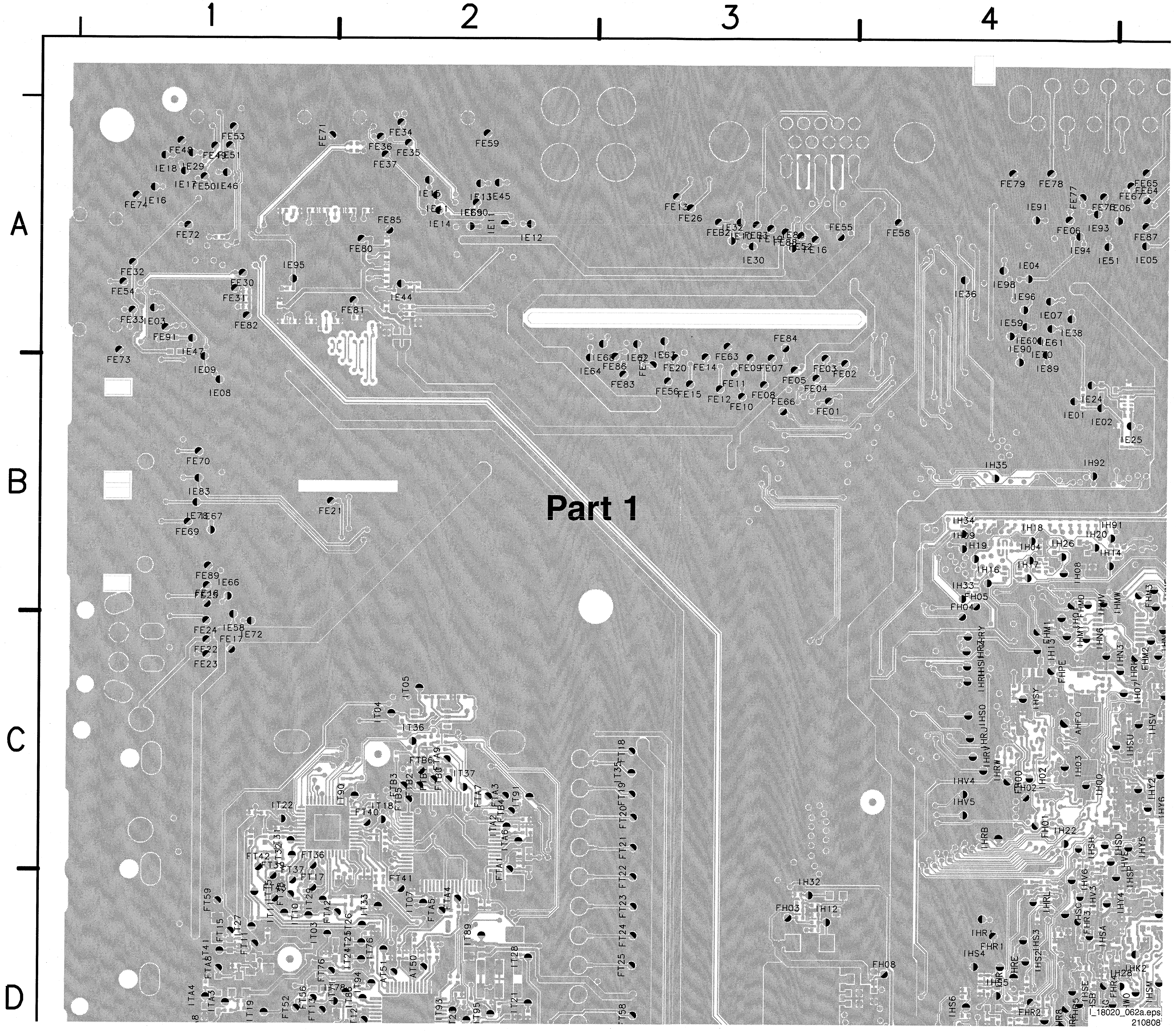


SSB: Test Points (Part 1 Bottom Side)


1
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A
B
C
D
Part 1
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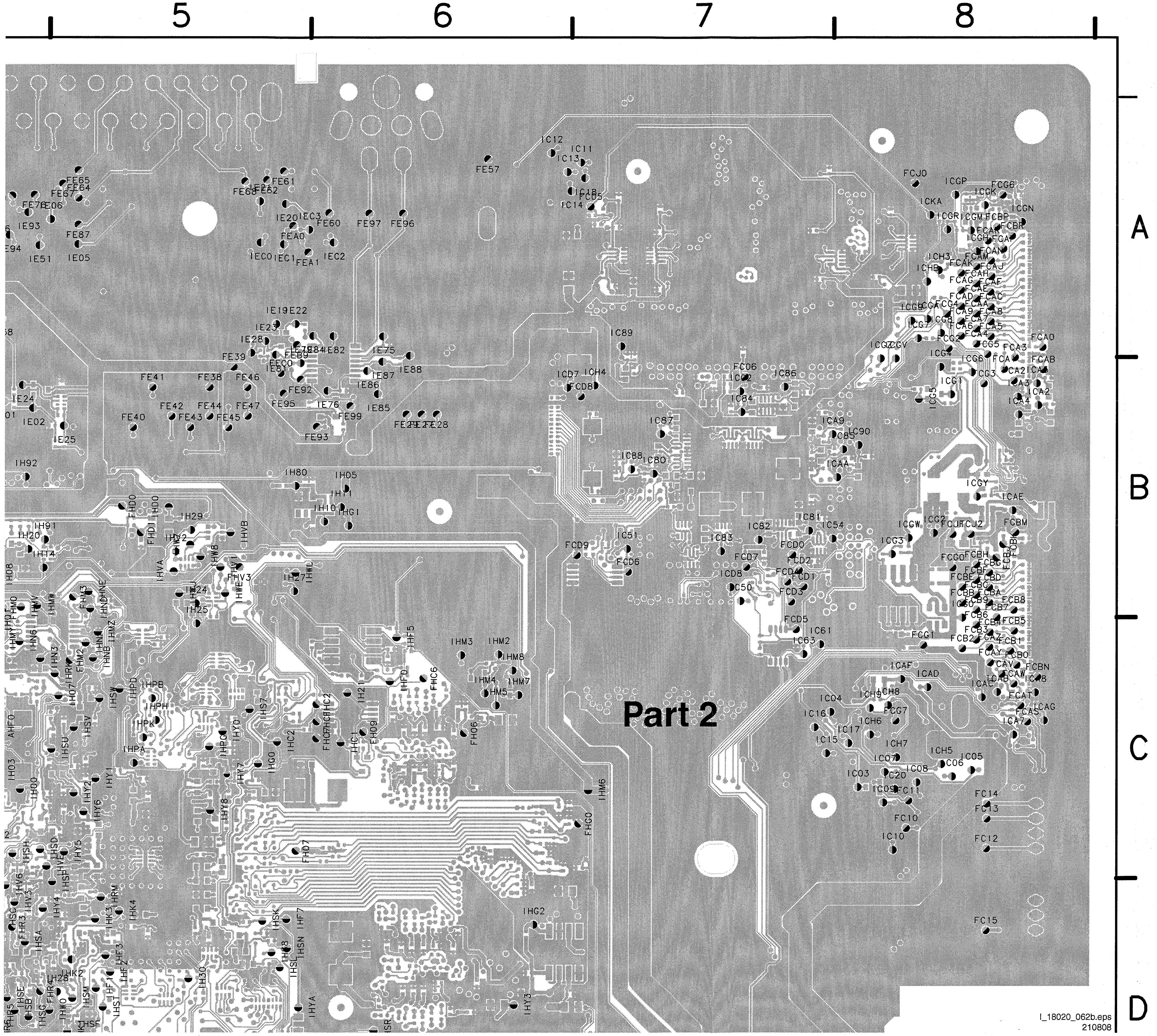
SSB: Test Points (Part 2 Bottom Side)


5
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A
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C
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IE06
IE93
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IE05
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IH27
IH24
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I_18020_062b.eps
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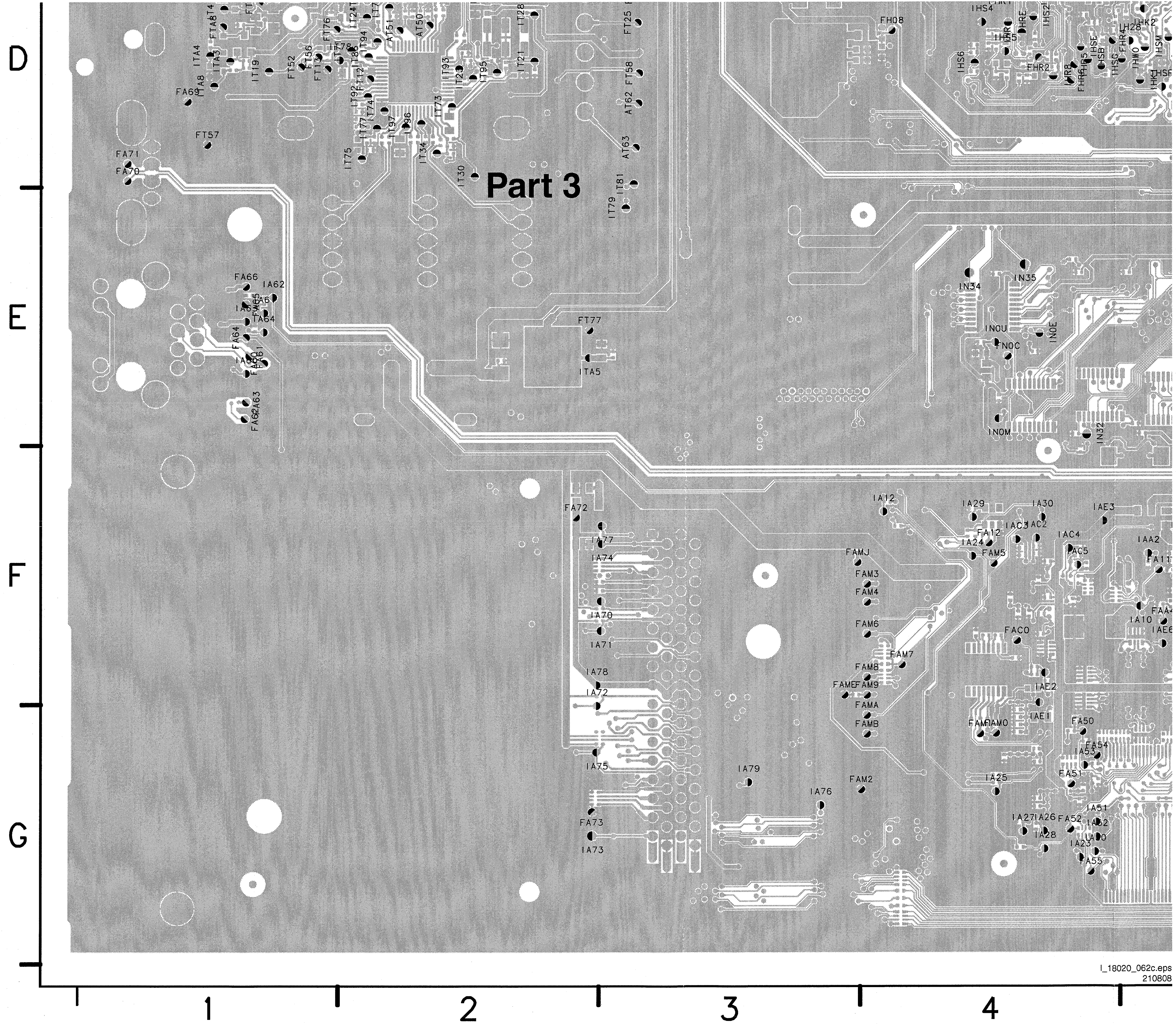
SSB: Test Points (Part 3 Bottom Side)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F
G
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FT77
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IA75
FA73
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IA76
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IA12
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FAM7
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FAMB
FAMO
IA29
IA30
IAE3
FA12
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IAC4
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IA10
FAA4
IAE6
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IA53
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IA51
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IA52
IA28
IA23
FA55
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IN35
INOU
INOC
INOE
INOM
IN32
FH08
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FHR2
IHK2
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IT81
AT63
AT62
FT58
FT25
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IT28
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IT96
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IT18
AT50
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ITA3
ITA4
IA8

I_18020_062c.eps
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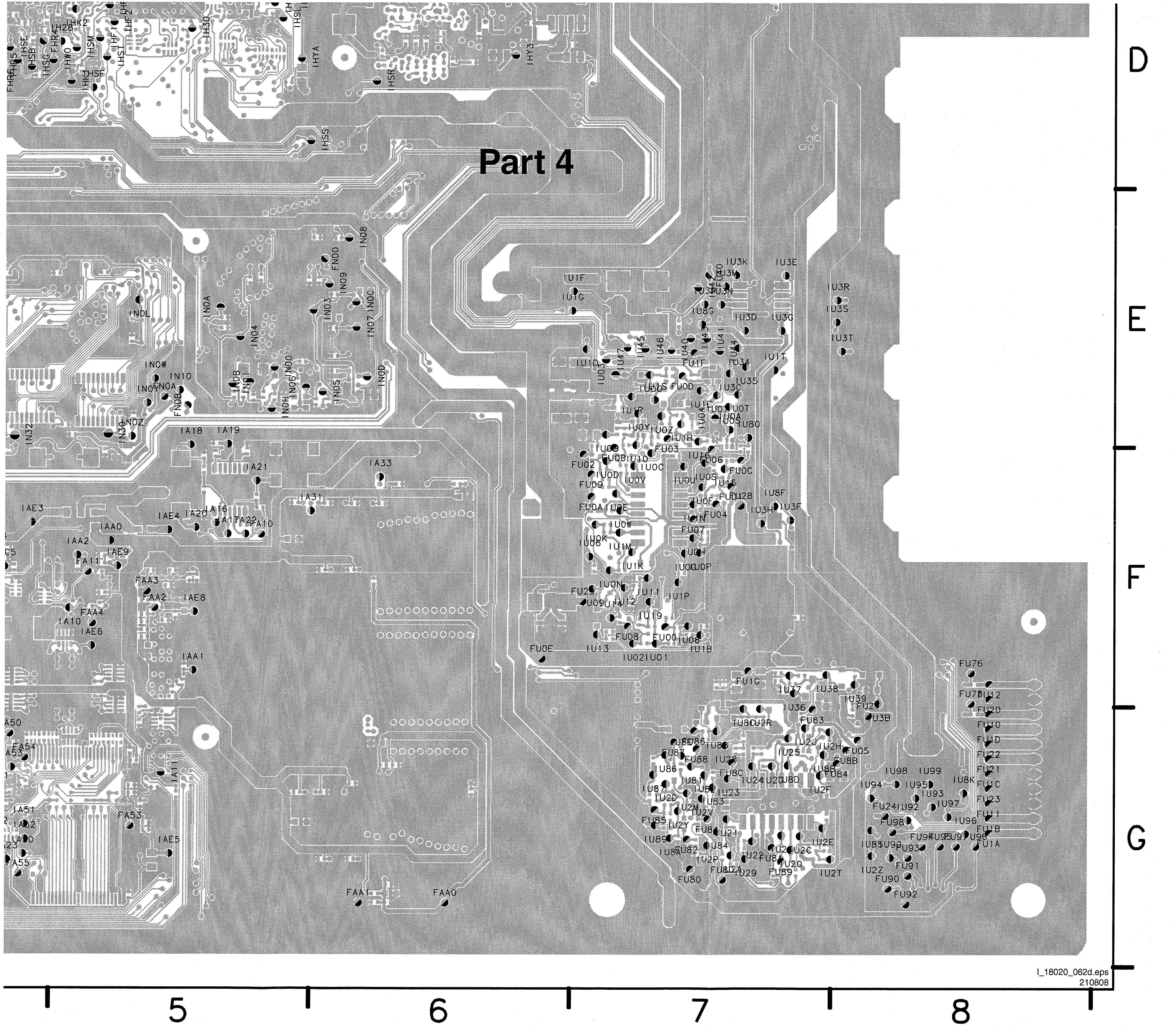
SSB: Test Points (Part 4 Bottom Side)


Part 4
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G
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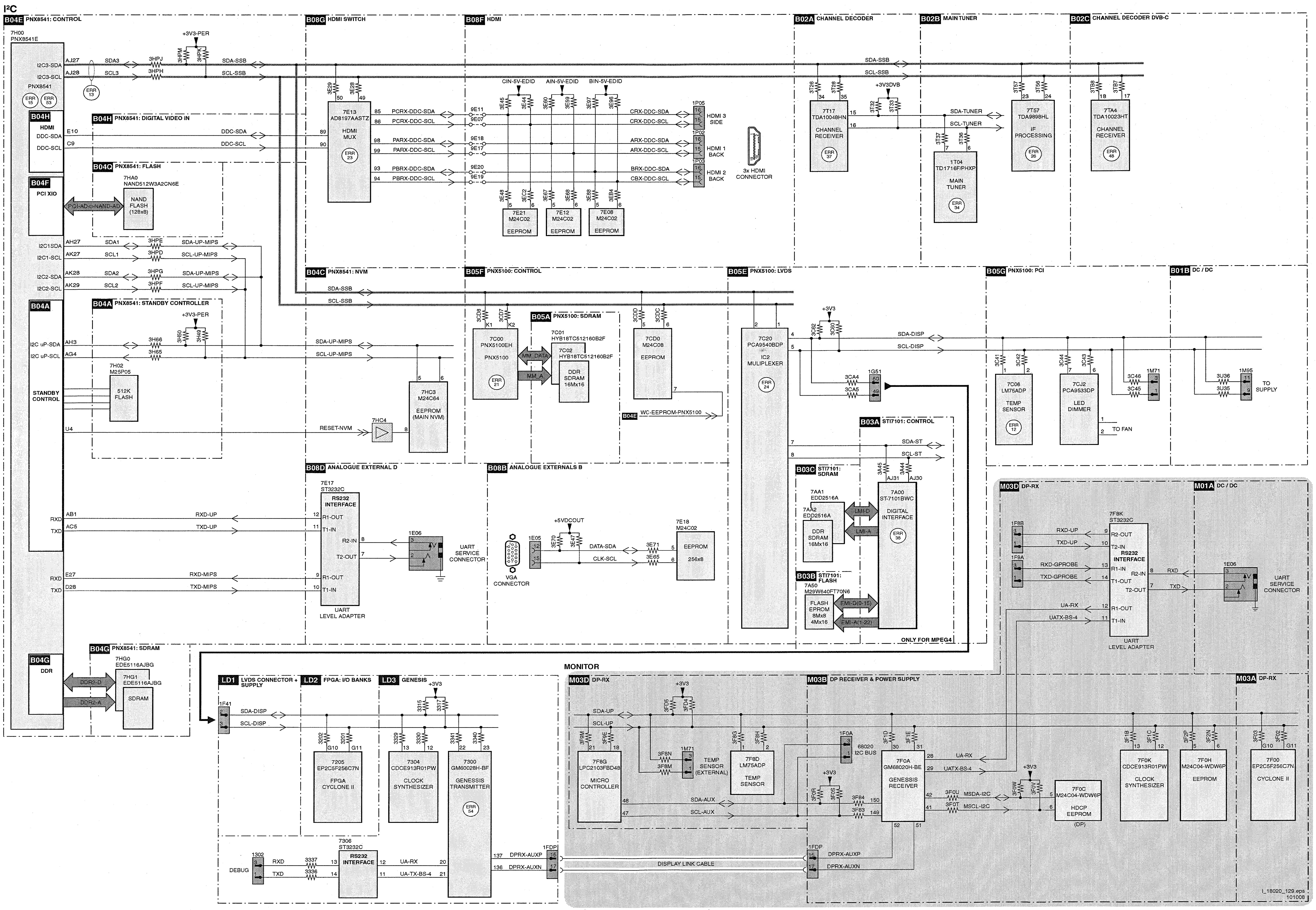
I2C IC Overview


I²C
B04E PNX8541: CONTROL
7H00
PNX8541E
I2C3-SDA
I2C3-SCL
PNX8541
ERR 15
ERR 53
ERR 13
AJ27
AJ28
SDA3
SCL3
3HPJ
3HPH
3HPM
3HPK
+3V3-PER
SDA-SSB
SCL-SSB
B04H HDMI
DDC-SDA
DDC-SCL
E10
C9
B04H PNX8541: DIGITAL VIDEO IN
B04F PCI XIO
B04Q PNX8541: FLASH
7HA0
NAND512W3A2CN6E
NAND FLASH (128x8)
PCI-AD<>NAND-AD
I2C1SDA
I2C1-SCL
I2C2-SDA
I2C2-SCL
AH27
AK27
AK28
AK29
SDA1
SCL1
SDA2
SCL2
3HPE
3HPD
3HPG
3HPF
SDA-UP-MIPS
SCL-UP-MIPS
B04A
B04A PNX8541: STANDBY CONTROLLER
+3V3-PER
3H50
3H49
3H66
3H65
I2C uP-SDA
I2C uP-SCL
AH3
AG4
7H02
M25P05
512K FLASH
STANDBY CONTROL
U4
RESET-NVM
7HC4
RXD
TXD
AB1
AC5
RXD-UP
TXD-UP
RXD
TXD
E27
D28
RXD-MIPS
TXD-MIPS
B04G DDR
B04G PNX8541: SDRAM
7HG0
EDE5116AJBG
7HG1
EDE5116AJBG
SDRAM
DDR2-D
DDR2-A
B08G HDMI SWITCH
3E29
3E28
7E13
AD8197AASTZ
HDMI MUX
ERR 23
CIN-5V-EDID
AIN-5V-EDID
BIN-5V-EDID
PCRX-DDC-SDA
PCRX-DDC-SCL
PARX-DDC-SDA
PARX-DDC-SCL
PBRX-DDC-SDA
PBRX-DDC-SCL
B08F HDMI
9E11
9E07
9E18
9E17
9E20
9E19
CRX-DDC-SDA
CRX-DDC-SCL
ARX-DDC-SDA
ARX-DDC-SCL
BRX-DDC-SDA
CBX-DDC-SCL
1P05
HDMI 3 SIDE
1P02
HDMI 1 BACK
1P03
HDMI 2 BACK
3x HDMI CONNECTOR
7E21 M24C02 EEPROM
7E12 M24C02 EEPROM
7E08 M24C02 EEPROM
B04C PNX8541: NVM
SDA-SSB
SCL-SSB
SDA-UP-MIPS
SCL-UP-MIPS
7HC3
M24C64
EEPROM (MAIN NVM)
B05F PNX5100: CONTROL
3CD8
3CD7
7C00
PNX5100EH
PNX5100
ERR 21
B05A PNX5100: SDRAM
7C01
HYB18TC512160B2F
7C02
HYB18TC512160B2F
DDR SDRAM 16Mx16
MM_DATA
MM_A
3CDD
3CDC
7CD0
M24C08
EEPROM
B04E WC-EEPROM-PNX5100
B02A CHANNEL DECODER
3T26
3T28
7T17
TDA10048HN
CHANNEL RECEIVER
ERR 37
+3V3DVB
3T32
3T33
B02B MAIN TUNER
SDA-TUNER
SCL-TUNER
3T37
3T36
1T04
TD1716F/PHXP
MAIN TUNER
ERR 34
3T57
3T56
7T57
TDA9898HL
IF PROCESSING
ERR 26
B02C CHANNEL DECODER DVB-C
3TB8
3TB7
7TA4
TDA10023HT
CHANNEL RECEIVER
ERR 48
B05E PNX5100: LVDS
+3V3
3C62
3C60
7C20
PCA9540BDP
I2C MULIPLEXER
ERR 24
3CA4
3CA5
1G51
SDA-DISP
SCL-DISP
B05G PNX5100: PCI
3C41
3C42
7C06
LM75ADP
TEMP SENSOR
ERR 12
3C44
3C43
7CJ2
PCA9533DP
LED DIMMER
TO FAN
3C46
3C45
1M71
B01B DC / DC
3U36
3U35
1M95
TO SUPPLY
B03A STI7101: CONTROL
SDA-ST
SCL-ST
3A45
3A44
AJ31
AJ30
B03C STI7101: SDRAM
7AA1
EDD2516A
7AA2
EDD2516A
DDR SDRAM 16Mx16
LMI-D
LMI-A
7A00
ST-7101BWC
DIGITAL INTERFACE
ERR 38
B03B STI7101: FLASH
7A50
M29W640FT70N6
FLASH EPROM 8Mx8 4Mx16
EMI-D(0-15)
EMI-A(1-22)
ONLY FOR MPEG4
B08D ANALOGUE EXTERNAL D
7E17
ST3232C
RS232 INTERFACE
R1-OUT
T1-IN
R2-IN
T2-OUT
R1-OUT
T1-IN
UART LEVEL ADAPTER
1E06
UART SERVICE CONNECTOR
B08B ANALOGUE EXTERNALS B
+5VDCOUT
1E05
3E70
3E47
DATA-SDA
CLK-SCL
3E71
3E65
VGA CONNECTOR
7E18
M24C02
EEPROM 256x8
M03D DP-RX
1F8B
1F9A
RXD-UP
TXD-UP
RXD-GPROBE
TXD-GPROBE
UA-RX
UATX-BS-4
M01A DC / DC
7F8K
ST3232C
RS232 INTERFACE
R2-OUT
T2-IN
R1-IN
R2-IN
T1-OUT
T2-OUT
R1-OUT
T1-IN
UART LEVEL ADAPTER
RXD
TXD
1E06
UART SERVICE CONNECTOR
MONITOR
LD1 LVDS CONNECTOR + SUPPLY
1F41
SDA-DISP
SCL-DISP
LD2 FPGA: I/O BANKS
3202
3201
7205
EP2C5F256C7N
FPGA CYCLONE II
LD3 GENESIS
+3V3
3315
3317
3329
3330
7304
CDCE913R01PW
CLOCK SYNTHESIZER
3341
3340
7300
GM60028H-BF
GENESSIS TRANSMITTER
ERR 54
7306
ST3232C
RS232 INTERFACE
1302
DEBUG
RXD
TXD
3337
3336
UA-RX
UA-TX-BS-4
DPRX-AUXP
DPRX-AUXN
1FDP
DISPLAY LINK CABLE
M03D DP-RX
+3V3
3FD5
3FD4
SDA-UP
SCL-UP
3F9M
3F9E
7F8G
LPC2103FBD48
MICRO CONTROLLER
3F8N
3F8M
1M71
TEMP SENSOR (EXTERNAL)
3F9G
3F9H
7F8D
LM75ADP
TEMP SENSOR
SDA-AUX
SCL-AUX
M03B DP RECEIVER & POWER SUPPLY
1F0A
68020 I2C BUS
+3V3
3F0R
3F0S
3F84
3F83
3F1D
3F1E
7F0A
GM68020H-BE
GENESSIS RECEIVER
UA-RX
UATX-BS-4
3F0U
3F0T
MSDA-I2C
MSCL-I2C
+3V3
3F0W
3F0V
7F0C
M24C04-WDW6P
HDCP EEPROM (DP)
1FDP
DPRX-AUXP
DPRX-AUXN
3F1B
3F1C
7F0K
CDCE913R01PW
CLOCK SYNTHESIZER
3F2P
3F2N
7F0H
M24C04-WDW6P
EEPROM
M03A DP-RX
3F03
3F02
7F00
EP2C5F256C7N
CYCLONE II
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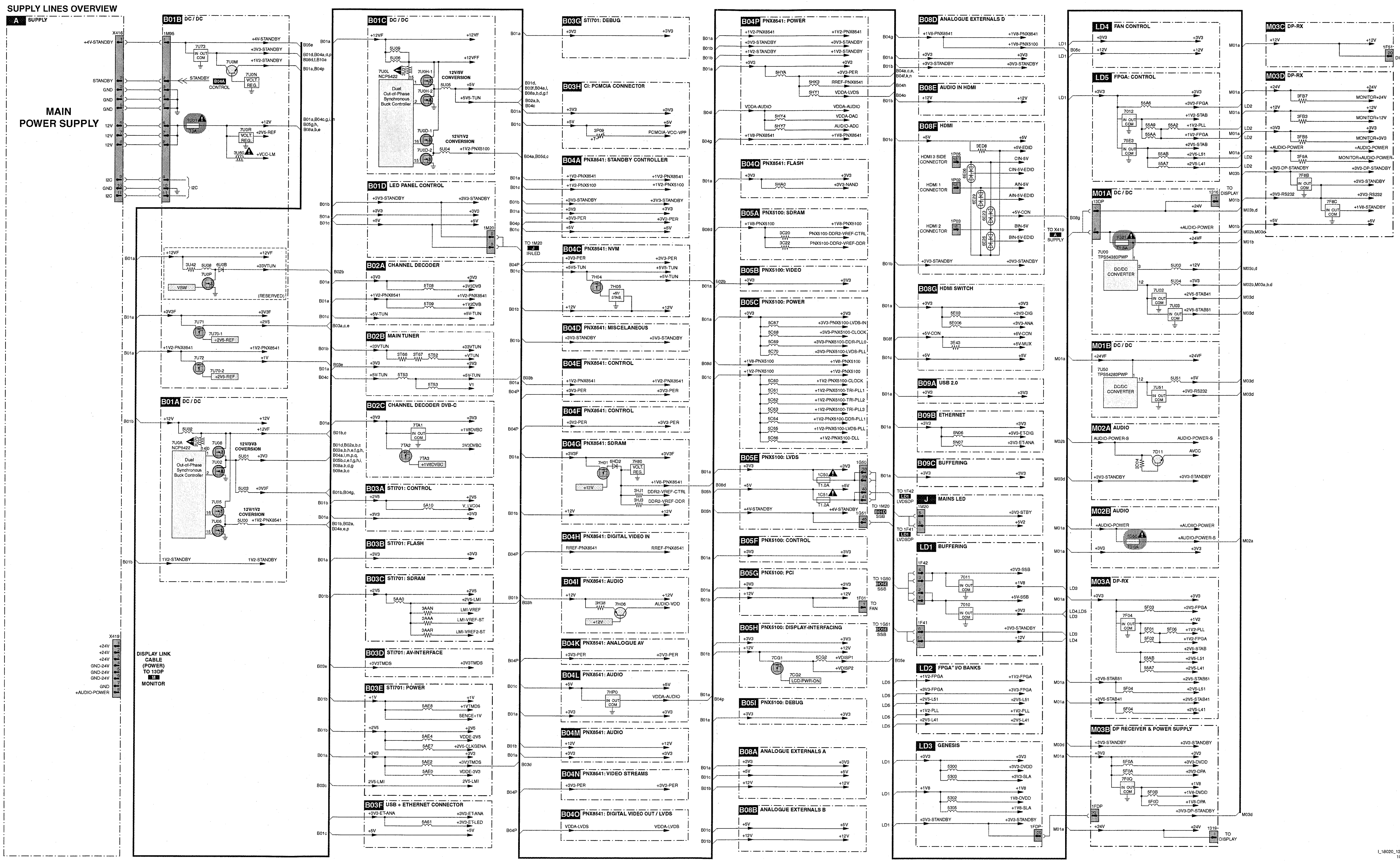
Supply Lines Overview


SUPPLY LINES OVERVIEW
A SUPPLY
MAIN POWER SUPPLY
DISPLAY LINK CABLE (POWER) TO 13DP M MONITOR
B01B DC / DC
B01A DC / DC
B01C DC / DC
B01D LED PANEL CONTROL
B02A CHANNEL DECODER
B02B MAIN TUNER
B02C CHANNEL DECODER DVB-C
B03A STI701: CONTROL
B03B STI701: FLASH
B03C STI701: SDRAM
B03D STI701: AV-INTERFACE
B03E STI701: POWER
B03F USB + ETHERNET CONNECTOR
B03G STI701: DEBUG
B03H CI: PCMCIA CONNECTOR
B04A PNX8541: STANDBY CONTROLLER
B04C PNX8541: NVM
B04D PNX8541: MISCELANEOUS
B04E PNX8541: CONTROL
B04F PNX8541: CONTROL
B04G PNX8541: SDRAM
B04H PNX8541: DIGITAL VIDEO IN
B04I PNX8541: AUDIO
B04K PNX8541: ANALOGUE AV
B04L PNX8541: AUDIO
B04M PNX8541: AUDIO
B04N PNX8541: VIDEO STREAMS
B04O PNX8541: DIGITAL VIDEO OUT / LVDS
B04P PNX8541: POWER
B04Q PNX8541: FLASH
B05A PNX5100: SDRAM
B05B PNX5100: VIDEO
B05C PNX5100: POWER
B05E PNX5100: LVDS
B05F PNX5100: CONTROL
B05G PNX5100: PCI
B05H PNX5100: DISPLAY-INTERFACING
B05I PNX5100: DEBUG
B08A ANALOGUE EXTERNALS A
B08B ANALOGUE EXTERNALS B
B08D ANALOGUE EXTERNALS D
B08E AUDIO IN HDMI
B08F HDMI
B08G HDMI SWITCH
B09A USB 2.0
B09B ETHERNET
B09C BUFFERING
J MAINS LED
LD1 BUFFERING
LD2 FPGA" I/O BANKS
LD3 GENESIS
LD4 FAN CONTROL
LD5 FPGA: CONTROL
M01A DC / DC
M01B DC / DC
M02A AUDIO
M02B AUDIO
M03A DP-RX
M03B DP RECEIVER & POWER SUPPLY
M03C DP-RX
M03D DP-RX
TO DISPLAY

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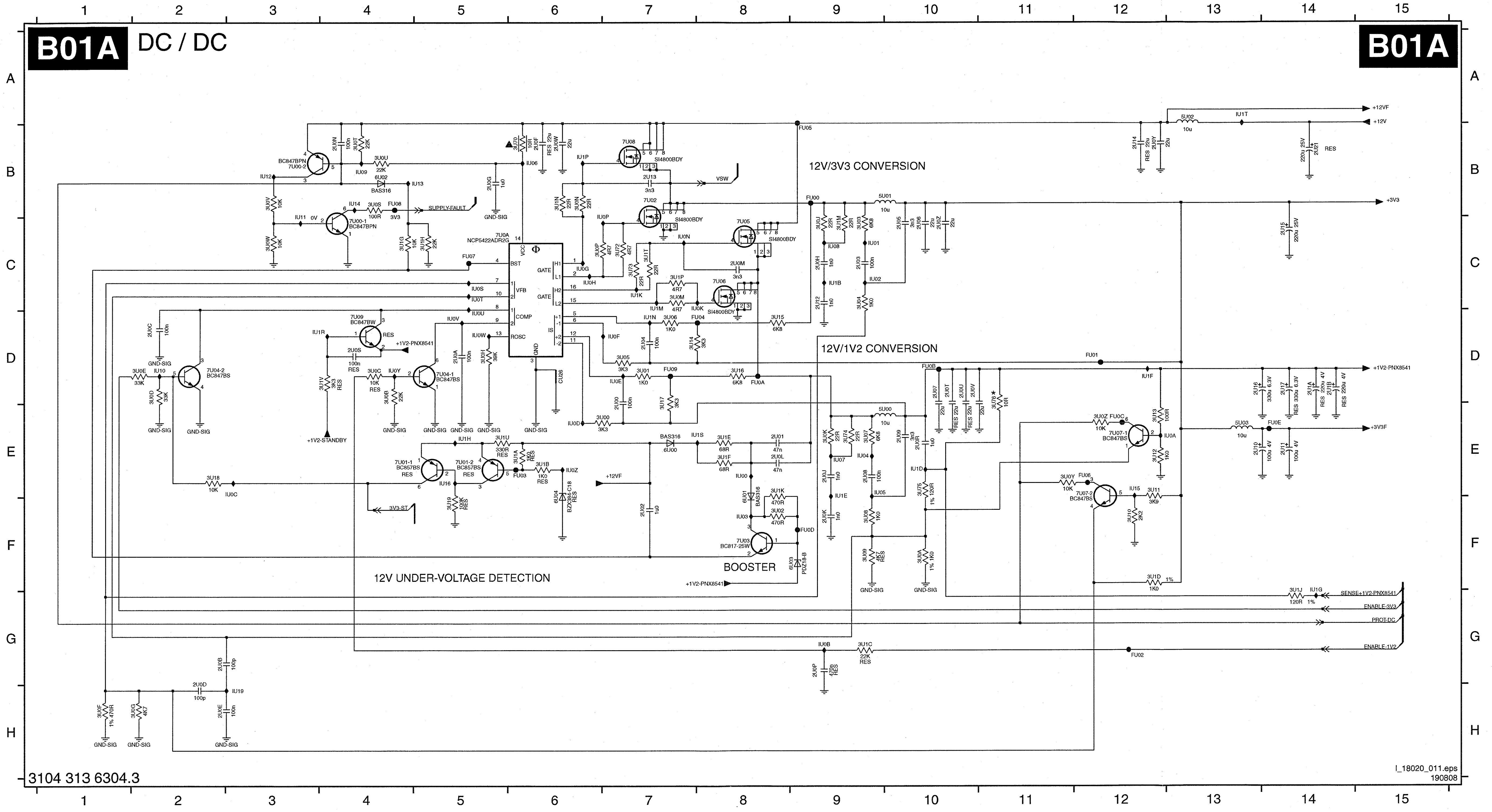
7. Circuit Diagrams and PWB Layouts

SSB: DC / DC

2U00	D7
2U01	E8
2U02	F7
2U03	C9
2U04	D7
2U05	C10
2U06	C10
2U07	D10
2U08	E9
2U09	E10
2U0A	D5
2U0B	G2
2U0C	D2
2U0D	H2
2U0E	H2
2U0F	B6
2U0G	B5
2U0H	C9
2U0J	E9
2U0K	F9
2U0L	E8
2U0M	C8
2U0N	B4
2U0P	G9
2U0R	E10
2U0S	D4
2U0T	D10
2U0U	D10
2U0V	D10
2U0W	B6
2U0Y	B12
2U0Z	C10
2U10	E13
2U11	E14
2U12	C9
2U13	B7
2U14	B12
2U15	C14
2U16	D13
2U17	D14
2U1A	D14
2U1B	D14
2U21	B14
3U00	E7
3U01	D7
3U02	F8
3U03	C9
3U04	C9
3U05	D7
3U06	D7
3U07	E9
3U08	F9
3U09	F9
3U0A	F10
3U0B	D4
3U0C	D4
3U0D	D2
3U0E	D2
3U0F	H1
3U0G	H2
3U0H	D5
3U0J	C9
3U0K	E9
3U0M	C7
3U0N	B6
3U0P	C6
3U0S	B4
3U0T	B4
3U0U	B4
3U0V	B3
3U0W	C3
3U0Y	E11
3U0Z	E12
3U10	F12
3U11	E12
3U12	E12
3U13	E12
3U14	D7
3U15	D8
3U16	D8
3U17	D7
3U18	E2
3U19	F5
3U1A	E6
3U1B	E6
3U1C	G9
3U1D	F12
3U1E	E8
3U1F	E8
3U1G	C4
3U1H	C5
3U1J	G14
3U1K	E8
3U1M	C9
3U1N	B6
3U1P	C7
3U1T	C7
3U1U	E5
3U1V	D4
3U70	B6
3U72	C7
3U73	C7
3U74	E9
3U75	E10
3U76	D11
5U00	E10
5U01	B10
5U02	A13
5U03	E13
6U00	E7
6U01	E8
6U02	B4
6U03	F9
6U04	E6
7U00-1	C4
7U00-2	B3
7U01-1	E4
7U01-2	E5
7U02	B7
7U03	F8
7U04-1	D5
7U04-2	D2
7U05	C8
7U06	C8
7U07-1	E12
7U07-2	E12
7U08	B7
7U09	D4
7U0A	C6
CU26	D6
FU00	B9
FU01	D12
FU02	G12
FU03	E6
FU04	D8
FU05	B9
FU06	E12
FU07	C5
FU08	B4
FU09	D7
FU0A	D8
FU0B	D10
FU0C	E12
FU0D	F9
FU0E	E14
IU00	E8
IU01	C9
IU02	C9
IU03	F8
IU04	E9
IU05	E9
IU06	B6
IU07	E9
IU08	C9
IU09	B4
IU0A	E13
IU0B	G9
IU0C	E3
IU0D	E6
IU0E	D7
IU0F	D7
IU0G	C6
IU0H	C6
IU0K	C8
IU0N	C7
IU0P	B7
IU0S	C5
IU0T	C5
IU0U	D5
IU0V	D5
IU0W	D5
IU0Y	D4
IU0Z	E6
IU10	D2
IU11	B3
IU12	B3
IU13	B5
IU14	B4
IU15	E12
IU16	E5
IU19	H3
IU1B	C9
IU1D	E10
IU1E	E9
IU1F	D12
IU1G	F14
IU1H	E5
IU1K	C7
IU1M	C7
IU1N	D7
IU1P	B6
IU1R	D3
IU1S	E8
IU1T	A13


B01A
DC / DC
B01A
12V/3V3 CONVERSION
12V/1V2 CONVERSION
12V UNDER-VOLTAGE DETECTION
BOOSTER
+12VF
+12V
+3V3
+1V2-PNX8541
+3V3F
SENSE+1V2-PNX8541
ENABLE-3V3
PROT-DC
ENABLE-1V2
SUPPLY-FAULT
VSW
3V3-ST
+1V2-STANDBY
+12VF
+1V2-PNX8541
7U0A
NCP5422ADR2G
VCC
BST
GATE
H1
L1
VFB
COMP
ROSC
GATE
H2
L2
IS
GND
7U08
SI4800BDY
7U02
SI4800BDY
7U05
SI4800BDY
7U06
SI4800BDY
7U00-2
BC847BPN
7U00-1
BC847BPN
7U09
BC847BW
7U04-1
BC847BS
7U04-2
BC847BS
7U01-1
BC857BS
7U01-2
BC857BS
7U03
BC817-25W
7U07-1
BC847BS
7U07-2
BC847BS
6U02
BAS316
6U00
BAS316
6U01
BAS316
6U04
BZX384-C18
6U03
PDZ18-B
5U01
10u
5U02
10u
5U00
10u
5U03
10u
3U70
10R
3U0U
22K
3U0T
22K
2U0N
100n
2U0F
RES 22u
2U0W
22u
2U0G
1u0
3U0S
100R
3U1N
22R
3U0N
22R
3U0P
4R7
3U72
4R7
3U73
22R
3U1T
22R
3U1P
4R7
3U0M
4R7
2U13
3n3
2U0M
3n3
3U06
1K0
3U15
6K8
3U05
3K3
3U01
1K0
3U16
6K8
3U00
3K3
3U14
3K3
3U17
3K3
2U04
100n
2U00
100n
3U0J
22R
3U1M
22R
3U03
6K8
2U05
3n3
2U06
22u
2U0Z
22u
2U0H
1n0
2U12
1n0
2U03
100n
3U04
1K0
2U14
RES 22u
2U0Y
22u
2U21
220u 25V
RES
2U15
220u 25V
2U07
22u
2U0T
RES 22u
2U0U
RES 22u
2U0V
22u
3U76 *
10R
3U13
100R
3U12
1K0
2U16
330u 6.3V
2U17
RES 330u 6.3V
2U1A
RES 220u 4V
2U1B
RES 220u 4V
2U10
100u 4V
2U11
100u 4V
3U0Z
10K
3U0Y
10K
3U11
3K9
3U10
2K2
3U1D
1K0
1%
3U1J
120R
1%
3U0K
22R
3U74
22R
3U07
6K8
2U09
3n3
2U0R
1u0
2U0J
1n0
2U08
100n
2U0K
1n0
3U08
1K0
3U09
4K7
RES
3U75
1% 120R
3U0A
1% 1K0
3U1C
22K
RES
2U0P
470n
RES
3U1E
68R
3U1F
68R
2U01
47n
2U0L
47n
3U1K
470R
3U02
470R
2U02
1u0
3U1U
330R
RES
3U1A
1K0
RES
3U1B
1K0
RES
3U19
100K
RES
3U18
10K
3U0E
33K
3U0D
33K
2U0C
100n
3U0V
10K
3U0W
10K
3U1G
10K
3U1H
22K
2U0S
100n
RES
3U1V
3K3
RES
3U0C
10K
RES
3U0B
22K
2U0A
100n
3U0H
39K
CU26
2U0B
100p
2U0D
100p
2U0E
100n
3U0F
1% 470R
3U0G
4K7
GND-SIG
FU00
FU01
FU02
FU03
FU04
FU05
FU06
FU07
FU08
FU09
FU0A
FU0B
FU0C
FU0D
FU0E
0V
3V3
3104 313 6304.3
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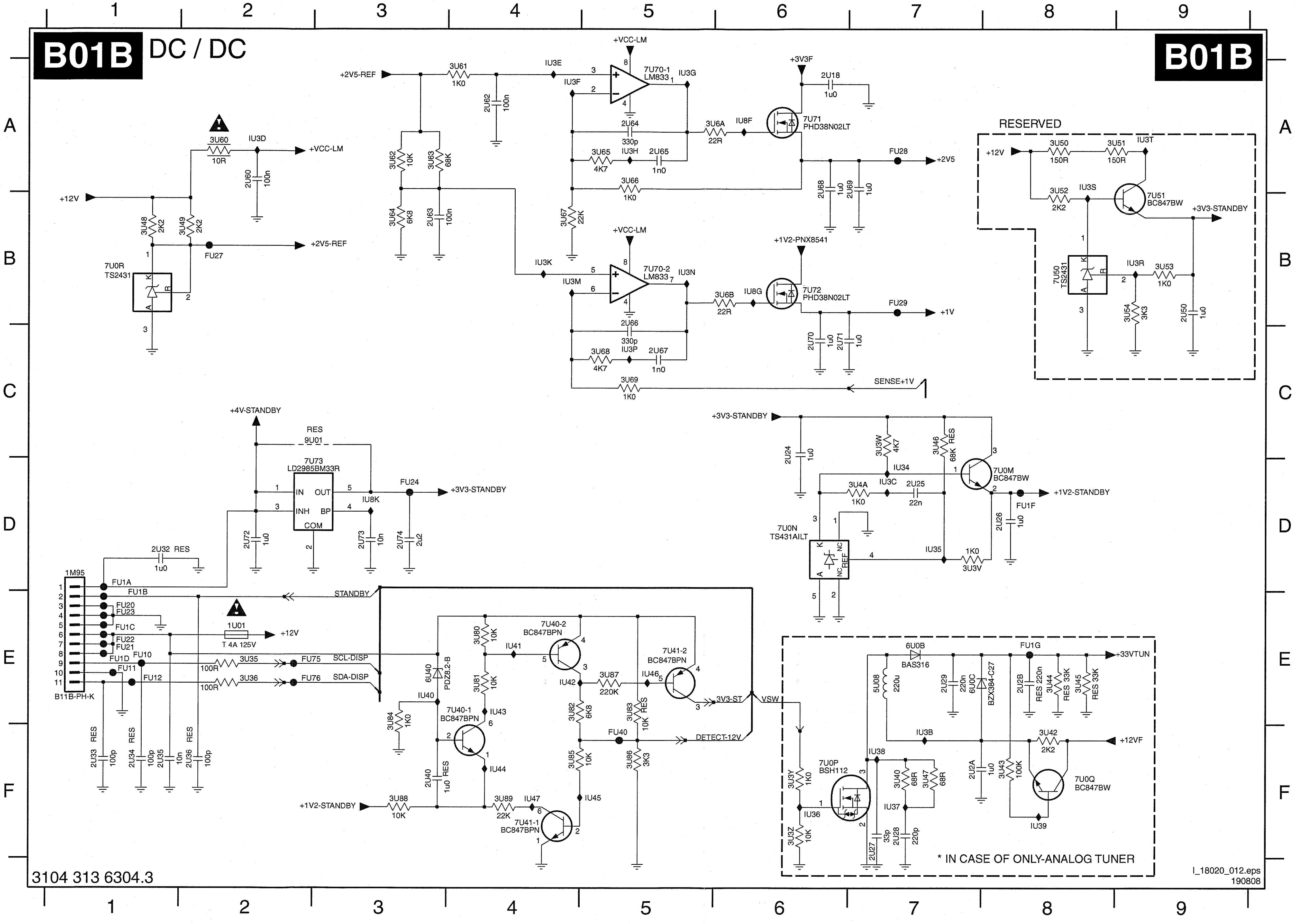
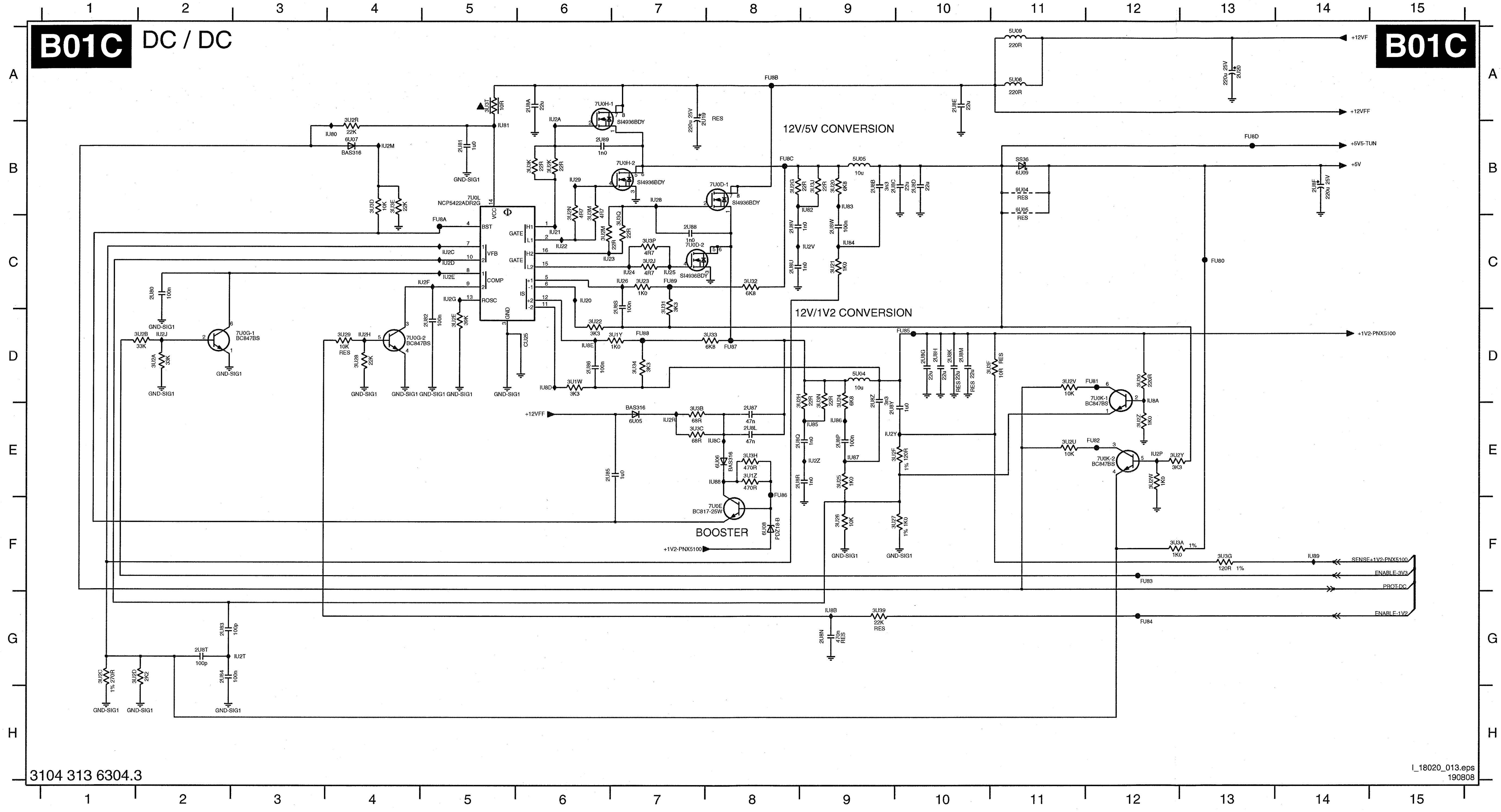
SSB: DC / DC


B01B
DC / DC
B01B
+2V5-REF
3U61
1K0
IU3E
+VCC-LM
7U70-1
LM833
IU3G
IU3F
2U62
100n
3U62
10K
3U63
68K
3U64
6K8
2U63
100n
2U64
330p
3U65
4K7
IU3H
2U65
1n0
3U66
1K0
3U67
22K
3U6A
22R
IU8F
+3V3F
2U18
1u0
7U71
PHD38N02LT
FU28
+2V5
2U68
1u0
2U69
1u0
3U60
10R
IU3D
+VCC-LM
2U60
100n
+12V
3U48
2K2
3U49
2K2
FU27
+2V5-REF
7U0R
TS2431
IU3K
IU3M
7U70-2
LM833
IU3N
+1V2-PNX8541
3U6B
22R
IU8G
7U72
PHD38N02LT
FU29
+1V
2U70
1u0
2U71
1u0
2U66
330p
3U68
4K7
IU3P
2U67
1n0
3U69
1K0
SENSE+1V
RESERVED
+12V
3U50
150R
3U51
150R
IU3T
3U52
2K2
IU3S
7U51
BC847BW
+3V3-STANDBY
7U50
TS2431
IU3R
3U53
1K0
3U54
3K3
2U50
1u0
+4V-STANDBY
RES
9U01
7U73
LD2985BM33R
IN
OUT
INH
BP
COM
FU24
+3V3-STANDBY
IU8K
2U72
1u0
2U73
10n
2U74
2u2
2U32 RES
1u0
1M95
FU1A
FU1B
FU20
FU23
FU1C
FU22
FU21
FU10
FU1D
FU11
FU12
B11B-PH-K
STANDBY
1U01
T 4A 125V
+12V
3U35
100R
FU75
SCL-DISP
3U36
100R
FU76
SDA-DISP
2U33
RES
100p
2U34
RES
100p
2U35
10n
2U36
RES
100p
+3V3-STANDBY
2U24
1u0
3U3W
4K7
3U46
RES
68K
IU34
7U0M
BC847BW
3U4A
1K0
IU3C
2U25
22n
+1V2-STANDBY
FU1F
2U26
1u0
7U0N
TS431AILT
IU35
1K0
3U3V
3U80
10K
7U40-2
BC847BPN
7U41-2
BC847BPN
IU41
6U40
PDZ8.2-B
IU42
3U87
220K
IU46
3U81
10K
IU43
IU40
3U84
1K0
7U40-1
BC847BPN
3U82
6K8
3U83
RES
10K
3V3-ST
VSW
FU40
DETECT-12V
IU44
2U40
RES
1u0
3U85
10K
3U86
3K3
IU45
+1V2-STANDBY
3U88
10K
3U89
22K
IU47
7U41-1
BC847BPN
6U0B
BAS316
FU1G
+33VTUN
5U08
220u
2U29
220n
6U0C
BZX384-C27
2U2B
RES 220n
3U44
RES 33K
3U45
RES 33K
IU3B
3U42
2K2
+12VF
IU38
7U0P
BSH112
3U40
68R
3U47
68R
2U2A
1u0
3U43
100K
7U0Q
BC847BW
3U3Y
1K0
IU36
IU37
3U3Z
10K
2U27
33p
2U28
220p
IU39
* IN CASE OF ONLY-ANALOG TUNER
3104 313 6304.3
I_18020_012.eps
190808

1M95	D1
1U01	E2
2U18	A6
2U24	C6
2U25	D7
2U26	D8
2U27	F7
2U28	F7
2U29	E7
2U2A	F7
2U2B	E8
2U32	D1
2U33	F1
2U34	F1
2U35	F1
2U36	F2
2U40	F3
2U50	B9
2U60	A2
2U62	A4
2U63	B3
2U64	A5
2U65	A5
2U66	C5
2U67	C5
2U68	A6
2U69	A7
2U70	C6
2U71	C6
2U72	D2
2U73	D3
2U74	D3
3U35	E2
3U36	E2
3U3V	D7
3U3W	C7
3U3Y	F6
3U3Z	F6
3U40	F7
3U42	F8
3U43	F8
3U44	E8
3U45	E8
3U46	C7
3U47	F7
3U48	B1
3U49	B2
3U4A	D7
3U50	A8
3U51	A9
3U52	B8
3U53	B9
3U54	B9
3U60	A2
3U61	A4
3U62	A3
3U63	A3
3U64	B3
3U65	A5
3U66	A5
3U67	B4
3U68	C5
3U69	C5
3U6A	A6
3U6B	B6
3U80	E4
3U81	E4
3U82	E4
3U83	E5
3U84	E3
3U85	F4
3U86	F5
3U87	E5
3U88	F3
3U89	F4
5U08	E7
6U0B	E7
6U0C	E7
6U40	E3
7U0M	D8
7U0N	D6
7U0P	F6
7U0Q	F8
7U0R	B1
7U40-1	E4
7U40-2	E4
7U41-1	F4
7U41-2	E5
7U50	B8
7U51	B9
7U70-1	A5
7U70-2	B5
7U71	A6
7U72	B6
7U73	D3
9U01	C3
FU10	E1
FU11	E1
FU12	E1
FU1A	D1
FU1B	E1
FU1C	E1
FU1D	E1
FU1F	D8
FU1G	E8
FU20	E1
FU21	E1
FU22	E1
FU23	E1
FU24	D3
FU27	B2
FU28	A7
FU29	B7
FU40	F5
FU75	E2
FU76	E2
IU34	D7
IU35	D7
IU36	F6
IU37	F7
IU38	F7
IU39	F8
IU3B	F7
IU3C	D7
IU3D	A2
IU3E	A4
IU3F	A4
IU3G	A5
IU3H	A5
IU3K	B4
IU3M	B4
IU3N	B5
IU3P	C5
IU3R	B9
IU3S	A8
IU3T	A9
IU40	E3
IU41	E4
IU42	E4
IU43	E4
IU44	F4
IU45	F5
IU46	E5
IU47	F4
IU8F	A6
IU8G	B6
IU8K	D3

SSB: DC / DC

2U19 A7
2U20 A13
2U80 C2
2U81 B5
2U82 D5
2U83 G2
2U84 G2
2U85 E6
2U86 D6
2U87 E8
2U88 C7
2U89 B6
2U8A A6
2U8B B9
2U8C B9
2U8D B10
2U8E A10
2U8F B14
2U8G D10
2U8H D10
2U8K D10
2U8L E8
2U8M D10
2U8N G9
2U8P E9
2U8Q E8
2U8R E8
2U8S C7
2U8T G2
2U8U C8
2U8V C8
2U8W C9
2U8Y E9
2U8Z D9
3U1W D6
3U1Y D7
3U1Z E8
3U20 B9
3U21 C9
3U22 D6
3U23 C7
3U24 D9
3U25 E9
3U26 F9
3U27 F10
3U28 D4
3U29 D4
3U2A D2
3U2B D2
3U2C G1
3U2D G2
3U2E D5
3U2F E10
3U2G B8
3U2H D9
3U2J C7
3U2K B6
3U2M C6
3U2N B6
3U2R B4
3U2U E11
3U2V D11
3U2W E12
3U2Y E12
3U2Z E12
3U30 D12
3U31 C7
3U32 C8
3U33 D8
3U34 D7
3U39 G9
3U3A F12
3U3B E7
3U3C E7
3U3D B4
3U3E B4
3U3F D11
3U3G F13
3U3H E8
3U3J B9
3U3K B6
3U3M B6
3U3N D9
3U3P C7
3U3Q C7
3U3T A5
5U04 D9
5U05 B9
5U06 A11
5U09 A11
6U05 E7
6U06 E8
6U07 B4
6U08 F8
6U09 B11
7U0D-1 B8
7U0D-2 C7
7U0E F8
7U0G-1 D3
7U0G-2 D4
7U0H-1 A6
7U0H-2 B7
7U0K-1 D12
7U0K-2 E12
7U0L B5
9U04 B11
9U05 B11
CU25 D6
FU80 C13
FU81 D12
FU82 E12
FU83 F12
FU84 G12
FU85 D10
FU86 E8
FU87 D8
FU88 D7
FU89 C7
FU8A C5
FU8B A8
FU8C B8
FU8D B13
IU20 C6
IU21 C6
IU22 C6
IU23 C6
IU24 C7
IU25 C7
IU26 C7
IU28 B7
IU29 B6
IU2A A6
IU2C C5
IU2D C5
IU2E C5
IU2F C5
IU2G C5
IU2H D4
IU2J D2
IU2M B4
IU2P E12
IU2R E7
IU2T G3
IU2V C9
IU2Y E9
IU2Z E9
IU80 B4
IU81 B5
IU82 B9
IU83 B9
IU84 C9
IU85 E9
IU86 E9
IU87 E9
IU88 E8
IU89 F14
IU8A D12
IU8B G9
IU8C E8
IU8D D6
IU8E D6


B01C
DC / DC
12V/5V CONVERSION
12V/1V2 CONVERSION
BOOSTER
7U0L NCP5422ADR2G
7U0H-1 SI4936BDY
7U0H-2 SI4936BDY
7U0D-1 SI4936BDY
7U0D-2 SI4936BDY
7U0G-1 BC847BS
7U0G-2 BC847BS
7U0K-1 BC847BS
7U0K-2 BC847BS
7U0E BC817-25W
+12VF
+12VFF
+5V5-TUN
+5V
+1V2-PNX5100
SENSE+1V2-PNX5100
ENABLE-3V3
PROT-DC
ENABLE-1V2
GND-SIG1
3104 313 6304.3
I_18020_013.eps
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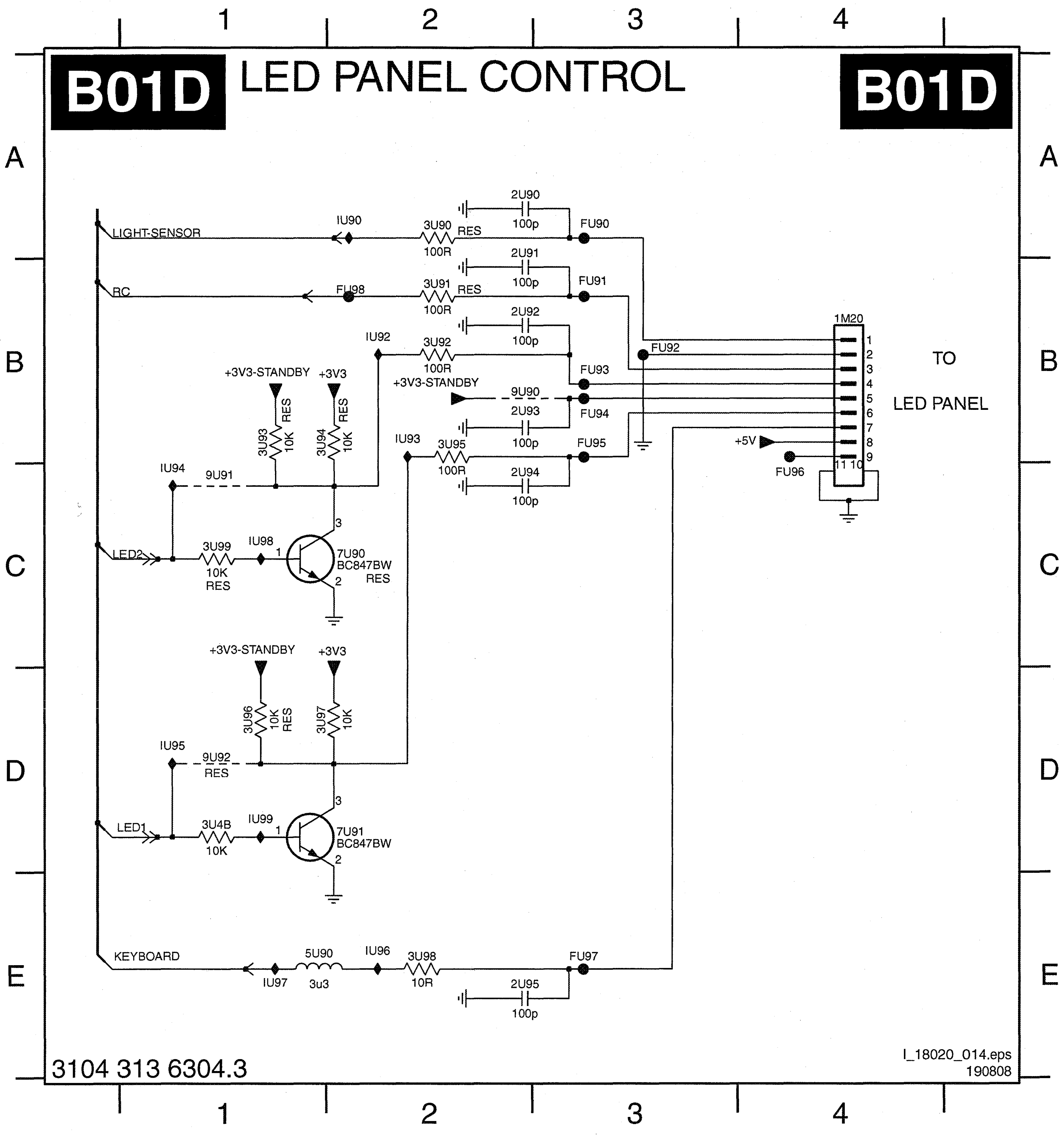
SSB: LED Panel Control

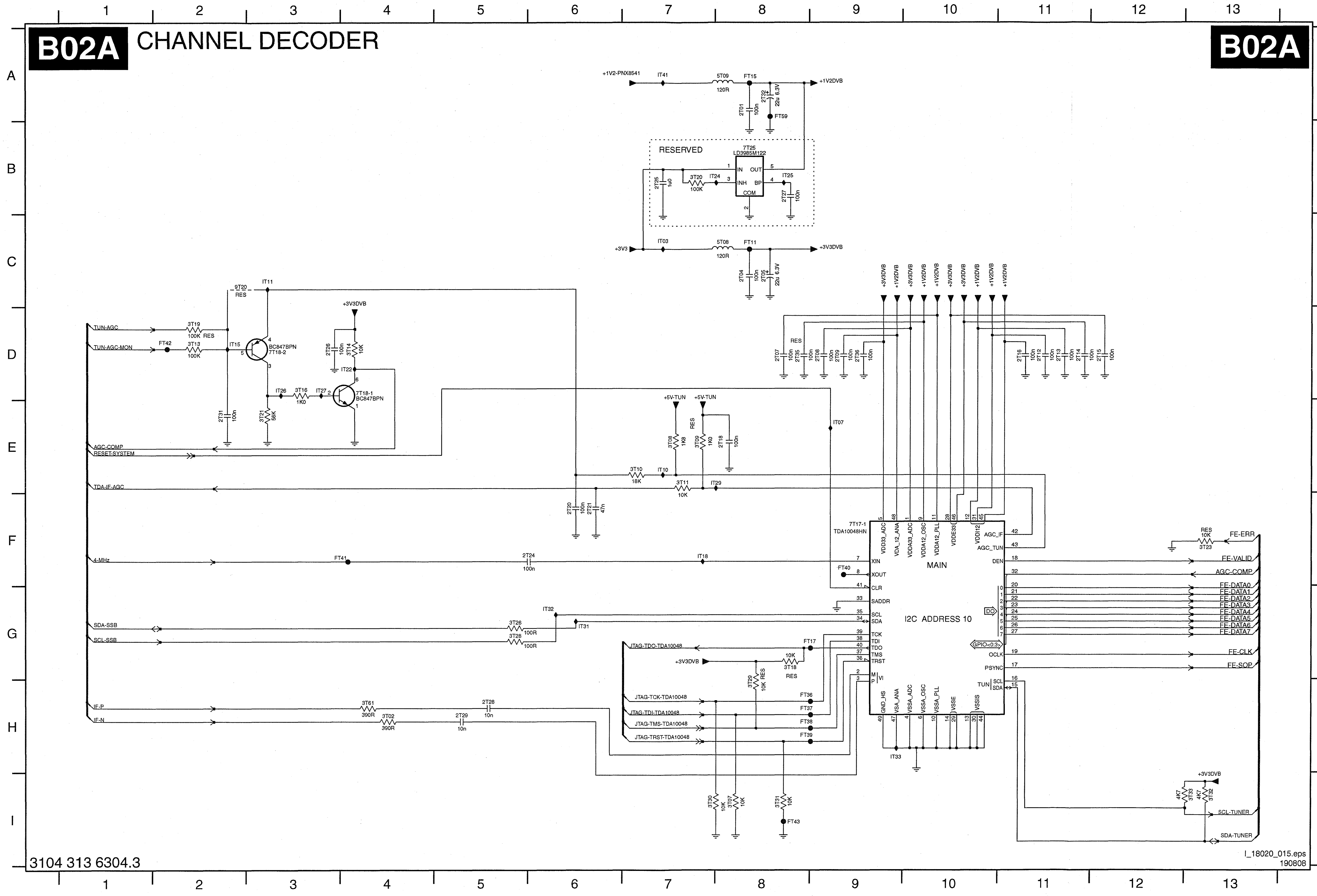
1M20 B4
2U90 A2
2U91 A2
2U92 B2
2U93 B2
2U94 C2
2U95 E2
3U4B D1
3U90 A2
3U91 B2
3U92 B2
3U93 B1
3U94 B1
3U95 B2
3U96 D1
3U97 D1
3U98 E2
3U99 C1
5U90 E1
7U90 C2
7U91 D2
9U90 B2
9U91 C1
9U92 D1
FU90 A3
FU91 B3
FU92 B3
FU93 B3
FU94 B3
FU95 B3
FU96 C4
FU97 E3
FU98 B2
IU90 A2
IU92 B2
IU93 B2
IU94 C1
IU95 D1
IU96 E2
IU97 E1
IU98 C1
IU99 D1


1
2
3
4
A
B
C
D
E
B01D
LED PANEL CONTROL
B01D
LIGHT-SENSOR
RC
LED2
LED1
KEYBOARD
IU90
3U90 RES 100R
2U90 100p
FU90
FU98
3U91 RES 100R
2U91 100p
FU91
IU92
3U92 100R
2U92 100p
FU92
FU93
+3V3-STANDBY
9U90
2U93 100p
FU94
IU93
3U95 100R
FU95
2U94 100p
1M20
1 2 3 4 5 6 7 8 9 11 10
+5V
FU96
TO
LED PANEL
+3V3-STANDBY
+3V3
3U93 10K RES
3U94 10K RES
IU94
9U91
3U99 10K RES
IU98
7U90 BC847BW RES
+3V3-STANDBY
+3V3
3U96 10K RES
3U97 10K
IU95
9U92 RES
3U4B 10K
IU99
7U91 BC847BW
5U90 3u3
IU97
IU96
3U98 10R
FU97
2U95 100p
3104 313 6304.3
I_18020_014.eps
190808

Personal Notes:

E_06532_012.eps
131004

SSB: Channel Decoder


B02A
CHANNEL DECODER
B02A
+1V2-PNX8541
IT41
5T09
120R
FT15
+1V2DVB
2T01
100n
2T32
22u 6.3V
FT59
RESERVED
7T25
LD3985M122
IN
OUT
INH
BP
COM
2T25
1u0
3T20
100K
IT24
IT25
2T27
100n
+3V3
IT03
5T08
120R
FT11
+3V3DVB
2T04
100n
2T05
22u 6.3V
9T20
RES
IT11
3T19
100K RES
TUN-AGC
TUN-AGC-MON
FT42
3T13
100K
IT15
BC847BPN
7T18-2
+3V3DVB
2T26
100n
3T14
10K
IT22
IT26
3T16
1K0
IT27
7T18-1
BC847BPN
2T31
100n
3T21
56K
AGC-COMP
RESET-SYSTEM
+5V-TUN
3T08
1K8
3T09
1K0
RES
2T18
100n
IT07
3T10
18K
IT10
3T11
10K
IT29
TDA-IF-AGC
2T20
100n
2T21
47n
RES
2T07
2T35
2T08
2T09
2T36
2T16
2T12
2T13
2T14
2T15
100n
4-MHz
FT41
2T24
100n
IT18
7T17-1
TDA10048HN
VDD33_ADC
VDA_12_ANA
VDDA33_ADC
VDDA12_OSC
VDDA12_PLL
VDDE33
VDDI12
XIN
XOUT
FT40
CLR
SADDR
SCL
SDA
TCK
TDI
TDO
TMS
TRST
M
P
VI
MAIN
I2C ADDRESS 10
AGC_IF
AGC_TUN
DEN
OCLK
PSYNC
TUN SCL SDA
D0
GPIO<0:3>
GND_HS
VSA_ANA
VSSA_ADC
VSSA_OSC
VSSA_PLL
VSSE
VSSIS
IT33
IT32
IT31
SDA-SSB
SCL-SSB
3T26
100R
3T28
100R
JTAG-TDO-TDA10048
+3V3DVB
FT17
10K
3T18
RES
3T29
10K RES
JTAG-TCK-TDA10048
JTAG-TDI-TDA10048
JTAG-TMS-TDA10048
JTAG-TRST-TDA10048
FT36
FT37
FT38
FT39
IF-P
IF-N
3T61
390R
3T02
390R
2T29
10n
2T28
10n
3T30
10K
3T07
10K
3T31
10K
FT43
RES
10K
3T23
FE-ERR
FE-VALID
AGC-COMP
FE-DATA0
FE-DATA1
FE-DATA2
FE-DATA3
FE-DATA4
FE-DATA5
FE-DATA6
FE-DATA7
FE-CLK
FE-SOP
+3V3DVB
4K7
3T33
4K7
3T32
SCL-TUNER
SDA-TUNER
3104 313 6304.3
I_18020_015.eps
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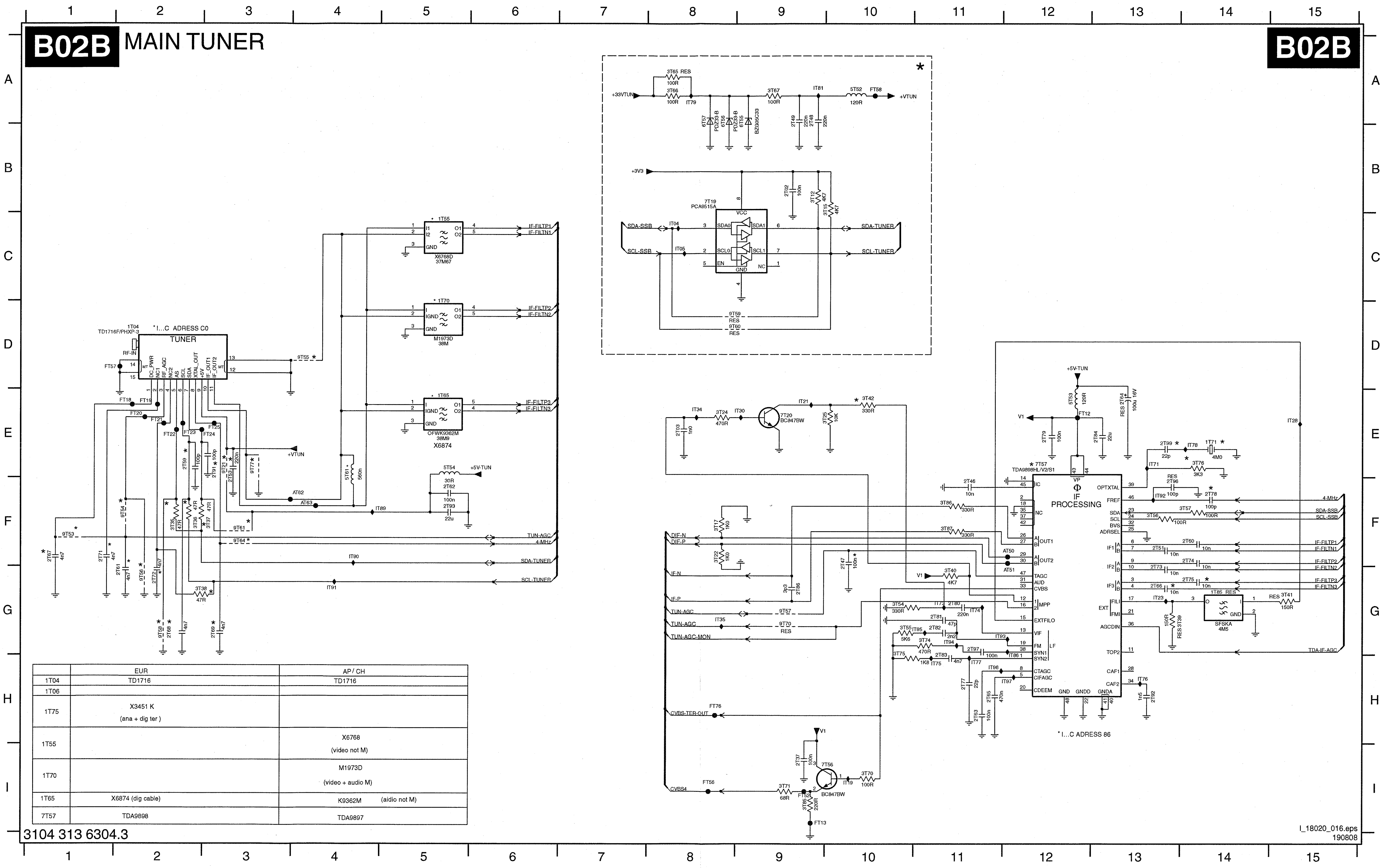
2T01	A8
2T04	C8
2T05	C8
2T07	D8
2T08	D9
2T09	D9
2T12	D11
2T13	D11
2T14	D11
2T15	D12
2T16	D11
2T18	E8
2T20	F6
2T21	F6
2T24	F6
2T25	B7
2T26	D3
2T27	B8
2T28	H5
2T29	H5
2T31	E2
2T32	A8
2T35	D8
2T36	D9
3T02	H4
3T07	I8
3T08	E7
3T09	E7
3T10	E7
3T11	E7
3T13	D2
3T14	D4
3T16	D3
3T18	G8
3T19	D2
3T20	B7
3T21	E3
3T23	F13
3T26	G5
3T28	G5
3T29	H8
3T30	I7
3T31	I8
3T32	I13
3T33	I13
3T61	H4
5T08	C8
5T09	A8
7T17-1	F9
7T18-1	D4
7T18-2	D3
7T25	B8
9T20	C2
FT11	C8
FT15	A8
FT17	G9
FT36	H8
FT37	H8
FT38	H8
FT39	H8
FT40	F9
FT41	F4
FT42	D2
FT43	I8
FT59	A8
IT03	C7
IT07	E9
IT10	E7
IT11	C3
IT15	D2
IT18	F7
IT22	D4
IT24	B7
IT25	B8
IT26	D3
IT27	D3
IT29	E8
IT31	G6
IT32	G6
IT33	H9
IT41	A7

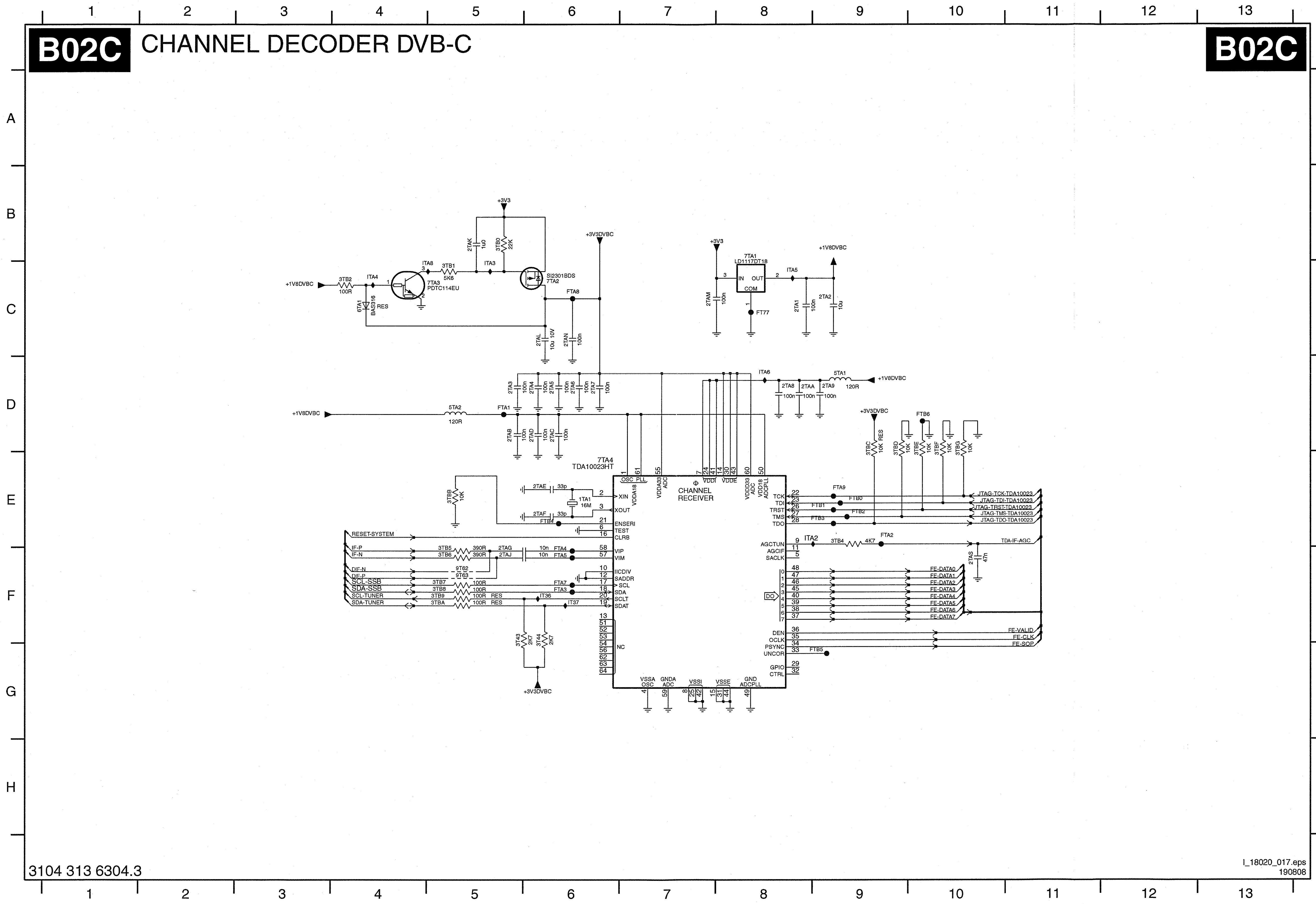
SSB: Main Tuner

1T04 D2
1T06 A2
1T08 C2
1T55 C5
1T65 E5
1T70 D5
1T71 E14
1T85 G14
2T02 B9
2T03 E8
2T37 I9
2T46 F11
2T47 F10
2T48 A9
2T49 A9
2T51 F13
2T53 E3
2T59 E2
2T60 F14
2T61 G2
2T62 F5
2T63 H11
2T64 E13
2T65 H11
2T66 G13
2T67 F1
2T68 G2
2T69 G3
2T71 F1
2T72 G2
2T73 G13
2T74 F14
2T75 G14
2T77 H11
2T78 F14
2T79 E12
2T80 G11
2T81 G11
2T82 G11
2T83 H11
2T84 E13
2T86 G9
2T91 E3
2T92 H13
2T93 F5
2T96 F13
2T97 G11
2T99 E13
3T12 B9
3T15 B10
3T17 F8
3T22 F8
3T24 E8
3T25 E10
3T35 F2
3T36 F2
3T37 F3
3T38 G2
3T39 G14
3T40 G11
3T41 G15
3T42 E10
3T54 G10
3T55 G10
3T56 F13
3T57 F14
3T65 A8
3T66 A8
3T67 A9
3T70 I10
3T71 I9
3T74 G11
3T75 H10
3T76 E14
3T85 I9
3T86 F11
3T87 F11
5T52 A10
5T53 E12
5T54 E5
5T61 E4
6T55 A9
6T56 A8
6T57 A8
7T19 B8
7T20 E9
7T56 I10
7T57 E12
9T21 E3
9T53 F1
9T54 F2
9T55 D4
9T56 G2
9T57 G9
9T58 G2
9T59 D8
9T60 D8
9T61 F3
9T64 F3
9T70 G9
9T77 E3
AT50 F12
AT51 G12
AT62 F4
AT63 F4
FT12 E12
FT13 I9
FT18 E2
FT19 E2
FT20 E2
FT21 E2
FT22 E2
FT23 E2
FT24 E3
FT25 E3
FT52 I9
FT56 I8
FT57 D2
FT58 A10
FT76 H8
IT04 C8
IT05 C8
IT19 I10
IT21 E9
IT23 G13
IT28 E15
IT30 E9
IT34 E8
IT35 G8
IT71 E13
IT73 G11
IT74 G11
IT75 H11
IT76 H13
IT77 H11
IT78 E14
IT79 A8
IT81 A9
IT86 H12
IT89 F5
IT90 F4
IT91 G4
IT92 F13
IT93 G11
IT94 G11
IT95 G11
IT96 H11
IT97 H12


B02B
MAIN TUNER
B02B
TUNER
TD1716F/PHXP-3
*I...C ADRESS C0
RF-IN
1T55
X6768D
37M67
1T70
M1973D
38M
1T65
OFWK9362M
38M9
X6874
IF-FILTP1
IF-FILTN1
IF-FILTP2
IF-FILTN2
IF-FILTP3
IF-FILTN3
+VTUN
+5V-TUN
TUN-AGC
4-MHz
SDA-TUNER
SCL-TUNER
+33VTUN
+VTUN
+3V3
7T19
PCA9515A
SDA-SSB
SCL-SSB
SDA-TUNER
SCL-TUNER
7T20
BC847BW
V1
7T57
TDA9898HL/V2/S1
IF PROCESSING
OPTXTAL
FREF
SDA
SCL
BVS
ADRSEL
OUT1
OUT2
TAGC
AUD
CVBS
MPP
EXTFILO
VIF
FM
SYN1
SYN2
CTAGC
CIFAGC
CDEEM
GND
GNDD
GNDA
IF1
IF2
IF3
EXT
AGCDIN
TOP2
CAF1
CAF2
1T85
SFSKA
4M5
TDA-IF-AGC
DIF-N
DIF-P
IF-N
IF-P
TUN-AGC
TUN-AGC-MON
CVBS-TER-OUT
CVBS4
7T56
BC847BW
FT13
*I...C ADRESS 86
3104 313 6304.3
I_18020_016.eps
190808

	EUR	AP / CH
1T04	TD1716	TD1716
1T06		
1T75	X3451 K (ana + dig ter)	
1T55		X6768 (video not M)
1T70		M1973D (video + audio M)
1T65	X6874 (dig cable)	K9362M (aidio not M)
7T57	TDA9898	TDA9897

SSB: Channel Decoder DVB-C


B02C
CHANNEL DECODER DVB-C
B02C
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H
+3V3
2TAK 1u0
3TB0 22K
ITA3
ITA8
3TB1 5K6
SI2301BDS
7TA2
+1V8DVBC
3TB2 100R
ITA4
7TA3 PDTC114EU
6TA1 BAS316
RES
FTA8
2TAL 10u 10V
2TAN 100n
+3V3DVBC
+3V3
7TA1 LD1117DT18
IN OUT COM
FT77
ITA5
2TAM 100n
2TA1 100n
2TA2 10u
+1V8DVBC
2TA3 100n
2TA4 100n
2TA5 100n
2TA6 100n
2TA7 100n
ITA6
5TA1 120R
2TA8 100n
2TAA 100n
2TA9 100n
+1V8DVBC
5TA2 120R
FTA1
2TAB 100n
2TAD 100n
2TAC 100n
7TA4
TDA10023HT
OSC PLL
VDDA18
VDDA33 ADC
VDDI
VDDE
VDD33 ADC
VDD18 ADCPLL
CHANNEL RECEIVER
3TBB 10K
2TAE 33p
1TA1 16M
2TAF 33p
FTB4
XIN
XOUT
ENSERI
TEST
CLRB
RESET-SYSTEM
IF-P
IF-N
3TB5 390R
3TB6 390R
2TAG 10n
2TAJ 10n
FTA4
FTA5
VIP
VIM
DIF-N
DIF-P
9T62
9T63
SCL-SSB
SDA-SSB
SCL-TUNER
SDA-TUNER
3TB7 100R
3TB8 100R
3TB9 100R RES
3TBA 100R RES
IT36
IT37
FTA7
FTA3
IICDIV
SADDR
SCL
SDA
SCLT
SDAT
NC
3T43 2K7
3T44 2K7
+3V3DVBC
+3V3DVBC
FTB6
3TBC 10K RES
3TBD 10K
3TBE 10K
3TBF 10K
3TBG 10K
FTA9
FTB0
FTB1
FTB2
FTB3
TCK
TDI
TRST
TMS
TDO
JTAG-TCK-TDA10023
JTAG-TDI-TDA10023
JTAG-TRST-TDA10023
JTAG-TMS-TDA10023
JTAG-TDO-TDA10023
ITA2
3TB4 4K7
FTA2
AGCTUN
AGCIF
SACLK
TDA-IF-AGC
2TAS 47n
DO
FE-DATA0
FE-DATA1
FE-DATA2
FE-DATA3
FE-DATA4
FE-DATA5
FE-DATA6
FE-DATA7
DEN
OCLK
PSYNC
UNCOR
FTB5
FE-VALID
FE-CLK
FE-SOP
GPIO CTRL
VSSA OSC
GNDA ADC
VSSI
VSSE
GND ADCPLL
3104 313 6304.3
I_18020_017.eps
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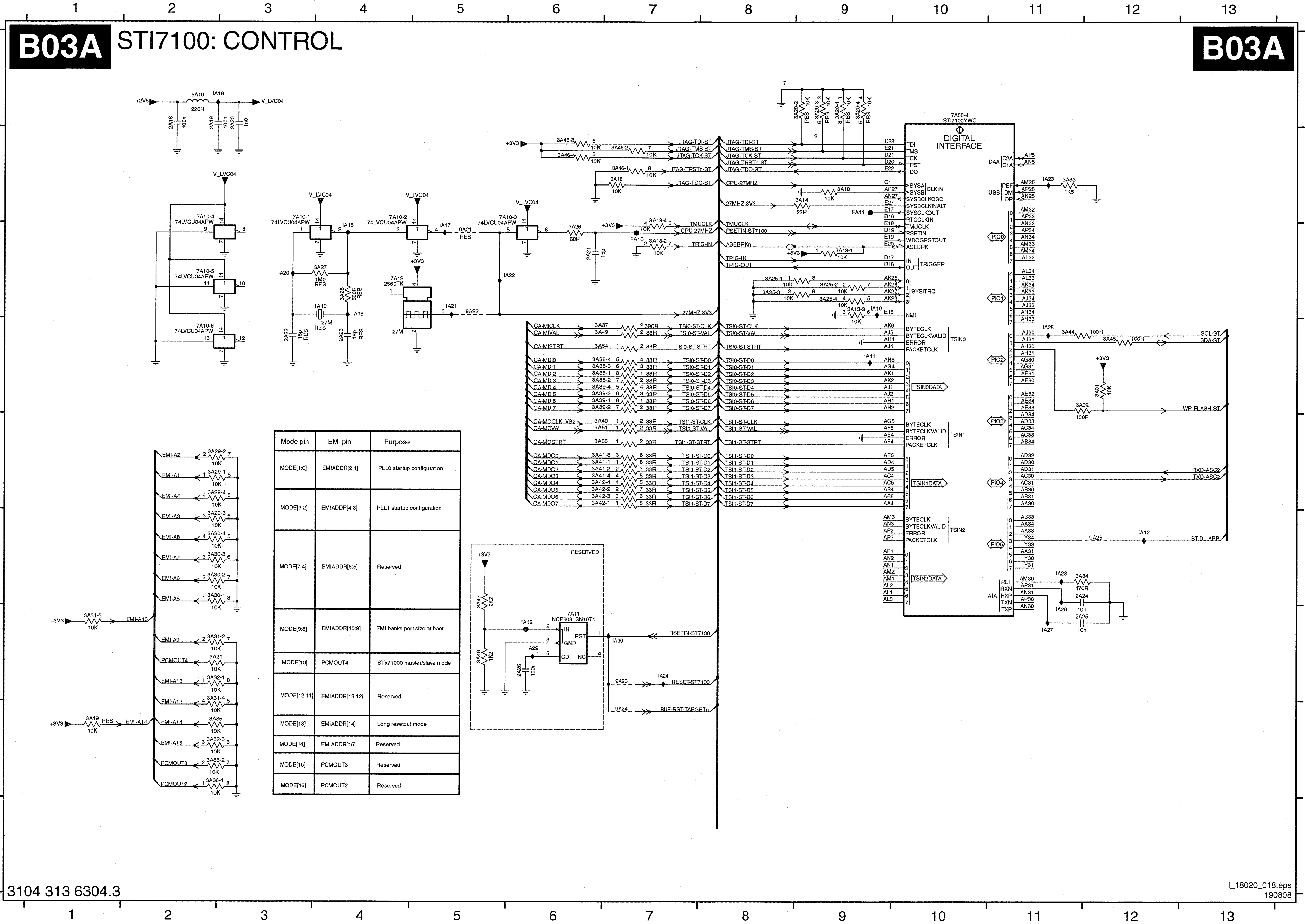
1TA1	E6
2TA1	C8
2TA2	C9
2TA3	D5
2TA4	D6
2TA5	D6
2TA6	D6
2TA7	D6
2TA8	D8
2TA9	D9
2TAA	D8
2TAB	D5
2TAC	D6
2TAD	D6
2TAE	E6
2TAF	E6
2TAG	F5
2TAJ	F5
2TAK	B5
2TAL	C6
2TAM	C7
2TAN	C6
2TAS	F10
3T43	F5
3T44	F6
3TB0	B5
3TB1	C5
3TB2	C4
3TB4	E9
3TB5	F5
3TB6	F5
3TB7	F5
3TB8	F5
3TB9	F5
3TBA	F5
3TBB	E5
3TBC	D9
3TBD	D9
3TBE	D10
3TBF	D10
3TBG	D10
5TA1	D9
5TA2	D5
6TA1	C4
7TA1	B8
7TA2	C6
7TA3	C4
7TA4	E6
9T62	F5
9T63	F5
FT77	C8
FTA1	D5
FTA2	E9
FTA3	F6
FTA4	F6
FTA5	F6
FTA7	F6
FTA8	C6
FTA9	E9
FTB0	E9
FTB1	E9
FTB2	E9
FTB3	E9
FTB4	E6
FTB5	G9
FTB6	D10
IT36	F6
IT37	F6
ITA2	E8
ITA3	C5
ITA4	C4
ITA5	C8
ITA6	D8
ITA8	C5

SSB: STi7100: Control


B03A
STI7100: CONTROL
B03A
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H I
+2V5
5A10
220R
IA19
V_LVC04
2A18 100n
2A19 100n
2A20 1n0
7A10-4 74LVCU04APW
7A10-5 74LVCU04APW
7A10-6 74LVCU04APW
7A10-1 74LVCU04APW
7A10-2 74LVCU04APW
7A10-3 74LVCU04APW
IA16
IA17
IA20
3A27 1M0 RES
3A28 560R RES
1A10 27M RES
IA18
2A22 18p RES
2A23 18p RES
7A12 2560TK
27M
+3V3
9A21 RES
9A22
IA21
IA22
3A26 68R
2A21 15p
+3V3
3A13-4 10K
TMUCLK
CPU-27MHZ
FA10
3A13-2 10K
TRIG-IN
27MHZ-3V3
3A46-3 10K
3A46-2 10K
3A46-4 10K
3A46-1 10K
3A16 10K
JTAG-TDI-ST
JTAG-TMS-ST
JTAG-TCK-ST
JTAG-TRSTn-ST
JTAG-TDO-ST
3A20-2 RES 10K
3A20-3 RES 10K
3A20-1 RES 10K
3A20-4 RES 10K
7A00-4 STI7100YWC
DIGITAL INTERFACE
TDI TMS TCK TRST TDO
SYSA SYSB CLKIN
SYSCLKOSC SYSCLKINALT SYSCLKOUT RTCCLKIN TMUCLK RSETIN WDOGRSTOUT ASEBRK
TRIGGER
SYSITRQ
NMI
3A14 22R
3A18 10K
FA11
3A25-1 10K
3A25-2 10K
3A25-3 10K
3A25-4 10K
3A13-3 10K
IA10
3A13-1 10K
CA-MICLK
CA-MIVAL
CA-MISTRT
CA-MIDI0 … CA-MIDI7
CA-MOCLK_VS2
CA-MOVAL
CA-MOSTRT
CA-MDO0 … CA-MDO7
3A37 390R
3A49 33R
3A54 33R
3A38-4 33R
3A38-3 33R
3A38-1 33R
3A38-2 33R
3A39-4 33R
3A39-3 33R
3A39-1 33R
3A39-2 33R
3A40 33R
3A51 33R
3A55 33R
3A41-3 33R
3A41-1 33R
3A41-2 33R
3A41-4 33R
3A42-4 33R
3A42-2 33R
3A42-3 33R
3A42-1 33R
TSI0-ST-CLK
TSI0-ST-VAL
TSI0-ST-STRT
TSI0-ST-D0 … TSI0-ST-D7
TSI1-ST-CLK
TSI1-ST-VAL
TSI1-ST-STRT
TSI1-ST-D0 … TSI1-ST-D7
BYTECLK BYTECLKVALID ERROR PACKETCLK
TSIN0
TSIN0DATA
TSIN1
TSIN1DATA
TSIN2
TSIN2DATA
IA11
DAA C2A C1A
AP5 AN5
USB REF DM DP
AM25 AP25 AN25
IA23
3A33 1K5
PIO0 PIO1 PIO2 PIO3 PIO4 PIO5
IA25
3A44 100R
3A45 100R
SCL-ST
SDA-ST
+3V3
3A01 10K
3A02 100R
WP-FLASH-ST
RXD-ASC2
TXD-ASC2
9A25
IA12
ST-DL-APP
ATA REF RXN RXP TXN TXP
IA28
3A34 470R
2A24 10n
IA26
2A25 10n
IA27
EMI-A2 3A29-2 10K
EMI-A1 3A29-1 10K
EMI-A4 3A29-4 10K
EMI-A3 3A29-3 10K
EMI-A8 3A30-4 10K
EMI-A7 3A30-3 10K
EMI-A6 3A30-2 10K
EMI-A5 3A30-1 10K
+3V3
3A31-3 10K
EMI-A10
EMI-A9 3A31-2 10K
PCMOUT4 3A21 10K
EMI-A13 3A32-1 10K
EMI-A12 3A31-4 10K
+3V3
3A19 10K RES
EMI-A14
EMI-A14 3A35 10K
EMI-A15 3A32-3 10K
PCMOUT3 3A36-2 10K
PCMOUT2 3A36-1 10K
RESERVED
+3V3
3A47 2K2
3A48 1K2
FA12
IA29
2A26 100n
7A11 NCP303LSN10T1
IN GND CD RST NC
IA30
RSETIN-ST7100
9A23
IA24
RESET-ST7100
9A24
BUF-RST-TARGETn
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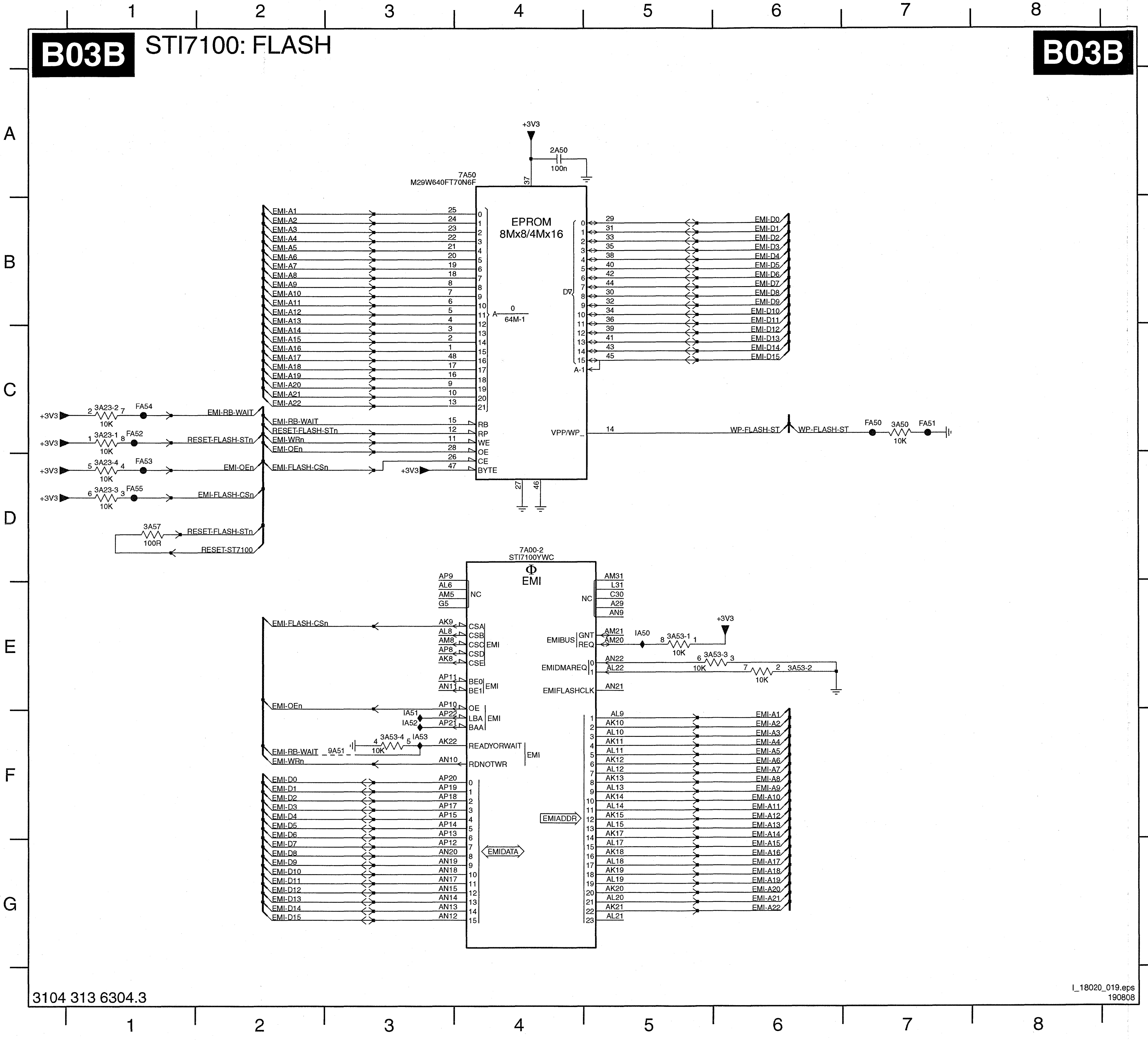
Mode pin	EMI pin	Purpose
MODE[1:0]	EMIADDR[2:1]	PLL0 startup configuration
MODE[3:2]	EMIADDR[4:3]	PLL1 startup configuration
MODE[7:4]	EMIADDR[8:5]	Reserved
MODE[9:8]	EMIADDR[10:9]	EMI banks port size at boot
MODE[10]	PCMOUT4	STx71000 master/slave mode
MODE[12:11]	EMIADDR[13:12]	Reserved
MODE[13]	EMIADDR[14]	Long resetout mode
MODE[14]	EMIADDR[15]	Reserved
MODE[15]	PCMOUT3	Reserved
MODE[16]	PCMOUT2	Reserved

1A10	C4
2A18	A2
2A19	A2
2A20	A3
2A21	C6
2A22	D3
2A23	D4
2A24	F11
2A25	G11
2A26	G6
3A01	D12
3A02	D11
3A13-1	C9
3A13-2	C7
3A13-3	C9
3A13-4	B7
3A14	B9
3A16	B7
3A18	B9
3A19	H1
3A20-1	A9
3A20-2	A9
3A20-3	A9
3A20-4	A9
3A21	G2
3A25-1	C8
3A25-2	C9
3A25-3	C8
3A25-4	C9
3A26	C6
3A27	C4
3A28	C4
3A29-1	E2
3A29-2	E2
3A29-3	F2
3A29-4	E2
3A30-1	F2
3A30-2	F2
3A30-3	F2
3A30-4	F2
3A31-2	G2
3A31-3	G1
3A31-4	G2
3A32-1	G2
3A32-3	H2
3A33	B11
3A34	F11
3A35	H2
3A36-1	H2
3A36-2	H2
3A37	D6
3A38-1	D6
3A38-2	D6
3A38-3	D6
3A38-4	D6
3A39-1	D6
3A39-2	D6
3A39-3	D6
3A39-4	D6
3A40	E6
3A41-1	E6
3A41-2	E6
3A41-3	E6
3A41-4	E6
3A42-1	E6
3A42-2	E6
3A42-3	E6
3A42-4	E6
3A44	D11
3A45	D12
3A46-1	B7
3A46-2	B7
3A46-3	B6
3A46-4	B6
3A47	F5
3A48	G5
3A49	D6
3A51	E6
3A54	D6
3A55	E6
5A10	A2
7A00-4	A10
7A10-1	B3
7A10-2	B4
7A10-3	B6
7A10-4	B2
7A10-5	C2
7A10-6	D2
7A11	G6
7A12	C4
9A21	C5
9A22	C5
9A23	G7
9A24	H7
9A25	F12
FA10	C7
FA11	B9
FA12	G6
IA10	C9
IA11	D9
IA12	F12
IA16	C4
IA17	C5
IA18	C4
IA19	A2
IA20	C3
IA21	C5
IA22	C6
IA23	B11
IA24	G7
IA25	D11
IA26	G11
IA27	G11
IA28	F11
IA29	G6
IA30	G7

SSB: STi7100: Flash


B03B
STI7100: FLASH
B03B
7A50
M29W640FT70N6F
EPROM
8Mx8/4Mx16
+3V3
2A50
100n
7A00-2
STI7100YWC
EMI
EMIBUS
EMIDMAREQ
EMIFLASHCLK
EMIADDR
EMIDATA
READYORWAIT
RDNOTWR
VPP/WP_
WP-FLASH-ST
FA50
3A50
10K
FA51
3A23-2
FA54
EMI-RB-WAIT
3A23-1
FA52
RESET-FLASH-STn
3A23-4
FA53
EMI-OEn
3A23-3
FA55
EMI-FLASH-CSn
3A57
100R
RESET-ST7100
3A53-1
3A53-3
3A53-2
3A53-4
IA50
IA51
IA52
IA53
9A51
EMI-WRn
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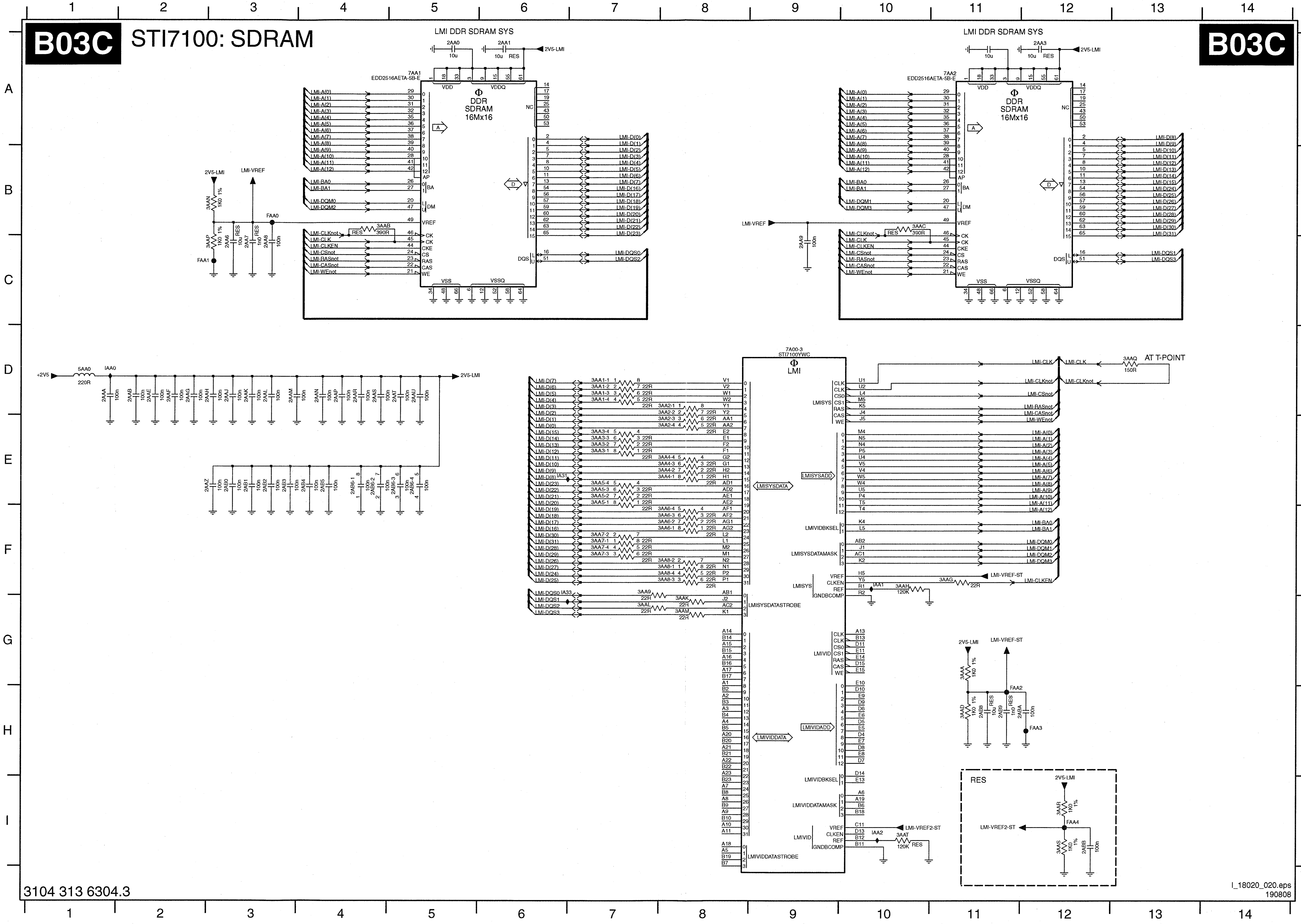
2A50	A4
3A23-1	C1
3A23-2	C1
3A23-3	D1
3A23-4	D1
3A50	C7
3A53-1	E5
3A53-2	E6
3A53-3	E6
3A53-4	F3
3A57	D1
7A00-2	D4
7A50	A4
9A51	F3
FA50	C7
FA51	C7
FA52	C1
FA53	D1
FA54	C1
FA55	D1
IA50	E5
IA51	F3
IA52	F3
IA53	F3

SSB: STi7100: SDRAM


B03C
STI7100: SDRAM
B03C
LMI DDR SDRAM SYS
LMI DDR SDRAM SYS
2V5-LMI
7AA1
EDD2516AETA-5B-E
7AA2
EDD2516AETA-5B-E
DDR
SDRAM
16Mx16
VDD
VDDQ
VSS
VSSQ
NC
VREF
CK
CKE
CS
RAS
CAS
WE
DM
BA
AP
DQS
LMI-VREF
FAA0
FAA1
3AAB
390R
3AAC
390R
7A00-3
STI7100YWC
LMI
LMISYS
LMISYSDATA
LMISYSADD
LMIVIDBKSEL
LMISYSDATAMASK
LMISYSDATASTROBE
LMIVID
LMIVIDDATA
LMIVIDADD
LMIVIDDATAMASK
LMIVIDDATASTROBE
GNDBCOMP
LMI-CLK
LMI-CLKnot
3AAQ
150R
AT T-POINT
LMI-VREF-ST
LMI-VREF2-ST
+2V5
5AA0
220R
IAA0
FAA2
FAA3
FAA4
RES
3104 313 6304.3
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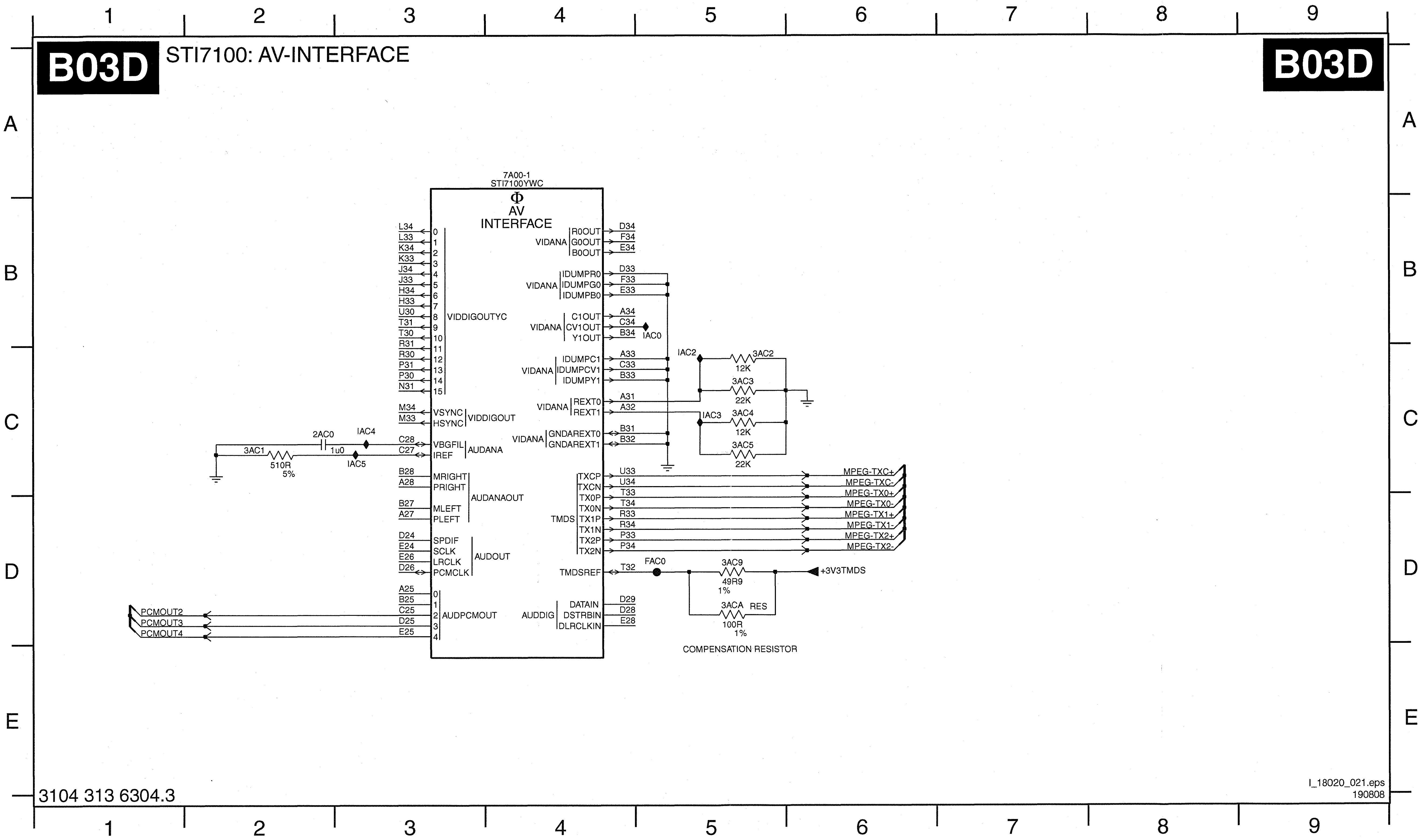
2AA0	A5
2AA1	A6
2AA2	A11
2AA3	A12
2AA6	C3
2AA7	C3
2AA8	C3
2AA9	C9
2AAA	D1
2AAB	D2
2AAE	D2
2AAF	D2
2AAG	D2
2AAH	D3
2AAJ	D3
2AAK	D3
2AAL	D3
2AAM	D3
2AAN	D4
2AAP	D4
2AAR	D4
2AAS	D4
2AAT	D5
2AAU	D5
2AAZ	E3
2AB0	E3
2AB1	E3
2AB2	E3
2AB3	E3
2AB4	E4
2AB5	E4
2AB6-1	E4
2AB6-2	E4
2AB6-3	E5
2AB6-4	E5
2AB8	H11
2AB9	H11
2ABA	H12
2ABB	I12
3AA1-1	D7
3AA1-2	D7
3AA1-3	D7
3AA1-4	D7
3AA2-1	D8
3AA2-2	D8
3AA2-3	E8
3AA2-4	E8
3AA3-1	E7
3AA3-2	E7
3AA3-3	E7
3AA3-4	E7
3AA4-1	E8
3AA4-2	E8
3AA4-3	E8
3AA4-4	E8
3AA5-1	E7
3AA5-2	E7
3AA5-3	E7
3AA5-4	E7
3AA6-1	F8
3AA6-2	F8
3AA6-3	F8
3AA6-4	F8
3AA7-1	F7
3AA7-2	F7
3AA7-3	F7
3AA7-4	F7
3AA8-1	F8
3AA8-2	F8
3AA8-3	F8
3AA8-4	F8
3AA9	F7
3AAA	G11
3AAB	B4
3AAC	B10
3AAD	H11
3AAG	F11
3AAH	F10
3AAK	G8
3AAL	G7
3AAM	G8
3AAN	B3
3AAP	C3
3AAQ	D13
3AAR	I12
3AAS	I12
3AAT	I10
5AA0	D1
7A00-3	D9
7AA1	A5
7AA2	A11
FAA0	B3
FAA1	C2
FAA2	H11
FAA3	H12
FAA4	I12
IA31	E6
IA33	F6
IAA0	D1
IAA1	F10
IAA2	I10

SSB: STi7100: AV-Interface


1 2 3 4 5 6 7 8 9
A B C D E
B03D
STI7100: AV-INTERFACE
B03D
7A00-1
STI7100YWC
Φ
AV
INTERFACE
L34 L33 K34 K33 J34 J33 H34 H33 U30 T31 T30 R31 R30 P31 P30 N31
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
VIDDIGOUTYC
M34 M33
VSYNC
HSYNC
VIDDIGOUT
2AC0
IAC4
3AC1
1u0
510R
5%
IAC5
C28 C27
VBGFIL
IREF
AUDANA
B28 A28 B27 A27
MRIGHT
PRIGHT
MLEFT
PLEFT
AUDANAOUT
D24 E24 E26 D26
SPDIF
SCLK
LRCLK
PCMCLK
AUDOUT
A25 B25 C25 D25 E25
0 1 2 3 4
AUDPCMOUT
PCMOUT2
PCMOUT3
PCMOUT4
VIDANA
R0OUT G0OUT B0OUT
D34 F34 E34
VIDANA
IDUMPR0 IDUMPG0 IDUMPB0
D33 F33 E33
VIDANA
C1OUT CV1OUT Y1OUT
A34 C34 B34
IAC0
VIDANA
IDUMPC1 IDUMPCV1 IDUMPY1
A33 C33 B33
VIDANA
REXT0 REXT1
A31 A32
VIDANA
GNDAREXT0 GNDAREXT1
B31 B32
IAC2
3AC2
12K
3AC3
22K
IAC3
3AC4
12K
3AC5
22K
TMDS
TXCP TXCN TX0P TX0N TX1P TX1N TX2P TX2N
U33 U34 T33 T34 R33 R34 P33 P34
MPEG-TXC+
MPEG-TXC-
MPEG-TX0+
MPEG-TX0-
MPEG-TX1+
MPEG-TX1-
MPEG-TX2+
MPEG-TX2-
TMDSREF
T32
FAC0
3AC9
49R9
1%
+3V3TMDS
3ACA
RES
100R
1%
COMPENSATION RESISTOR
AUDDIG
DATAIN DSTRBIN DLRCLKIN
D29 D28 E28
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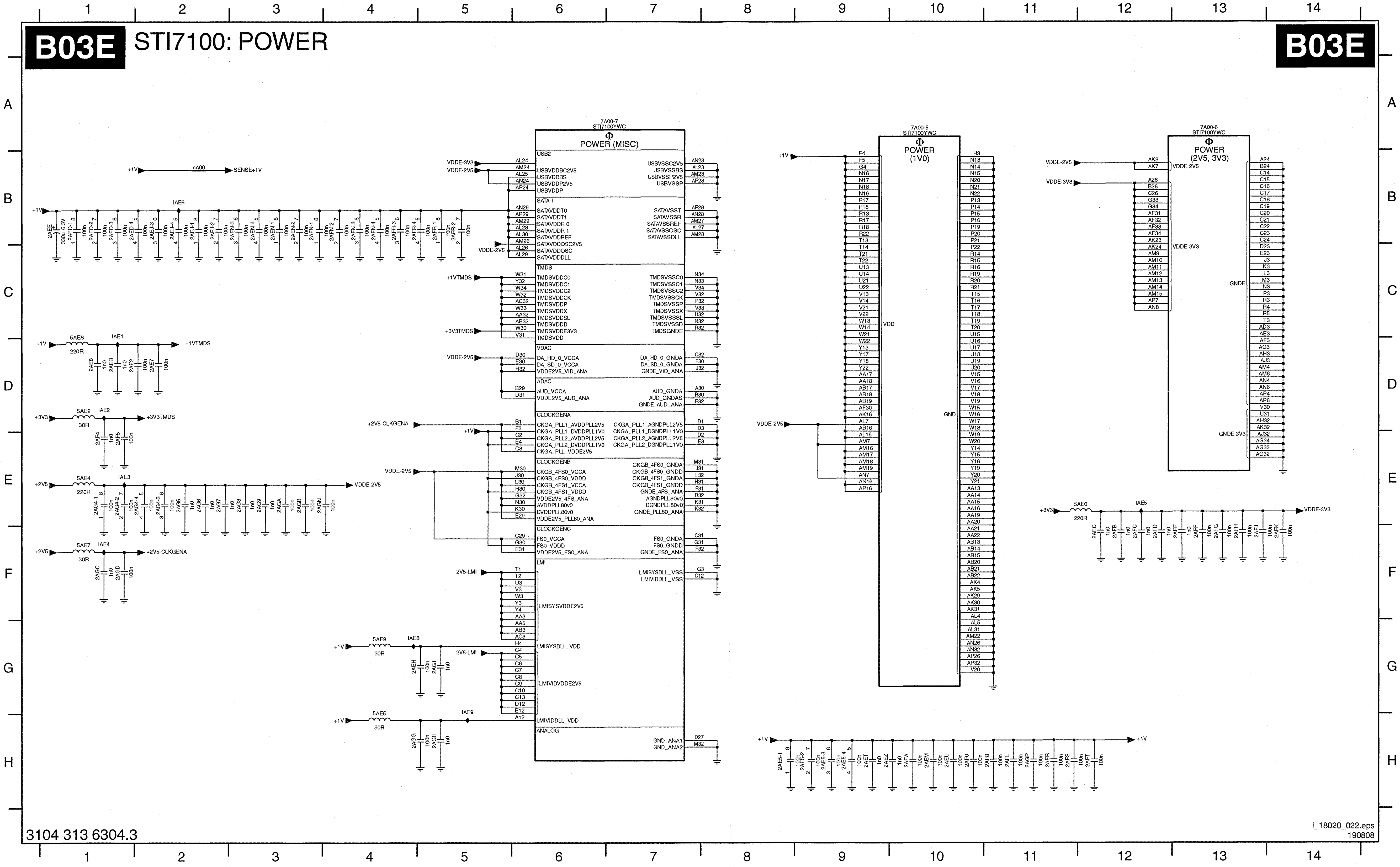
2AC0	C2
3AC1	C2
3AC2	C5
3AC3	C5
3AC4	C5
3AC5	C5
3AC9	D5
3ACA	D5
7A00-1	A4
FAC0	D5
IAC0	B5
IAC2	C5
IAC3	C5
IAC4	C3
IAC5	C3

SSB: STi7100: Power


B03E
STI7100: POWER
B03E
7A00-7
STI7100YWC
POWER (MISC)
7A00-5
STI7100YWC
POWER
(1V0)
7A00-6
STI7100YWC
POWER
(2V5, 3V3)
USB2
SATA-I
TMDS
VDAC
ADAC
CLOCKGENA
CLOCKGENB
CLOCKGENC
LMI
ANALOG
VDD
GND
VDDE 2V5
VDDE 3V3
GNDE
GNDE 3V3
+1V
+1VTMDS
+3V3TMDS
+2V5-CLKGENA
VDDE-2V5
VDDE-3V3
2V5-LMI
SENSE+1V
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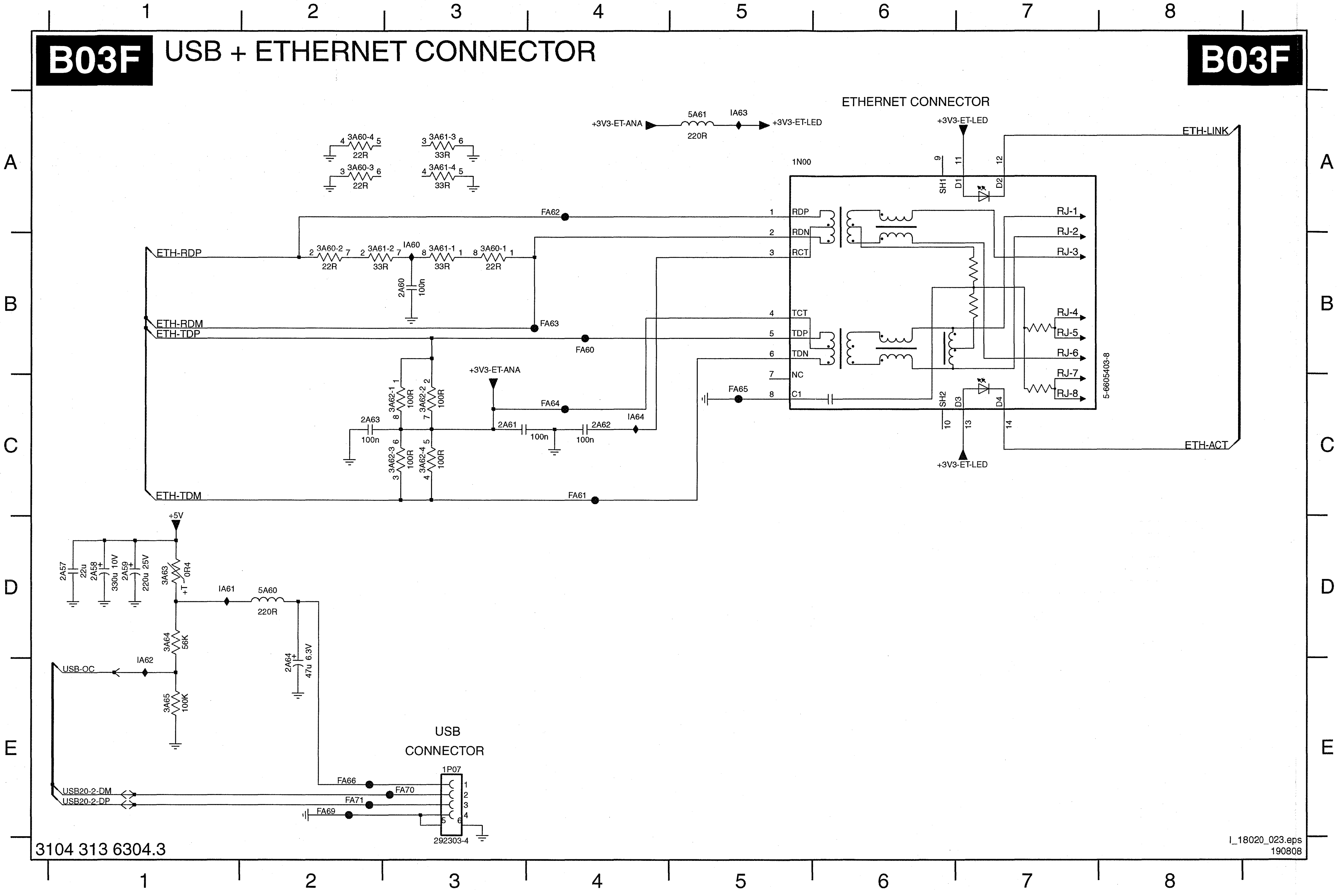
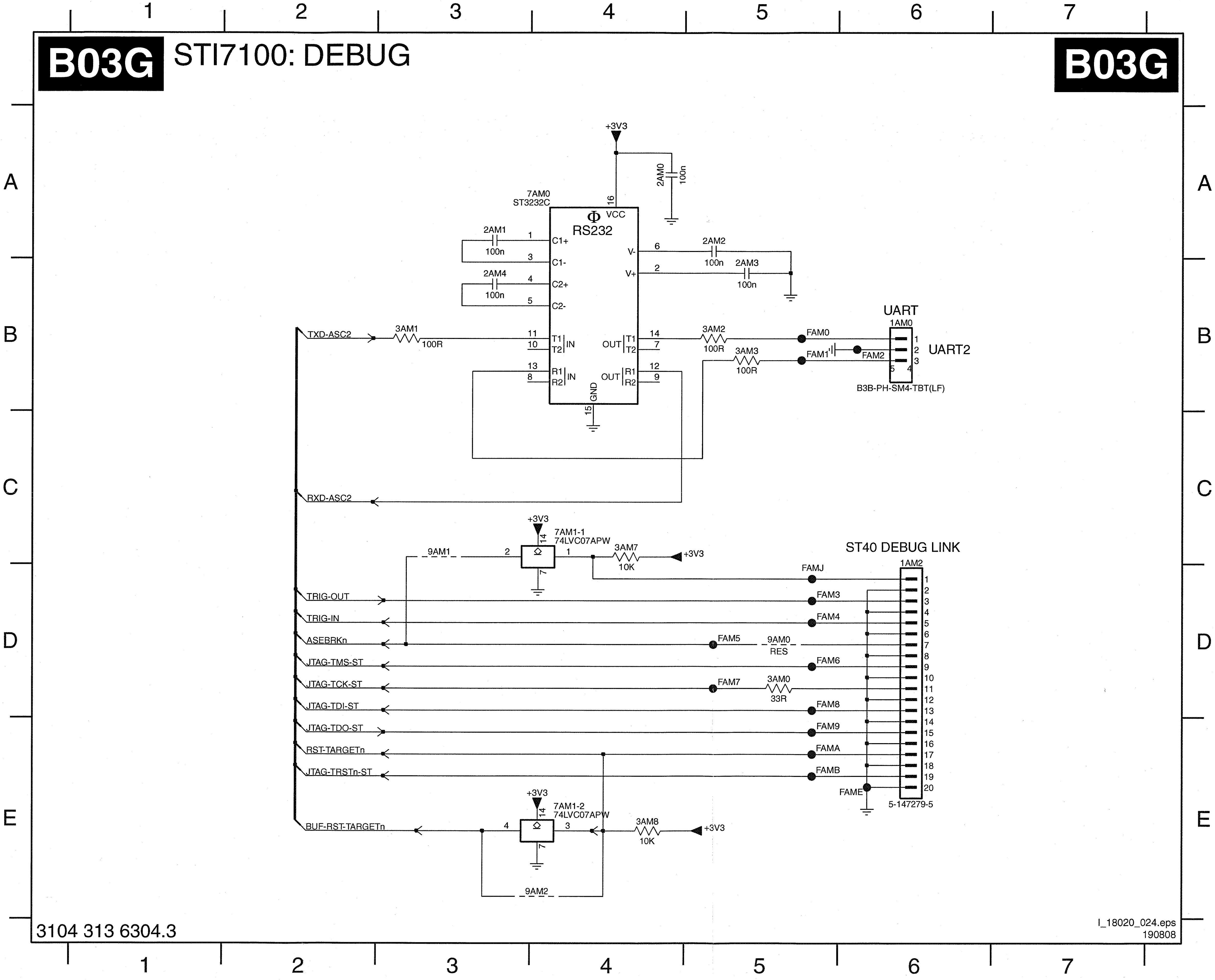
2AE2	D1
2AE5-1	H8
2AE5-2	H9
2AE5-3	H9
2AE5-4	H9
2AE7	D2
2AE8	D1
2AEA	H10
2AEB	D1
2AEC	F12
2AED-1	B1
2AED-2	B1
2AED-3	B1
2AED-4	B1
2AEE	B1
2AEH	G4
2AEJ-1	B2
2AEJ-2	B2
2AEJ-3	B2
2AEJ-4	B2
2AEM	H10
2AEN-1	B3
2AEN-2	B3
2AEN-3	B3
2AEN-4	B3
2AER	H11
2AET	H9
2AEU	H10
2AEZ	H9
2AF0	H10
2AF4	E1
2AF5	E1
2AF8	H11
2AFB	F12
2AFC	F12
2AFD	F12
2AFE	F13
2AFF	F13
2AFG	F13
2AFH	F13
2AFJ	F13
2AFK	F14
2AFL	H11
2AFN-1	B3
2AFN-2	B4
2AFN-3	B4
2AFN-4	B4
2AFR-1	B5
2AFR-2	B5
2AFR-3	B4
2AFR-4	B4
2AFS	H11
2AFT	H12
2AG4-1	E1
2AG4-2	E1
2AG4-3	E2
2AG4-4	E1
2AG5	E2
2AG6	E2
2AG7	E2
2AG8	E3
2AG9	E3
2AGA	E3
2AGB	E3
2AGC	F1
2AGD	F1
2AGG	H4
2AGH	H5
2AGN	E3
2AGP	H11
2AGT	G5
5AE0	E12
5AE2	D1
5AE4	E1
5AE5	H4
5AE7	F1
5AE8	D1
5AE9	G4
7A00-5	A10
7A00-6	A13
7A00-7	A7
IAE1	C1
IAE2	D1
IAE3	E1
IAE4	F1
IAE5	E12
IAE6	B2
IAE8	G4
IAE9	G5
cA00	B2

SSB: STi7100: USB & Ethernet Connector


B03F
USB + ETHERNET CONNECTOR
B03F
ETHERNET CONNECTOR
+3V3-ET-ANA
5A61
220R
IA63
+3V3-ET-LED
1N00
ETH-LINK
ETH-ACT
RDP
RDN
RCT
TCT
TDP
TDN
NC
C1
SH1
SH2
D1
D2
D3
D4
RJ-1
RJ-2
RJ-3
RJ-4
RJ-5
RJ-6
RJ-7
RJ-8
5-6605403-8
3A60-4 22R
3A60-3 22R
3A61-3 33R
3A61-4 33R
ETH-RDP
ETH-RDM
ETH-TDP
ETH-TDM
3A60-2 22R
3A61-2 33R
IA60
3A61-1 33R
3A60-1 22R
2A60 100n
FA60
FA61
FA62
FA63
FA64
FA65
IA64
2A61 100n
2A62 100n
2A63 100n
3A62-1 100R
3A62-2 100R
3A62-3 100R
3A62-4 100R
+5V
2A57 22u
2A58 330u 10V
2A59 220u 25V
3A63 0R4
IA61
5A60 220R
3A64 56K
3A65 100K
IA62
USB-OC
2A64 47u 6.3V
USB CONNECTOR
1P07
292303-4
FA66
FA69
FA70
FA71
USB20-2-DM
USB20-2-DP
3104 313 6304.3
I_18020_023.eps
190808

1N00	A5
1P07	E3
2A57	D1
2A58	D1
2A59	D1
2A60	B3
2A61	C3
2A62	C4
2A63	C2
2A64	E2
3A60-1	B3
3A60-2	B2
3A60-3	A2
3A60-4	A2
3A61-1	B3
3A61-2	B2
3A61-3	A3
3A61-4	A3
3A62-1	C3
3A62-2	C3
3A62-3	C3
3A62-4	C3
3A63	D1
3A64	D1
3A65	E1
5A60	D2
5A61	A5
FA60	B4
FA61	C4
FA62	A4
FA63	B4
FA64	C4
FA65	C5
FA66	E2
FA69	E2
FA70	E3
FA71	E2
IA60	B3
IA61	D1
IA62	E1
IA63	A5
IA64	C4

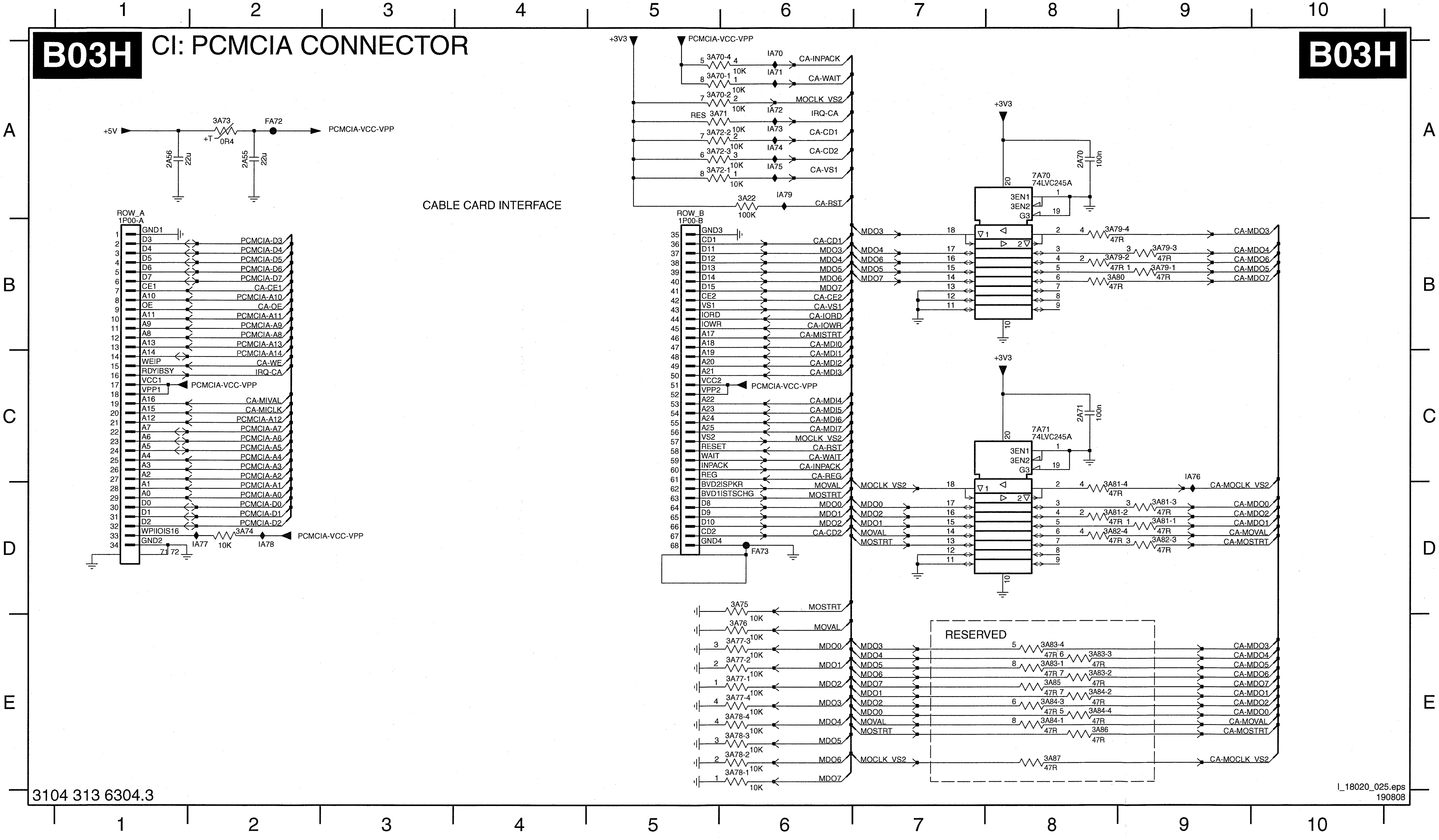
SSB: STi7100: Debug


B03G
STI7100: DEBUG
B03G
1
2
3
4
5
6
7
A
B
C
D
E
+3V3
2AM0
100n
7AM0
ST3232C
16
VCC
RS232
2AM1
100n
1
C1+
3
C1-
2AM4
100n
4
C2+
5
C2-
V-
6
V+
2
2AM2
100n
2AM3
100n
TXD-ASC2
3AM1
100R
11
T1
10
T2
IN
OUT
14
7
3AM2
100R
3AM3
100R
13
R1
8
R2
12
9
15
GND
FAM0
FAM1
FAM2
UART
1AM0
1
2
3
5
4
UART2
B3B-PH-SM4-TBT(LF)
RXD-ASC2
+3V3
7AM1-1
74LVC07APW
14
9AM1
2
1
7
3AM7
10K
+3V3
ST40 DEBUG LINK
FAMJ
1AM2
TRIG-OUT
FAM3
TRIG-IN
FAM4
ASEBRKn
FAM5
9AM0
RES
JTAG-TMS-ST
FAM6
JTAG-TCK-ST
FAM7
3AM0
33R
JTAG-TDI-ST
FAM8
JTAG-TDO-ST
FAM9
RST-TARGETn
FAMA
JTAG-TRSTn-ST
FAMB
FAME
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
5-147279-5
+3V3
7AM1-2
74LVC07APW
14
BUF-RST-TARGETn
4
3
7
3AM8
10K
+3V3
9AM2
3104 313 6304.3
I_18020_024.eps
190808

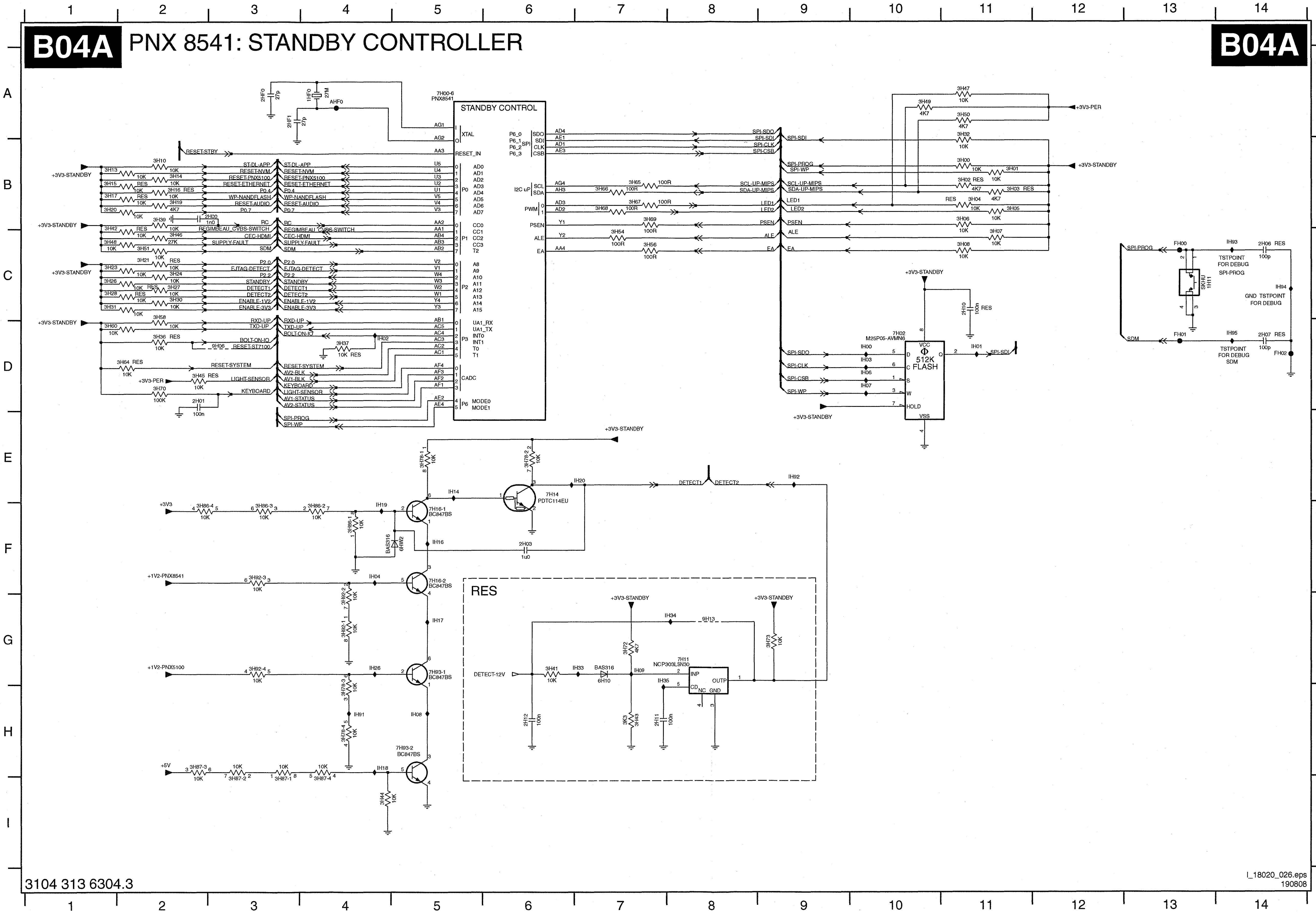
1AM0	B6
1AM2	D6
2AM0	A4
2AM1	A3
2AM2	A5
2AM3	B5
2AM4	B3
3AM0	D5
3AM1	B3
3AM2	B5
3AM3	B5
3AM7	C4
3AM8	E4
7AM0	A4
7AM1-1	C4
7AM1-2	E4
9AM0	D5
9AM1	C3
9AM2	E4
FAM0	B5
FAM1	B5
FAM2	B6
FAM3	D5
FAM4	D5
FAM5	D5
FAM6	D5
FAM7	D5
FAM8	D5
FAM9	E5
FAMA	E5
FAMB	E5
FAME	E6
FAMJ	D5

SSB: CI: PCMCIA Connector

1P00-A	B1
1P00-B	B5
2A55	A2
2A56	A1
2A70	A8
2A71	C8
3A22	A6
3A70-1	A5
3A70-2	A5
3A70-4	A5
3A71	A5
3A72-1	A5
3A72-2	A5
3A72-3	A5
3A73	A2
3A74	D2
3A75	D6
3A76	E6
3A77-1	E6
3A77-2	E6
3A77-3	E6
3A77-4	E6
3A78-1	E6
3A78-2	E6
3A78-3	E6
3A78-4	E6
3A79-1	B9
3A79-2	B8
3A79-3	B9
3A79-4	B8
3A80	B8
3A81-1	D9
3A81-2	D8
3A81-3	D9
3A81-4	D8
3A82-3	D9
3A82-4	D8
3A83-1	E8
3A83-2	E8
3A83-3	E8
3A83-4	E8
3A84-1	E8
3A84-2	E8
3A84-3	E8
3A84-4	E8
3A85	E8
3A86	E8
3A87	E8
7A70	A8
7A71	C8
FA72	A2
FA73	D6
IA70	A6
IA71	A6
IA72	A6
IA73	A6
IA74	A6
IA75	A6
IA76	C9
IA77	D2
IA78	D2
IA79	A6

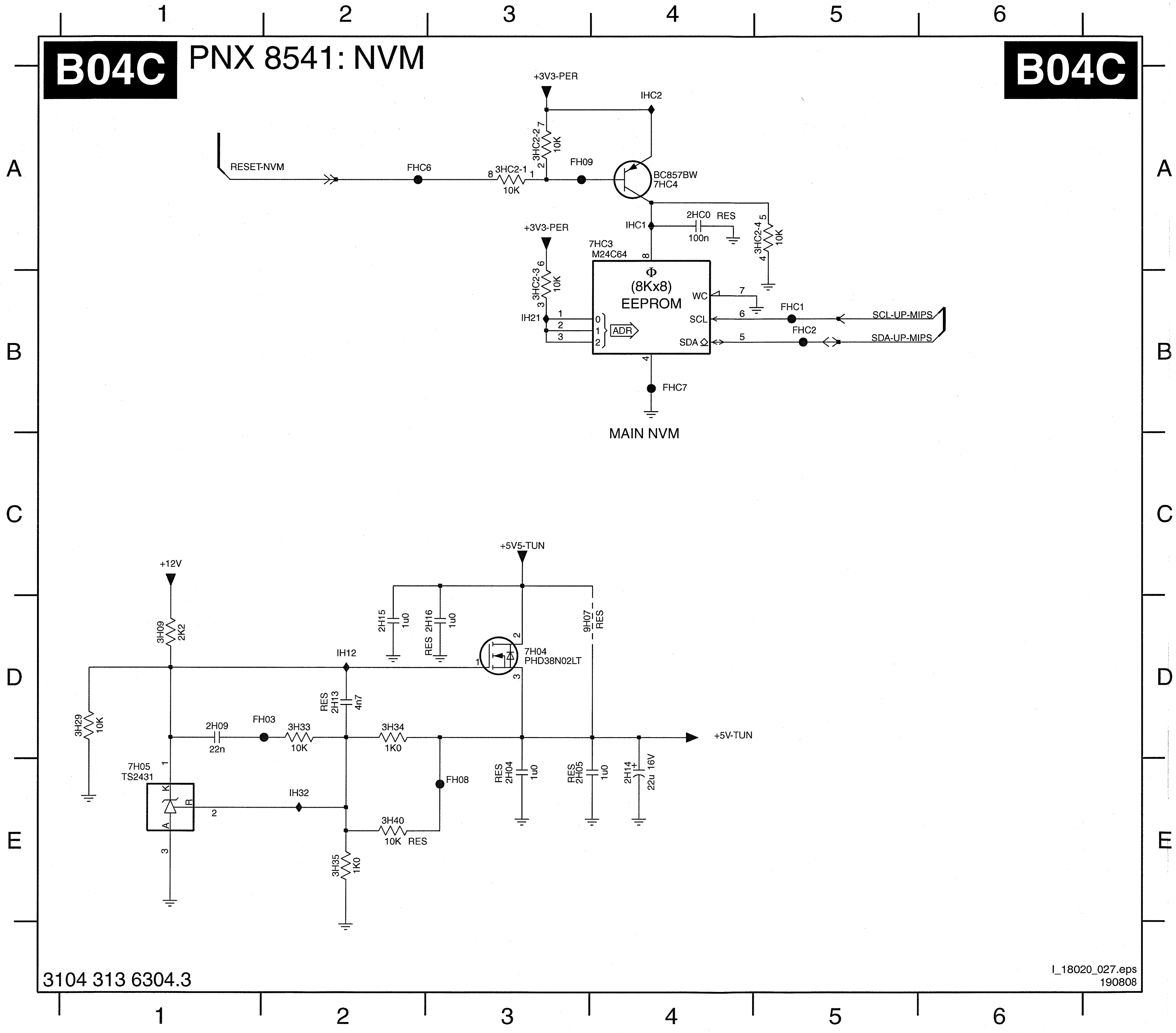

B03H
CI: PCMCIA CONNECTOR
B03H
+5V
3A73
0R4
FA72
PCMCIA-VCC-VPP
2A56 22u
2A55 22u
CABLE CARD INTERFACE
ROW_A
1P00-A
ROW_B
1P00-B
+3V3
PCMCIA-VCC-VPP
CA-INPACK
CA-WAIT
MOCLK_VS2
IRQ-CA
CA-CD1
CA-CD2
CA-VS1
CA-RST
3A22 100K
7A70 74LVC245A
7A71 74LVC245A
2A70 100n
2A71 100n
3EN1
3EN2
G3
IA76
CA-MOCLK_VS2
3A74 10K
IA77
IA78
FA73
RESERVED
MDO0
MDO1
MDO2
MDO3
MDO4
MDO5
MDO6
MDO7
MOVAL
MOSTRT
CA-MDO0
CA-MDO1
CA-MDO2
CA-MDO3
CA-MDO4
CA-MDO5
CA-MDO6
CA-MDO7
CA-MOVAL
CA-MOSTRT
1 2 3 4 5 6 7 8 9 10
A B C D E
3104 313 6304.3
I_18020_025.eps
190808

SSB: PNX8541: Standby Controller


B04A
PNX 8541: STANDBY CONTROLLER
B04A
7H00-6
PNX8541
STANDBY CONTROL
XTAL
RESET_IN
P0
P1
P2
P3
CADC
P6
MODE0
MODE1
SPI
I2C uP
SCL
SDA
PWM
PSEN
ALE
EA
RESET-STBY
ST-DL-APP
RESET-NVM
RESET-PNX5100
RESET-ETHERNET
WP-NANDFLASH
RESET-AUDIO
RC
REGIMBEAU_CVBS-SWITCH
CEC-HDMI
SUPPLY-FAULT
SDM
EJTAG-DETECT
STANDBY
DETECT1
DETECT2
ENABLE-1V2
ENABLE-3V3
RXD-UP
TXD-UP
BOLT-ON-IO
RESET-ST7100
RESET-SYSTEM
AV2-BLK
AV1-BLK
KEYBOARD
LIGHT-SENSOR
AV1-STATUS
AV2-STATUS
SPI-PROG
SPI-WP
SPI-SDO
SPI-SDI
SPI-CLK
SPI-CSB
SCL-UP-MIPS
SDA-UP-MIPS
LED1
LED2
+3V3-STANDBY
+3V3-PER
7H02
M25P05-AVMN6
512K
FLASH
HOLD
TSTPOINT
FOR DEBUG
SPI-PROG
GND TSTPOINT
FOR DEBUG
SDM
+3V3
+1V2-PNX8541
+1V2-PNX5100
+5V
7H16-1
BC847BS
7H16-2
BC847BS
7H93-1
BC847BS
7H93-2
BC847BS
7H14
PDTC114EU
BAS316
DETECT1
DETECT2
RES
DETECT-12V
7H11
NCP303LSN30
INP
OUTP
CD
NC
GND
3104 313 6304.3
I_18020_026.eps
190808

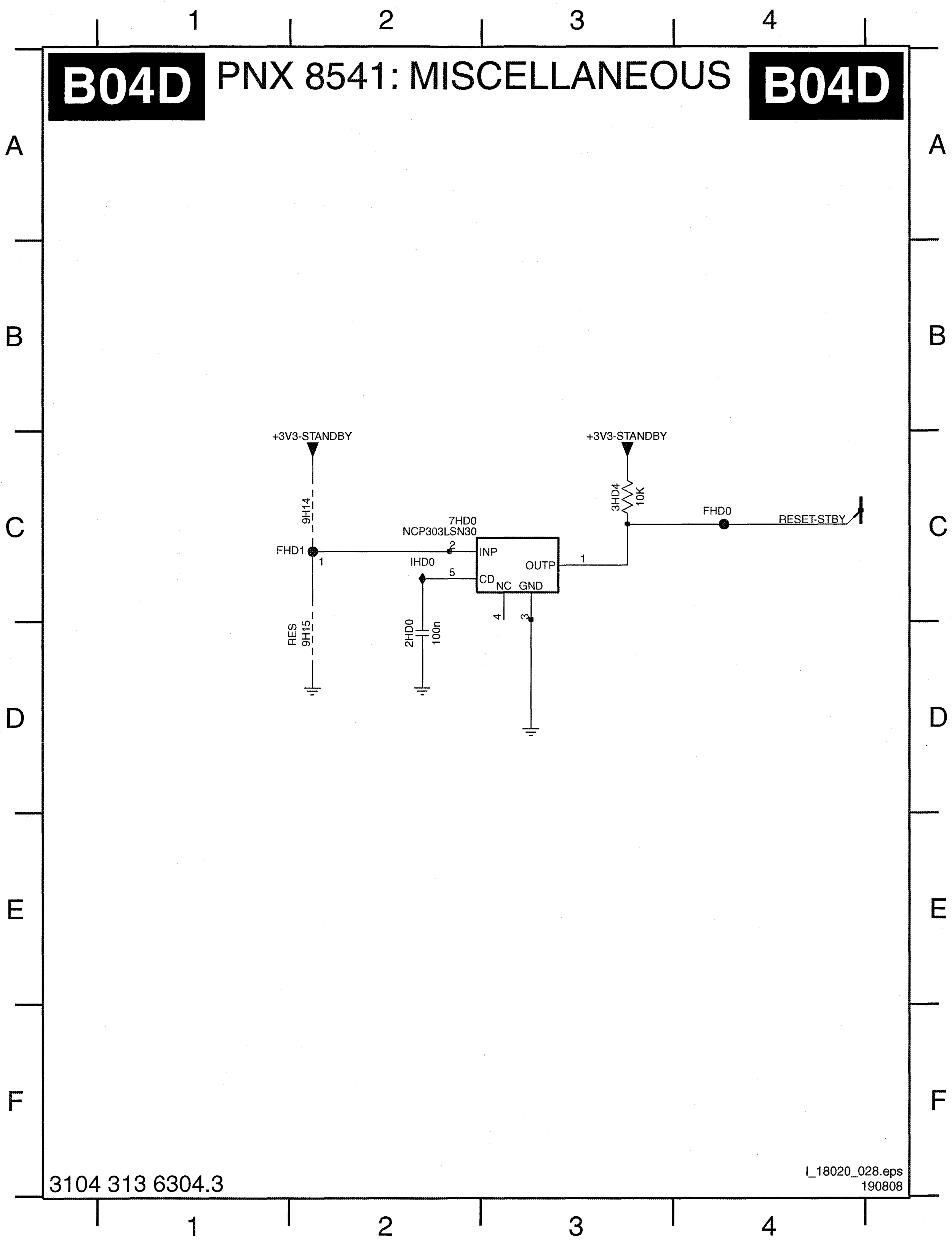
1H11	C13
1HF0	A4
2H00	B3
2H01	D2
2H03	F6
2H06	C14
2H07	D14
2H10	C11
2H11	H7
2H12	H6
2HF0	A3
2HF1	A3
3H00	B11
3H01	B11
3H02	B11
3H03	B11
3H04	B11
3H05	B11
3H06	B11
3H07	C11
3H08	C11
3H10	B2
3H13	B1
3H14	B2
3H15	B1
3H16	B2
3H17	B1
3H19	B2
3H20	B1
3H21	C2
3H23	C1
3H24	C2
3H26	C1
3H27	C2
3H28	C1
3H30	C2
3H31	C1
3H32	A11
3H36	D2
3H37	D4
3H39	B2
3H41	G6
3H42	C1
3H43	H7
3H44	I4
3H45	D2
3H46	C2
3H47	A11
3H48	C1
3H49	A10
3H50	A11
3H51	C2
3H54	C7
3H56	C7
3H58	C2
3H60	D1
3H64	D2
3H65	B7
3H66	B7
3H67	B7
3H68	B7
3H69	B7
3H70	D2
3H72	G7
3H73	G9
3H78-1	E5
3H78-2	E6
3H78-3	H4
3H78-4	H4
3H86-1	F4
3H86-2	F4
3H86-3	F3
3H86-4	F2
3H87-1	H3
3H87-2	H3
3H87-3	H2
3H87-4	H4
3H92-1	G4
3H92-2	G4
3H92-3	F3
3H92-4	G3
6H10	G7
6HW2	F5
7H00-6	A5
7H02	D10
7H11	G8
7H14	E6
7H16-1	F5
7H16-2	F5
7H93-1	G5
7H93-2	H5
9H06	D3
9H13	G8
AHF0	A4
FH00	C13
FH01	D13
FH02	D14
IH00	D10
IH01	D11
IH02	D4
IH03	D10
IH04	F4
IH06	D10
IH07	D10
IH08	H5
IH09	G7
IH14	E5
IH16	F5
IH17	G5
IH18	H4
IH19	F4
IH20	E7
IH26	G4
IH33	G7
IH34	G8
IH35	G7
IH91	H4
IH92	E9
IH93	C14
IH94	C14
IH95	D14

SSB: PNX8541: NVM


1
2
3
4
5
6
A
B
C
D
E
B04C
PNX 8541: NVM
B04C
+3V3-PER
IHC2
RESET-NVM
FHC6
3HC2-2
10K
3HC2-1
10K
FH09
BC857BW
7HC4
IHC1
2HC0 RES
100n
3HC2-4
10K
+3V3-PER
7HC3
M24C64
3HC2-3
10K
Φ
(8Kx8)
EEPROM
WC
SCL
SDA
ADR
IH21
FHC1
FHC2
SCL-UP-MIPS
SDA-UP-MIPS
FHC7
MAIN NVM
+5V5-TUN
+12V
3H09
2K2
2H15
1u0
RES 2H16
1u0
9H07
RES
IH12
7H04
PHD38N02LT
RES
2H13
4n7
3H29
10K
2H09
22n
FH03
3H33
10K
3H34
1K0
+5V-TUN
RES
2H04
1u0
RES
2H05
1u0
2H14
22u 16V
7H05
TS2431
K
R
A
IH32
FH08
3H40
10K RES
3H35
1K0
3104 313 6304.3
I_18020_027.eps
190808

2H04	E3
2H05	E3
2H09	D1
2H13	D2
2H14	E4
2H15	D2
2H16	D3
2HC0	A4
3H09	D1
3H29	D1
3H33	D2
3H34	D2
3H35	E2
3H40	E2
3HC2-1	A3
3HC2-2	A3
3HC2-3	B3
3HC2-4	A5
7H04	D3
7H05	E1
7HC3	A4
7HC4	A4
9H07	D3
FH03	D2
FH08	E3
FH09	A3
FHC1	B5
FHC2	B5
FHC6	A2
FHC7	B4
IH12	D2
IH21	B3
IH32	E2
IHC1	A4
IHC2	A4

SSB: PNX8541: Misc.

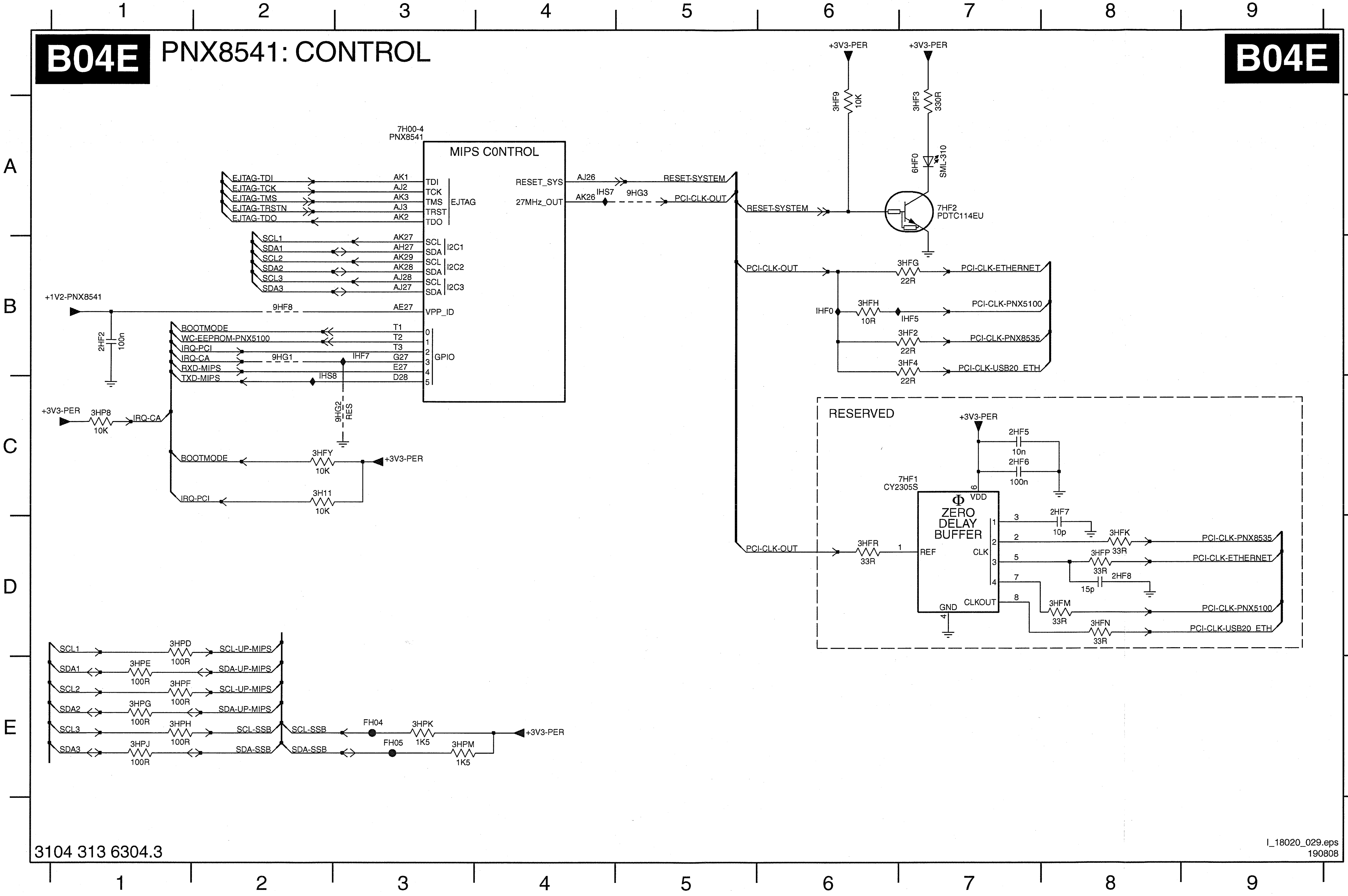

B04D
PNX 8541: MISCELLANEOUS
B04D
1
2
3
4
A
B
C
D
E
F
+3V3-STANDBY
+3V3-STANDBY
9H14
FHD1
1
RES
9H15
7HD0
NCP303LSN30
2
INP
IHD0
5
CD
NC
GND
OUTP
4
3
1
2HD0
100n
3HD4
10K
FHD0
RESET-STBY
3104 313 6304.3
I_18020_028.eps
190808

2HD0	D2
3HD4	C3
7HD0	C2
9H14	C2
9H15	D2
FHD0	C4
FHD1	C2
IHD0	C2

Personal Notes:

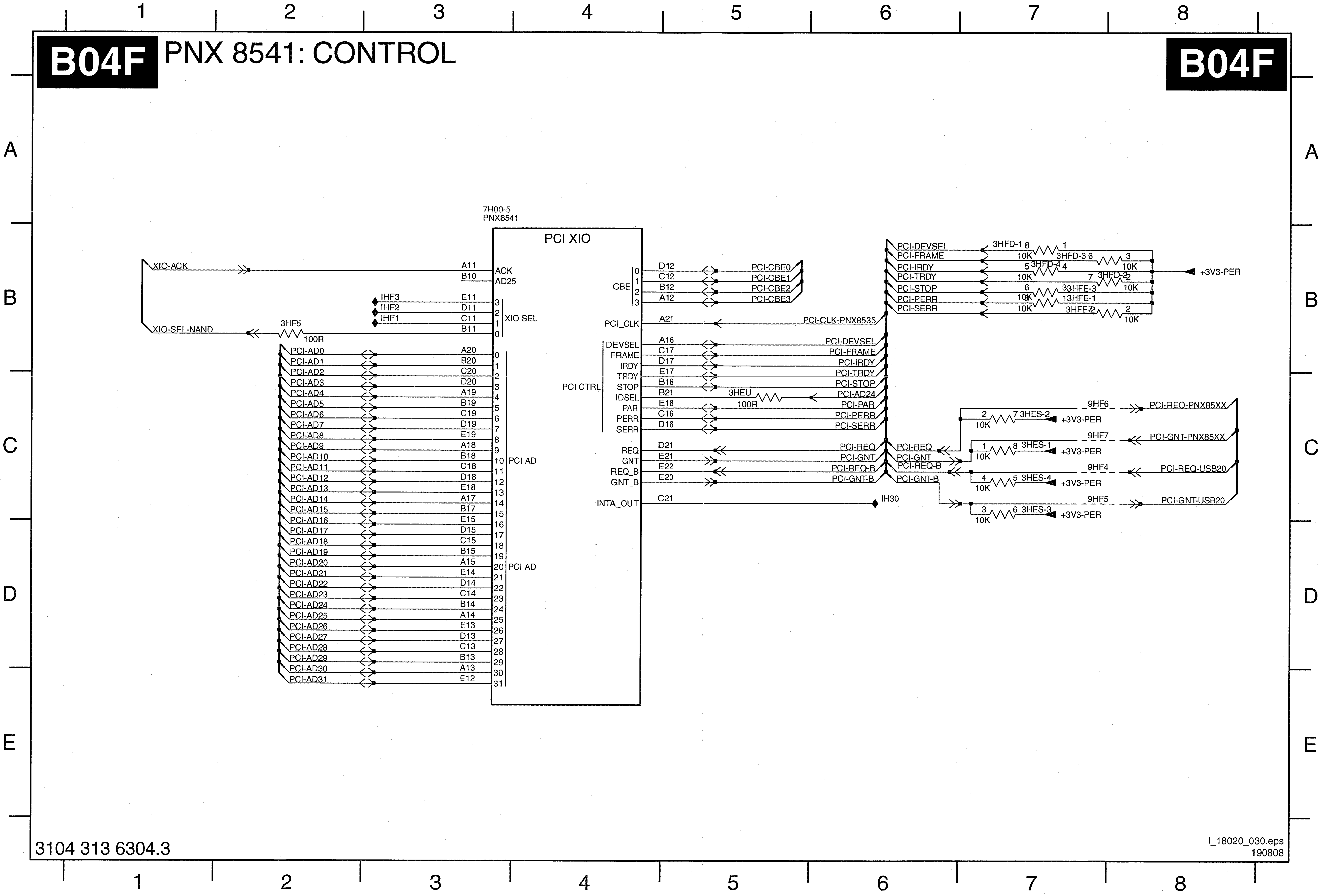
E_06532_012.eps
131004

SSB: PNX8541: Control


B04E
PNX8541: CONTROL
B04E
7H00-4
PNX8541
MIPS CONTROL
EJTAG-TDI
EJTAG-TCK
EJTAG-TMS
EJTAG-TRSTN
EJTAG-TDO
AK1 AJ2 AK3 AJ3 AK2
TDI TCK TMS TRST TDO
EJTAG
SCL1 SDA1 SCL2 SDA2 SCL3 SDA3
AK27 AH27 AK29 AK28 AJ28 AJ27
SCL SDA I2C1
SCL SDA I2C2
SCL SDA I2C3
+1V2-PNX8541
9HF8
AE27
VPP_ID
2HF2 100n
BOOTMODE
WC-EEPROM-PNX5100
IRQ-PCI
IRQ-CA
RXD-MIPS
TXD-MIPS
9HG1
IHF7
IHS8
T1 T2 T3 G27 E27 D28
0 1 2 3 4 5
GPIO
9HG2 RES
+3V3-PER
3HP8 10K
IRQ-CA
BOOTMODE
3HFY 10K
+3V3-PER
IRQ-PCI
3H11 10K
RESET_SYS
27MHz_OUT
AJ26
RESET-SYSTEM
AK26
IHS7
9HG3
PCI-CLK-OUT
+3V3-PER
3HF9 10K
+3V3-PER
3HF3 330R
6HF0
SML-310
RESET-SYSTEM
7HF2
PDTC114EU
PCI-CLK-OUT
3HFG 22R
PCI-CLK-ETHERNET
IHF0
3HFH 10R
IHF5
PCI-CLK-PNX5100
3HF2 22R
PCI-CLK-PNX8535
3HF4 22R
PCI-CLK-USB20_ETH
RESERVED
+3V3-PER
2HF5 10n
2HF6 100n
7HF1
CY2305S
Φ
VDD
ZERO DELAY BUFFER
PCI-CLK-OUT
3HFR 33R
REF
CLK
CLKOUT
GND
2HF7 10p
3HFK 33R
PCI-CLK-PNX8535
3HFP 33R
PCI-CLK-ETHERNET
2HF8 15p
3HFM 33R
PCI-CLK-PNX5100
3HFN 33R
PCI-CLK-USB20_ETH
SCL1
3HPD 100R
SCL-UP-MIPS
SDA1
3HPE 100R
SDA-UP-MIPS
SCL2
3HPF 100R
SCL-UP-MIPS
SDA2
3HPG 100R
SDA-UP-MIPS
SCL3
3HPH 100R
SCL-SSB
SDA3
3HPJ 100R
SDA-SSB
SCL-SSB
FH04
3HPK 1K5
+3V3-PER
SDA-SSB
FH05
3HPM 1K5
3104 313 6304.3
I_18020_029.eps
190808
1 2 3 4 5 6 7 8 9
A B C D E

2HF2	B1
2HF5	C7
2HF6	C7
2HF7	C8
2HF8	D8
3H11	C2
3HF2	B7
3HF3	A7
3HF4	B7
3HF9	A6
3HFG	B7
3HFH	B6
3HFK	D8
3HFM	D8
3HFN	D8
3HFP	D8
3HFR	D6
3HFY	C2
3HP8	C1
3HPD	D1
3HPE	E1
3HPF	E1
3HPG	E1
3HPH	E1
3HPJ	E1
3HPK	E3
3HPM	E3
6HF0	A7
7H00-4	A3
7HF1	C7
7HF2	A7
9HF8	B2
9HG1	B2
9HG2	C3
9HG3	A5
FH04	E3
FH05	E3
IHF0	B6
IHF5	B7
IHF7	B3
IHS7	A4
IHS8	B2

SSB: PNX8541: Control


B04F
PNX 8541: CONTROL
B04F
7H00-5
PNX8541
PCI XIO
XIO-ACK
XIO-SEL-NAND
3HF5
100R
IHF3
IHF2
IHF1
A11 ACK
B10 AD25
E11 3
D11 2
C11 1
B11 0
XIO SEL
PCI-AD0 A20 0
PCI-AD1 B20 1
PCI-AD2 C20 2
PCI-AD3 D20 3
PCI-AD4 A19 4
PCI-AD5 B19 5
PCI-AD6 C19 6
PCI-AD7 D19 7
PCI-AD8 E19 8
PCI-AD9 A18 9
PCI-AD10 B18 10
PCI-AD11 C18 11
PCI-AD12 D18 12
PCI-AD13 E18 13
PCI-AD14 A17 14
PCI-AD15 B17 15
PCI-AD16 E15 16
PCI-AD17 D15 17
PCI-AD18 C15 18
PCI-AD19 B15 19
PCI-AD20 A15 20
PCI-AD21 E14 21
PCI-AD22 D14 22
PCI-AD23 C14 23
PCI-AD24 B14 24
PCI-AD25 A14 25
PCI-AD26 E13 26
PCI-AD27 D13 27
PCI-AD28 C13 28
PCI-AD29 B13 29
PCI-AD30 A13 30
PCI-AD31 E12 31
PCI AD
PCI AD
CBE
0 D12 PCI-CBE0
1 C12 PCI-CBE1
2 B12 PCI-CBE2
3 A12 PCI-CBE3
PCI_CLK A21 PCI-CLK-PNX8535
PCI CTRL
DEVSEL A16 PCI-DEVSEL
FRAME C17 PCI-FRAME
IRDY D17 PCI-IRDY
TRDY E17 PCI-TRDY
STOP B16 PCI-STOP
IDSEL B21 PCI-AD24
3HEU
100R
PAR E16 PCI-PAR
PERR C16 PCI-PERR
SERR D16 PCI-SERR
REQ D21 PCI-REQ
GNT E21 PCI-GNT
REQ_B E22 PCI-REQ-B
GNT_B E20 PCI-GNT-B
INTA_OUT C21
IH30
PCI-DEVSEL
PCI-FRAME
PCI-IRDY
PCI-TRDY
PCI-STOP
PCI-PERR
PCI-SERR
3HFD-1 8 1 10K
3HFD-3 6 3 10K
5 3HFD-4 4 10K
7 3HFD-2 2 10K
6 3 3HFE-3 10K
1 3HFE-1 10K
3HFE-2 2 10K
+3V3-PER
PCI-REQ
PCI-GNT
PCI-REQ-B
PCI-GNT-B
2 7 3HES-2 10K +3V3-PER
1 8 3HES-1 10K +3V3-PER
4 5 3HES-4 10K +3V3-PER
3 6 3HES-3 10K +3V3-PER
9HF6 PCI-REQ-PNX85XX
9HF7 PCI-GNT-PNX85XX
9HF4 PCI-REQ-USB20
9HF5 PCI-GNT-USB20
A B C D E
1 2 3 4 5 6 7 8
3104 313 6304.3
I_18020_030.eps
190808

3HES-1	C7
3HES-2	C7
3HES-3	C7
3HES-4	C7
3HEU	C5
3HF5	B2
3HFD-1	B7
3HFD-2	B8
3HFD-3	B7
3HFD-4	B7
3HFE-1	B7
3HFE-2	B7
3HFE-3	B7
7H00-5	A3
9HF4	C7
9HF5	C7
9HF6	C7
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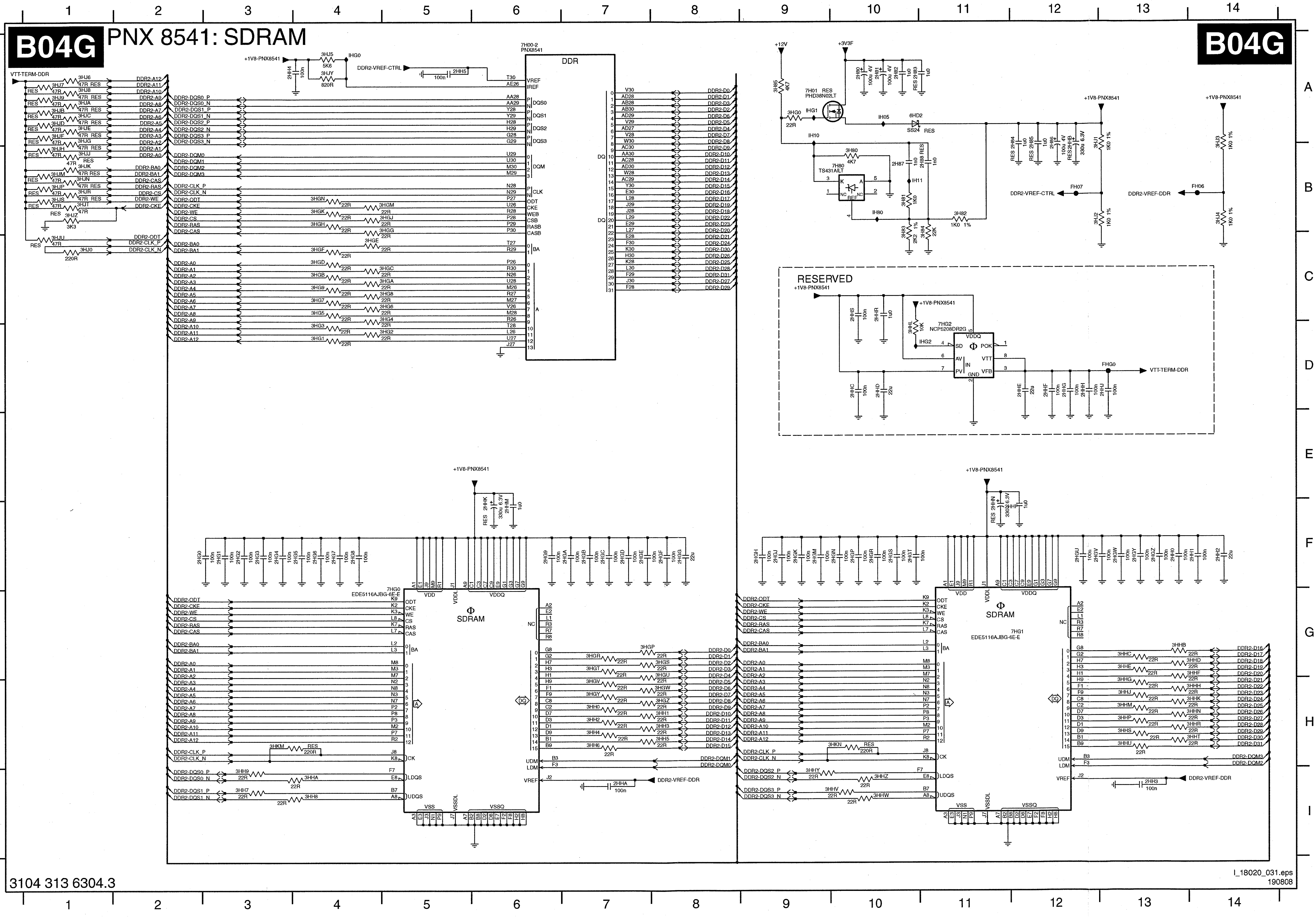
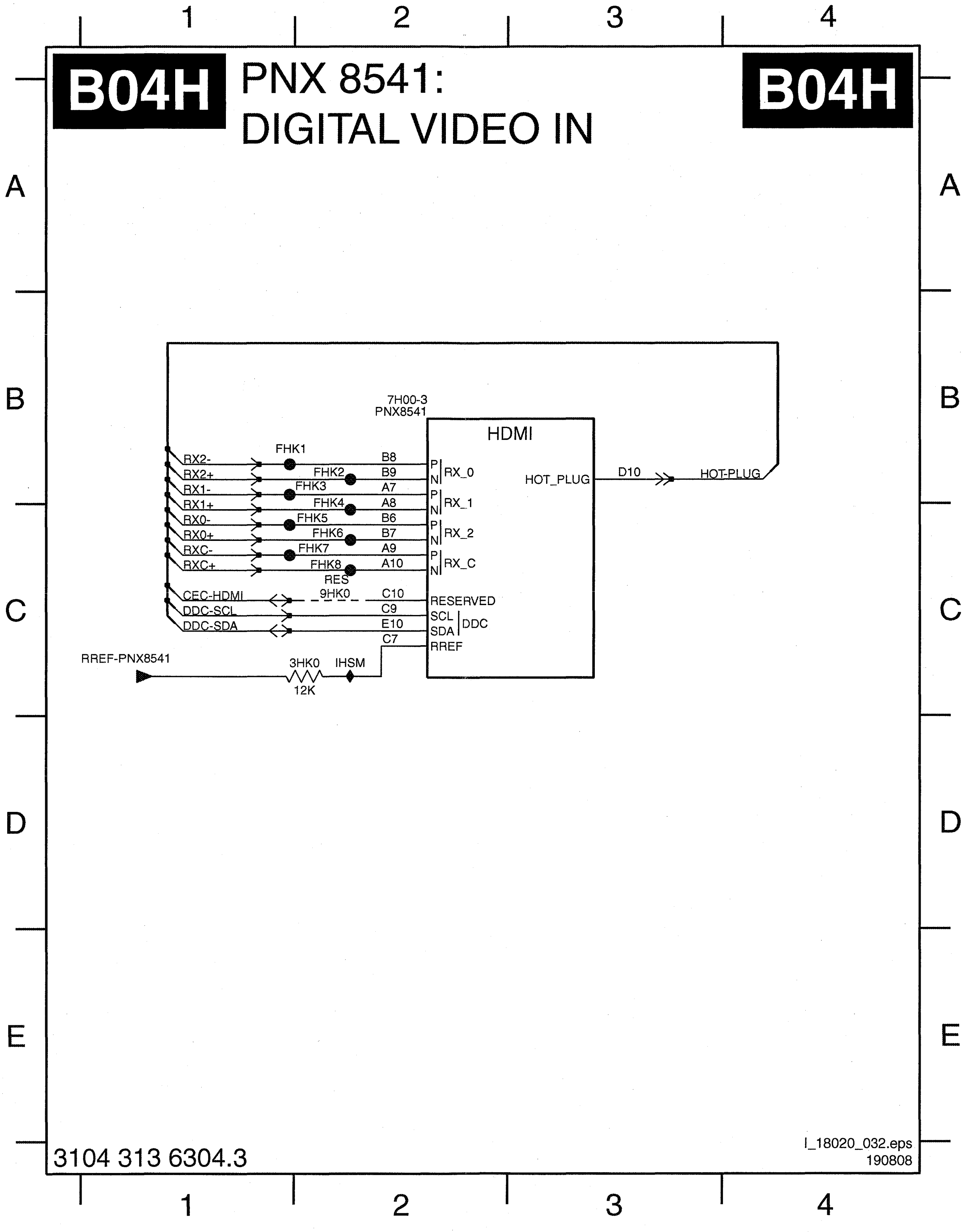
IH30	C6
IHF1	B2
IHF2	B2
IHF3	B2

SSB: PNX8541: SDRAM


B04G
PNX 8541: SDRAM
B04G
7H00-2
PNX8541
DDR
VTT-TERM-DDR
+1V8-PNX8541
DDR2-VREF-CTRL
DDR2-VREF-DDR
+12V
+3V3F
7H01 RES
PHD38N02LT
7H80
TS431AILT
6HD2
SS24 RES
RESERVED
7HG2
NCP5208DR2G
7HG0
EDE5116AJBG-6E-E
SDRAM
7HG1
EDE5116AJBG-6E-E
SDRAM
3104 313 6304.3
I_18020_031.eps
190808

Part	Location
2H80	A10
2H81	A10
2H82	A10
2H83	A10
2H84	A12
2H85	A12
2H86	A12
2H87	B10
2H88	B11
2HG0	F2
2HG1	F3
2HG2	F3
2HG3	F3
2HG4	F3
2HG5	F4
2HG6	F4
2HG7	F4
2HG8	F4
2HG9	F6
2HGA	F7
2HGB	F7
2HGC	F7
2HGD	F7
2HGE	F7
2HGF	F8
2HGG	F8
2HGH	F9
2HGJ	F9
2HGK	F9
2HGM	F9
2HGN	F10
2HGP	F10
2HGR	F10
2HGS	F10
2HGT	F10
2HGU	F12
2HGV	F12
2HGW	F13
2HGY	F13
2HGZ	F13
2HH0	F13
2HH1	F14
2HH2	F14
2HH3	I13
2HH4	A3
2HH5	A5
2HHA	I7
2HHB	A12
2HHC	D10
2HHD	D10
2HHE	D12
2HHF	D12
2HHG	D12
2HHH	D12
2HHJ	D13
2HHK	F6
2HHM	F6
2HHN	F11
2HHP	F12
2HHR	C10
2HHS	C10
3H80	B10
3H81	B10
3H82	B11
3H83	B10
3H84	B11
3H85	A9
3HG0	A9
3HG1	D4
3HG2	D5
3HG3	D4
3HG4	C5
3HG5	C4
3HG6	C5
3HG7	C4
3HG8	C5
3HG9	C4
3HGA	C5
3HGB	C4
3HGC	C5
3HGD	C4
3HGE	C4
3HGF	C4
3HGG	B5
3HGH	B4
3HGJ	B5
3HGK	B4
3HGM	B5
3HGN	B4
3HGP	G7
3HGR	G7
3HGS	G8
3HGT	G7
3HGU	G8
3HGV	H7
3HGW	H8
3HGY	H7
3HGZ	H8
3HH0	H7
3HH1	H8
3HH2	H7
3HH3	H8
3HH4	H7
3HH5	H8
3HH6	H7
3HH7	I3
3HH8	I4
3HH9	I3
3HHA	I4
3HHB	G13
3HHC	G13
3HHD	G14
3HHE	G13
3HHF	G14
3HHG	H13
3HHH	H14
3HHJ	H13
3HHK	H14
3HHL	D10
3HHM	H13
3HHN	H14
3HHP	H13
3HHR	H14
3HHS	H13
3HHT	H14
3HHU	H13
3HHV	I10
3HHW	I10
3HHY	I9
3HHZ	I10
3HJ0	C1
3HJ1	A12
3HJ2	B12
3HJ3	A14
3HJ4	B14
3HJ5	A4
3HJ6	A1
3HJ7	A1
3HJ8	A1
3HJ9	A1
3HJA	A1
3HJB	A1
3HJC	A1
3HJD	A1
3HJE	A1
3HJF	A1
3HJG	A1
3HJH	B1
3HJJ	B1
3HJK	B1
3HJM	B1
3HJN	B1
3HJP	B1
3HJR	B1
3HJS	B1
3HJT	B1
3HJU	C1
3HJY	A4
3HJZ	B1
3HKM	H3
3HKN	H10
6HD2	A10
7H00-2	A6
7H01	A9
7H80	B10
7HG0	G5
7HG1	G12
7HG2	D11
FH06	B14
FH07	B12
FHG0	D13
IH05	A10
IH10	A9
IH11	B10
IH80	B10
IHG0	A4
IHG1	A9
IHG2	D11

SSB: PNX8541: Digital Video In

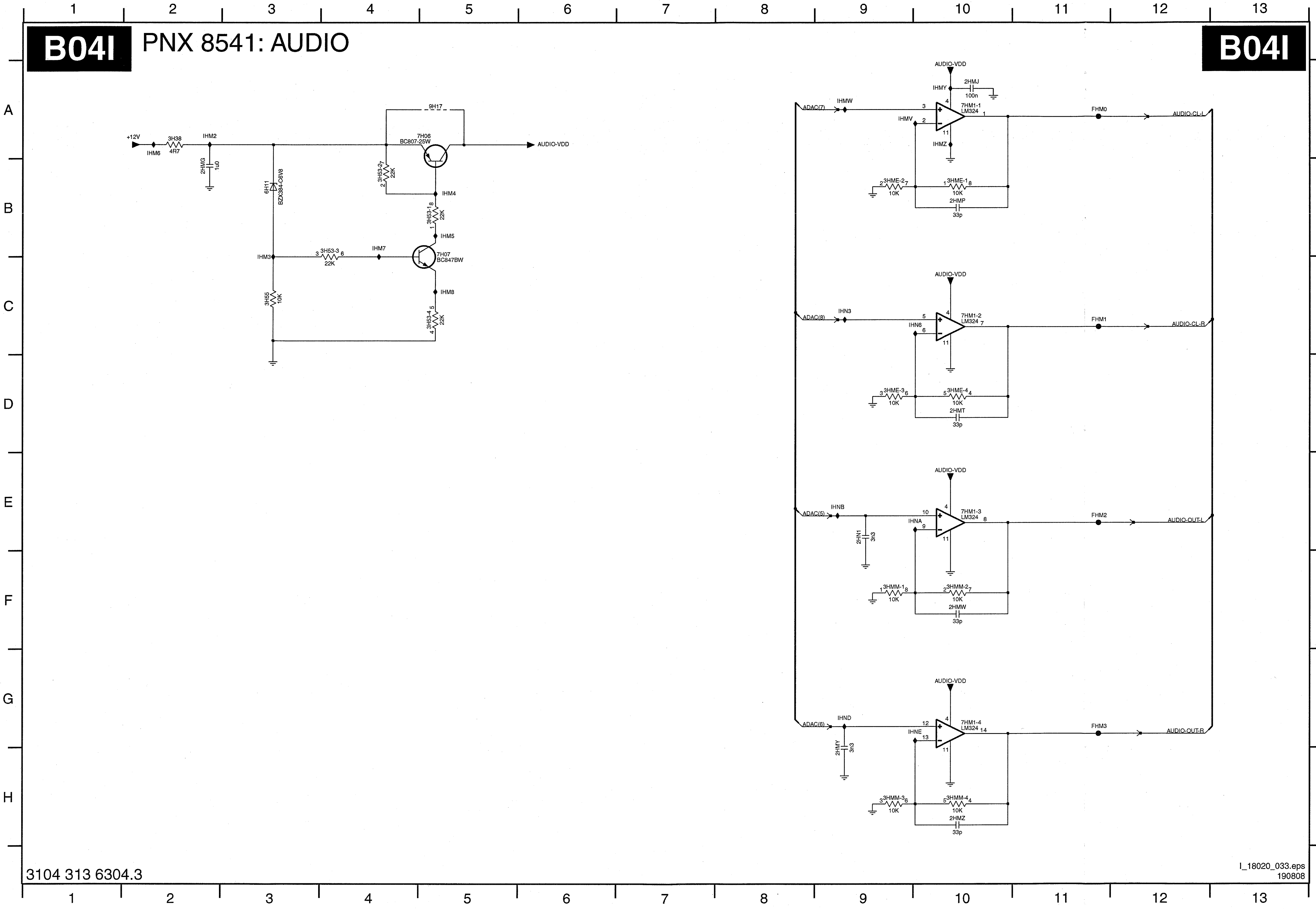

1
2
3
4
A
B
C
D
E
B04H
PNX 8541:
DIGITAL VIDEO IN
B04H
7H00-3
PNX8541
HDMI
RX2-
RX2+
RX1-
RX1+
RX0-
RX0+
RXC-
RXC+
FHK1
FHK2
FHK3
FHK4
FHK5
FHK6
FHK7
FHK8
B8
B9
A7
A8
B6
B7
A9
A10
P
N
RX_0
RX_1
RX_2
RX_C
HOT_PLUG
D10
HOT-PLUG
RES
9HK0
CEC-HDMI
DDC-SCL
DDC-SDA
C10
C9
E10
C7
RESERVED
SCL
SDA
DDC
RREF
RREF-PNX8541
3HK0
12K
IHSM
3104 313 6304.3
I_18020_032.eps
190808

3HK0	C2
7H00-3	B2
9HK0	C2
FHK1	B1
FHK2	B2
FHK3	B2
FHK4	C2
FHK5	C2
FHK6	C2
FHK7	C2
FHK8	C2
IHSM	C2

Personal Notes:

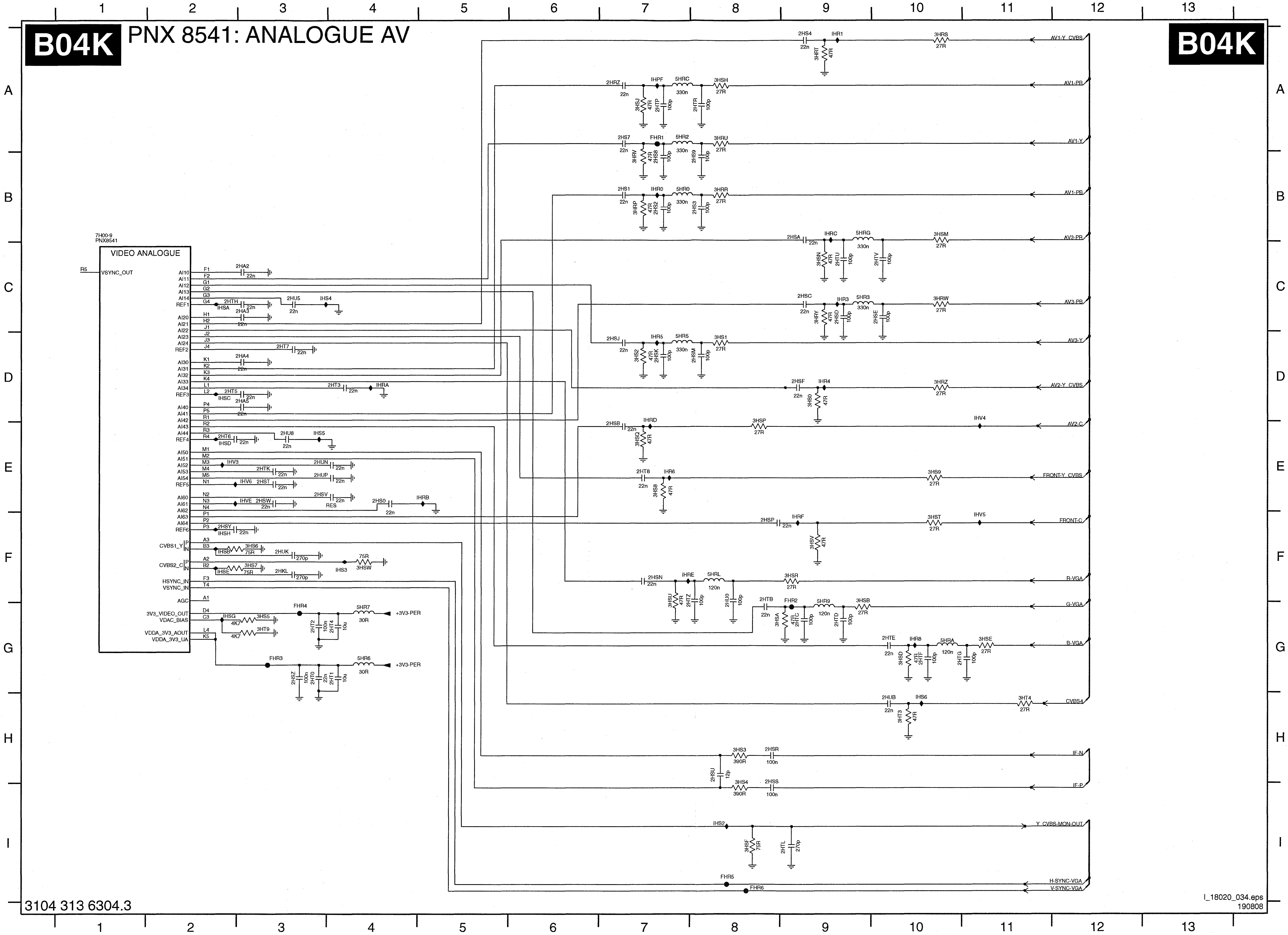
E_06532_012.eps
131004

SSB: PNX8541: Audio


B04I
PNX 8541: AUDIO
B04I
+12V
3H38
4R7
IHM6
IHM2
2HMG
1u0
6H11
BZX384-C6V8
9H17
7H06
BC807-25W
3H53-2
22K
IHM4
3H53-1
22K
IHM5
IHM3
3H53-3
22K
IHM7
7H07
BC847BW
IHM8
3H55
10K
3H53-4
22K
AUDIO-VDD
2HMJ
100n
IHMY
IHMW
ADAC(7)
IHMV
7HM1-1
LM324
IHMZ
3HME-2
10K
3HME-1
10K
2HMP
33p
FHM0
AUDIO-CL-L
IHN3
ADAC(8)
IHN6
7HM1-2
LM324
3HME-3
10K
3HME-4
10K
2HMT
33p
FHM1
AUDIO-CL-R
IHNB
ADAC(5)
IHNA
2HN1
3n3
7HM1-3
LM324
3HMM-1
10K
3HMM-2
10K
2HMW
33p
FHM2
AUDIO-OUT-L
IHND
ADAC(6)
IHNE
2HMY
3n3
7HM1-4
LM324
3HMM-3
10K
3HMM-4
10K
2HMZ
33p
FHM3
AUDIO-OUT-R
3104 313 6304.3
I_18020_033.eps
190808

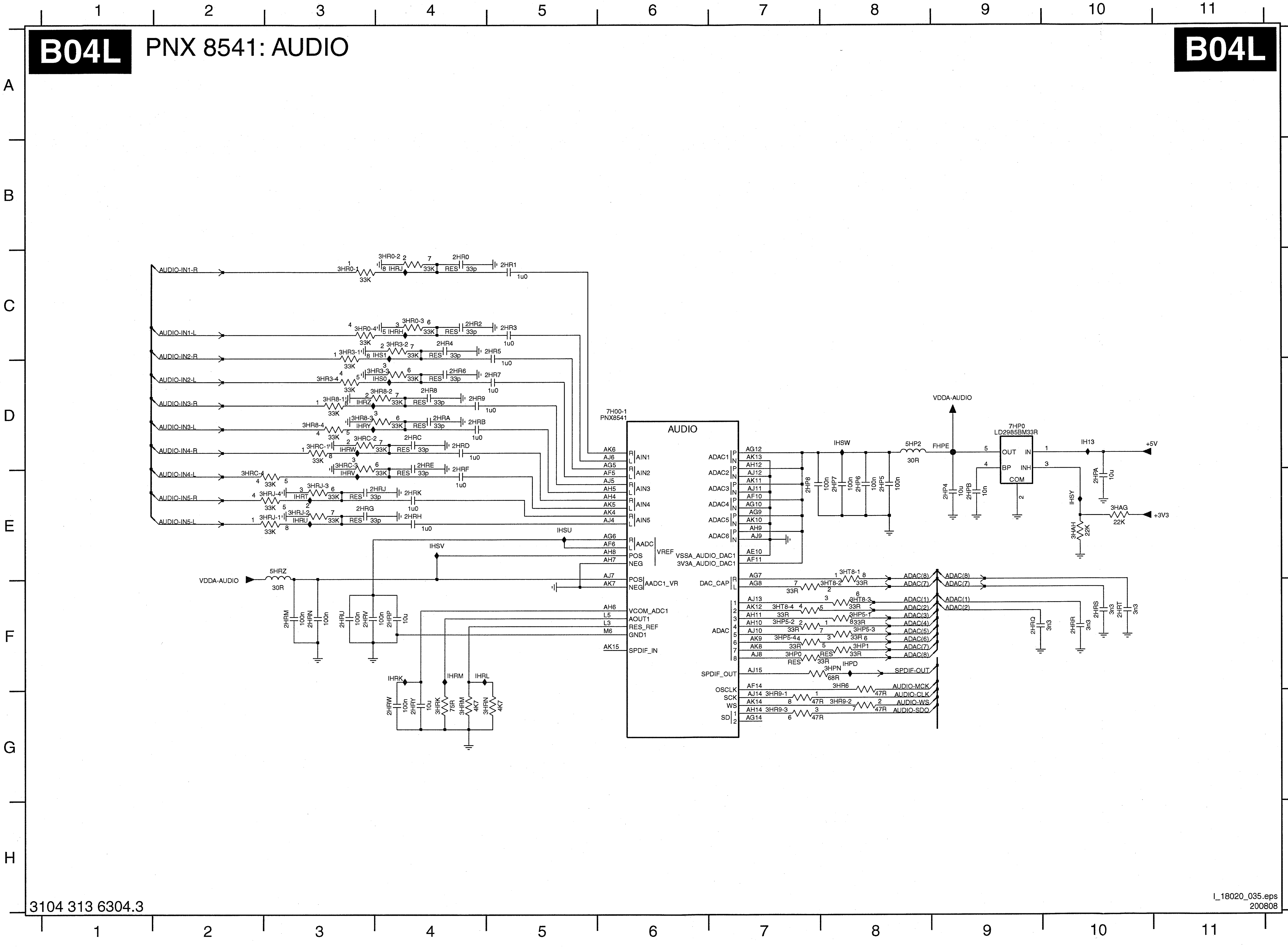
2HMG	B2
2HMJ	A10
2HMP	B10
2HMT	D10
2HMW	F10
2HMY	G9
2HMZ	H10
2HN1	E9
3H38	A2
3H53-1	B5
3H53-2	B4
3H53-3	B4
3H53-4	C5
3H55	C3
3HME-1	B10
3HME-2	B9
3HME-3	D9
3HME-4	D10
3HMM-1	F9
3HMM-2	F10
3HMM-3	H9
3HMM-4	H10
6H11	B3
7H06	A5
7H07	B5
7HM1-1	A10
7HM1-2	C10
7HM1-3	E10
7HM1-4	G10
9H17	A5
FHM0	A11
FHM1	C11
FHM2	E11
FHM3	G11
IHM2	A2
IHM3	B3
IHM4	B5
IHM5	B5
IHM6	A2
IHM7	B4
IHM8	C5
IHMV	A9
IHMW	A9
IHMY	A10
IHMZ	A10
IHN3	C9
IHN6	C10
IHNA	E10
IHNB	E9
IHND	G9
IHNE	G10

SSB: PNX8541: Analogue AV


B04K
PNX 8541: ANALOGUE AV
B04K
7H00-9
PNX8541
VIDEO ANALOGUE
VSYNC_OUT
R5
CVBS1_Y
CVBS2_C
HSYNC_IN
VSYNC_IN
AGC
3V3_VIDEO_OUT
VDAC_BIAS
VDDA_3V3_AOUT
VDDA_3V3_UA
REF1
REF2
REF3
REF4
REF5
REF6
+3V3-PER
AV1-Y_CVBS
AV1-PR
AV1-Y
AV1-PB
AV3-PR
AV3-PB
AV3-Y
AV2-Y_CVBS
AV2-C
FRONT-Y_CVBS
FRONT-C
R-VGA
G-VGA
B-VGA
CVBS4
IF-N
IF-P
Y_CVBS-MON-OUT
H-SYNC-VGA
V-SYNC-VGA
FHR5
FHR6
3104 313 6304.3
I_18020_034.eps
190808
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H I

2HA2	C3
2HA3	C3
2HA4	D3
2HA5	D3
2HKL	F3
2HRZ	A7
2HS0	E4
2HS1	B7
2HS2	B7
2HS3	B8
2HS4	A9
2HS7	A7
2HS8	B7
2HS9	B8
2HSA	B9
2HSB	E7
2HSC	C9
2HSD	C9
2HSE	C10
2HSF	D9
2HSJ	D7
2HSK	D7
2HSM	D8
2HSN	F7
2HSP	F8
2HSR	H8
2HSS	I8
2HST	E3
2HSU	H8
2HSV	E3
2HSW	E3
2HSY	F2
2HSZ	G3
2HT0	G3
2HT1	G4
2HT2	G3
2HT3	D4
2HT4	G4
2HT5	D2
2HT6	E2
2HT7	D3
2HT8	E7
2HTB	F8
2HTC	G9
2HTD	G9
2HTE	G10
2HTF	G10
2HTG	G10
2HTH	C2
2HTK	E3
2HTL	I9
2HTP	A7
2HTR	A8
2HTU	C9
2HTV	C10
2HTZ	F8
2HU0	F8
2HU5	C3
2HU8	E3
2HUB	H10
2HUK	F3
2HUN	E3
2HUP	E3
3HRP	B7
3HRR	B8
3HRS	A10
3HRT	A9
3HRU	A8
3HRV	B7
3HRW	C10
3HRY	C9
3HRZ	D10
3HS0	D9
3HS1	D8
3HS2	D7
3HS3	H8
3HS4	I8
3HS5	G3
3HS6	F3
3HS7	F3
3HS8	E7
3HS9	E10
3HSA	G8
3HSB	G9
3HSD	G10
3HSE	G11
3HSF	I8
3HSH	A8
3HSJ	A7
3HSM	B10
3HSN	C9
3HSP	E8
3HSQ	E7
3HSR	F9
3HST	F10
3HSU	F7
3HSV	F9
3HSW	F4
3HT3	H10
3HT4	H11
3HT9	G3
5HR0	B7
5HR2	A7
5HR3	C9
5HR5	D7
5HR6	G4
5HR7	G4
5HR9	G9
5HRA	G10
5HRC	A7
5HRG	B9
5HRL	F8
7H00-9	B1
FHR1	A7
FHR2	F9
FHR3	G3
FHR4	G3
FHR5	I8
FHR6	I8
IHPF	A7
IHR0	B7
IHR1	A9
IHR3	C9
IHR4	D9
IHR5	D7
IHR6	E7
IHR8	G10
IHRA	D4
IHRB	E5
IHRC	B9
IHRD	D7
IHRE	F7
IHRF	F9
IHS2	I8
IHS3	F4
IHS4	C3
IHS5	E3
IHS6	H10
IHSA	C2
IHSB	F2
IHSC	D2
IHSD	E2
IHSE	F2
IHSG	G2
IHSH	F2
IHV3	E2
IHV4	D11
IHV5	F11
IHV6	E3
IHVE	E3

SSB: PNX8541: Audio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7H00-1
PNX8541
AUDIO
AUDIO-IN1-R
AUDIO-IN1-L
AUDIO-IN2-R
AUDIO-IN2-L
AUDIO-IN3-R
AUDIO-IN3-L
AUDIO-IN4-R
AUDIO-IN4-L
AUDIO-IN5-R
AUDIO-IN5-L
AIN1
AIN2
AIN3
AIN4
AIN5
AADC
VREF
POS
NEG
AADC1_VR
VCOM_ADC1
AOUT1
RES_REF
GND1
SPDIF_IN
ADAC1
ADAC2
ADAC3
ADAC4
ADAC5
ADAC6
VSSA_AUDIO_DAC1
3V3A_AUDIO_DAC1
DAC_CAP
ADAC
SPDIF_OUT
OSCLK
SCK
WS
SD
VDDA-AUDIO
5HRZ
30R
5HP2
30R
FHPE
IHSW
7HP0
LD2985BM33R
OUT
IN
BP
INH
COM
IH13
+5V
3HAG
22K
+3V3
3HAH
22K
IHSY
ADAC(8)
ADAC(7)
ADAC(1)
ADAC(2)
ADAC(3)
ADAC(4)
ADAC(5)
ADAC(6)
SPDIF-OUT
AUDIO-MCK
AUDIO-CLK
AUDIO-WS
AUDIO-SDO
IHSU
IHSV
IHRK
IHRM
IHRL
IHPD
3104 313 6304.3
I_18020_035.eps
200808

2HP4	E9
2HP5	E8
2HP6	E8
2HP7	E8
2HP8	E7
2HPA	E10
2HPB	E9
2HR0	C4
2HR1	C5
2HR2	C4
2HR3	C5
2HR4	C4
2HR5	C5
2HR6	D4
2HR7	D5
2HR8	D4
2HR9	D4
2HRA	D4
2HRB	D4
2HRC	D4
2HRD	D4
2HRE	D4
2HRF	E4
2HRG	E3
2HRH	E4
2HRJ	E4
2HRK	E4
2HRM	F3
2HRN	F3
2HRP	F4
2HRQ	F9
2HRR	F10
2HRS	F10
2HRT	F10
2HRU	F3
2HRV	F3
2HRW	G4
2HRY	G4
3HAG	E10
3HAH	E10
3HP0	F7
3HP1	F8
3HP5-1	F8
3HP5-2	F7
3HP5-3	F8
3HP5-4	F7
3HPN	F8
3HR0-1	C3
3HR0-2	C4
3HR0-3	C4
3HR0-4	C3
3HR3-1	C3
3HR3-2	C4
3HR3-3	D4
3HR3-4	D3
3HR6	F8
3HR8-1	D3
3HR8-2	D4
3HR8-3	D3
3HR8-4	D3
3HR9-1	G8
3HR9-2	G7
3HR9-3	G7
3HRC-1	D3
3HRC-2	D3
3HRC-3	D3
3HRC-4	E2
3HRJ-1	E3
3HRJ-2	E3
3HRJ-3	E3
3HRJ-4	E3
3HRK	G4
3HRM	G4
3HRN	G5
3HT8-1	E8
3HT8-2	F8
3HT8-3	F8
3HT8-4	F7
5HP2	D8
5HRZ	E3
7H00-1	D6
7HP0	D9
FHPE	D9
IH13	D10
IHPD	F8
IHRH	C4
IHRJ	C4
IHRK	F4
IHRL	F4
IHRM	F4
IHRT	E3
IHRU	E3
IHRV	E3
IHRW	D3
IHRY	D3
IHRZ	D3
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IHS1	C4
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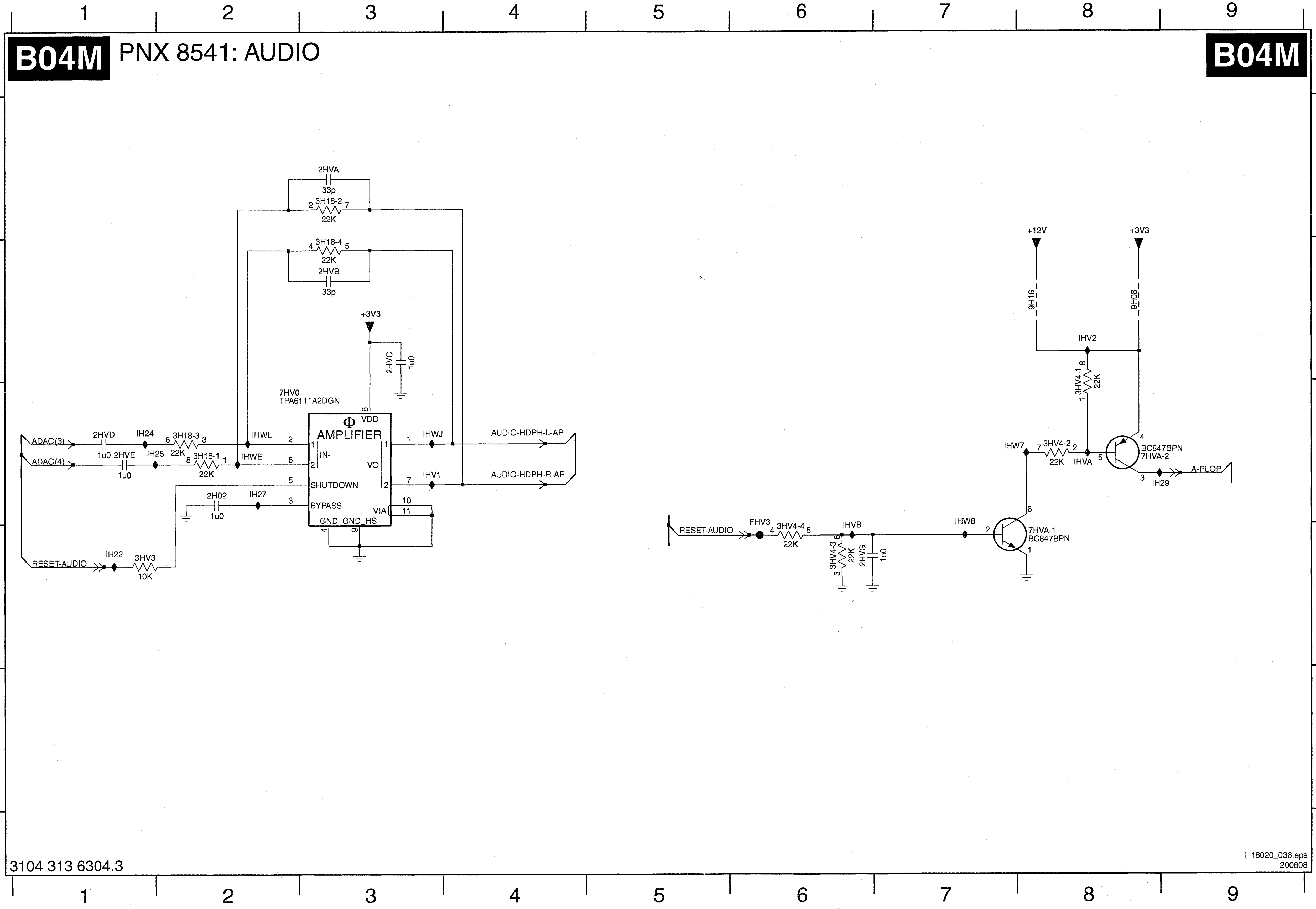
IHSW	D8
IHSY	E10

SSB: PNX8541: Audio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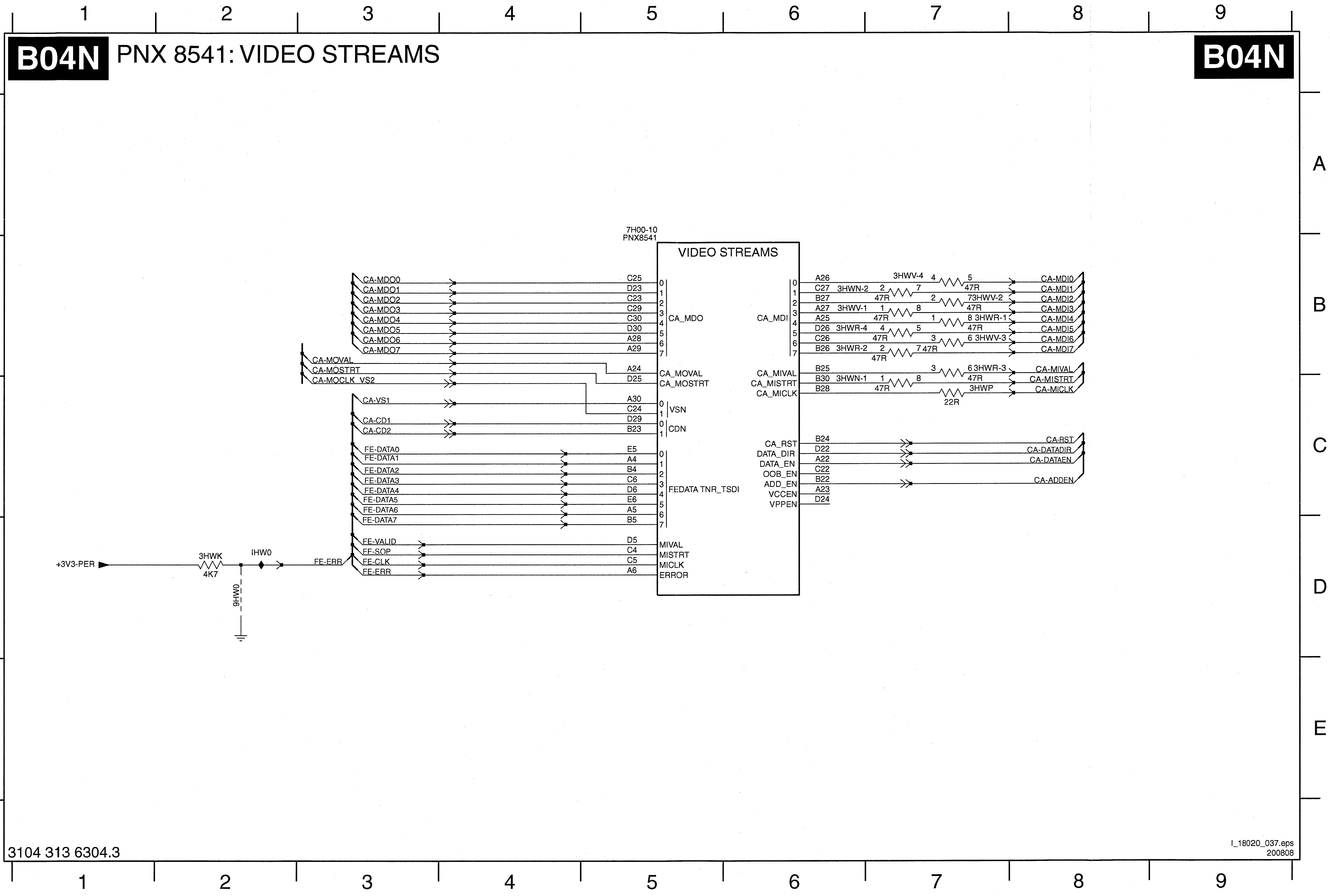
PNX 8541: AUDIO
B04M
1 2 3 4 5 6 7 8 9
A B C D E
2HVA
33p
3H18-2
22K
3H18-4
22K
2HVB
33p
+3V3
2HVC
1u0
7HV0
TPA6111A2DGN
VDD
AMPLIFIER
IN-
VO
SHUTDOWN
BYPASS
VIA
GND GND_HS
ADAC(3)
ADAC(4)
2HVD
1u0
2HVE
1u0
IH24
IH25
3H18-3
22K
3H18-1
22K
IHWL
IHWE
IHWJ
IHV1
AUDIO-HDPH-L-AP
AUDIO-HDPH-R-AP
2H02
1u0
IH27
RESET-AUDIO
IH22
3HV3
10K
+12V
+3V3
9H16
9H08
IHV2
3HV4-1
22K
IHW7
3HV4-2
22K
IHVA
BC847BPN
7HVA-2
IH29
A-PLOP
RESET-AUDIO
FHV3
3HV4-4
22K
IHVB
3HV4-3
22K
2HVG
1n0
IHW8
7HVA-1
BC847BPN
3104 313 6304.3
I_18020_036.eps
200808

2H02	C2
2HVA	A3
2HVB	B3
2HVC	B3
2HVD	C1
2HVE	C1
2HVG	D6
3H18-1	C2
3H18-2	A3
3H18-3	C2
3H18-4	B3
3HV3	D1
3HV4-1	C8
3HV4-2	C8
3HV4-3	D6
3HV4-4	D6
7HV0	C2
7HVA-1	D8
7HVA-2	C8
9H08	B8
9H16	B8
FHV3	D6
IH22	D1
IH24	C1
IH25	C1
IH27	C2
IH29	C8
IHV1	C3
IHV2	B8
IHVA	C8
IHVB	D6
IHW7	C7
IHW8	C7
IHWE	C2
IHWJ	C3
IHWL	C2

SSB: PNX8541: Video Streams



B04N
PNX 8541: VIDEO STREAMS
B04N
7H00-10
PNX8541
VIDEO STREAMS
CA-MDO0
CA-MDO1
CA-MDO2
CA-MDO3
CA-MDO4
CA-MDO5
CA-MDO6
CA-MDO7
C25
D23
C23
C29
C30
D30
A28
A29
CA_MDO
CA-MOVAL
CA-MOSTRT
CA-MOCLK_VS2
A24
D25
CA_MOVAL
CA_MOSTRT
CA-VS1
A30
C24
VSN
CA-CD1
CA-CD2
D29
B23
CDN
FE-DATA0
FE-DATA1
FE-DATA2
FE-DATA3
FE-DATA4
FE-DATA5
FE-DATA6
FE-DATA7
E5
A4
B4
C6
D6
E6
A5
B5
FEDATA TNR_TSDI
FE-VALID
FE-SOP
FE-CLK
FE-ERR
D5
C4
C5
A6
MIVAL
MISTRT
MICLK
ERROR
+3V3-PER
3HWK
4K7
IHW0
9HW0
FE-ERR
CA_MDI
A26
C27
B27
A27
A25
D26
C26
B26
3HWV-4
3HWN-2
3HWV-2
3HWV-1
3HWR-1
3HWR-4
3HWV-3
3HWR-2
47R
CA-MDI0
CA-MDI1
CA-MDI2
CA-MDI3
CA-MDI4
CA-MDI5
CA-MDI6
CA-MDI7
CA_MIVAL
CA_MISTRT
CA_MICLK
B25
B30
B28
3HWR-3
3HWN-1
3HWP
22R
CA-MIVAL
CA-MISTRT
CA-MICLK
CA_RST
DATA_DIR
DATA_EN
OOB_EN
ADD_EN
VCCEN
VPPEN
B24
D22
A22
C22
B22
A23
D24
CA-RST
CA-DATADIR
CA-DATAEN
CA-ADDEN
A
B
C
D
E
1
2
3
4
5
6
7
8
9
3104 313 6304.3
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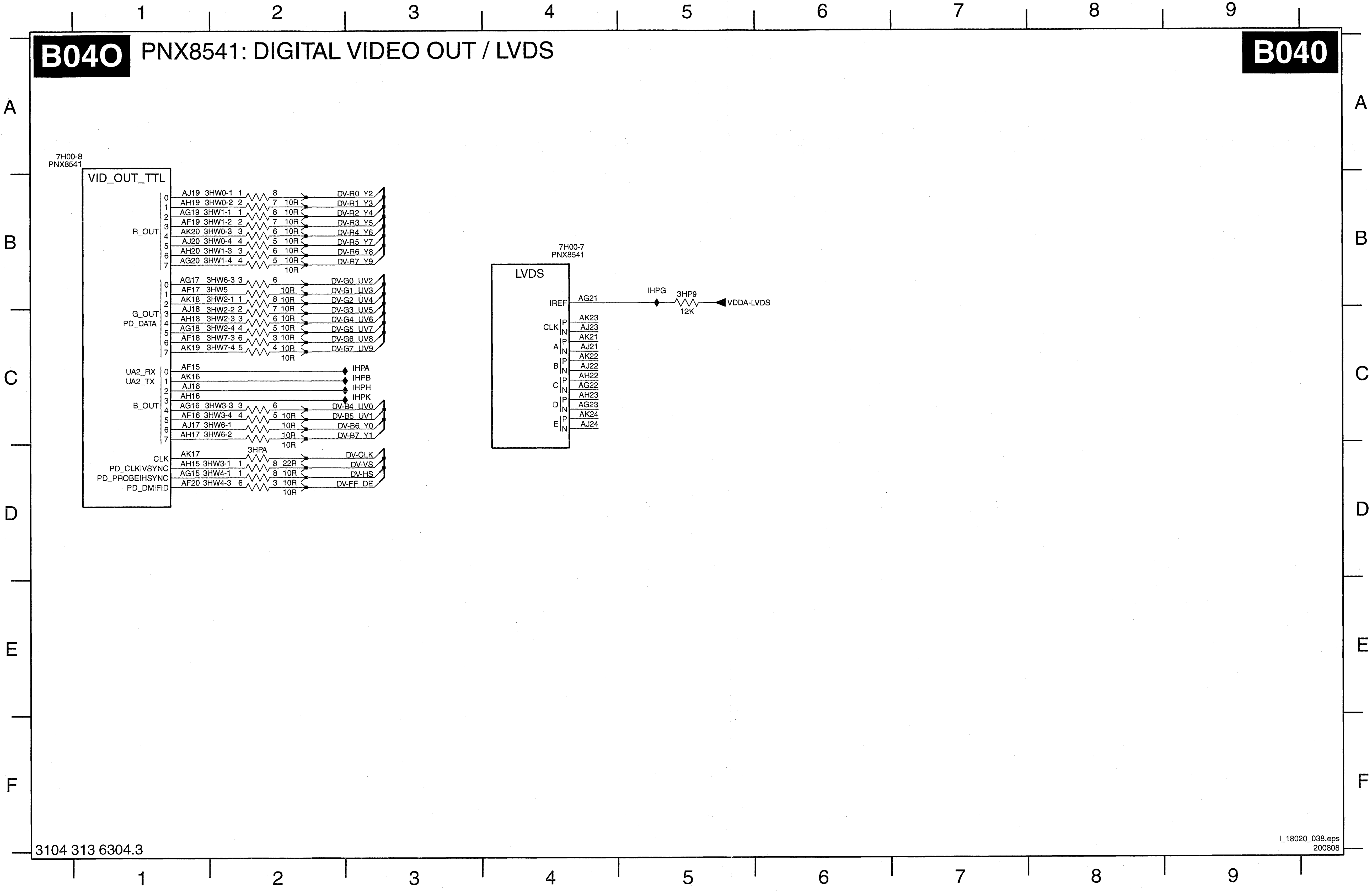
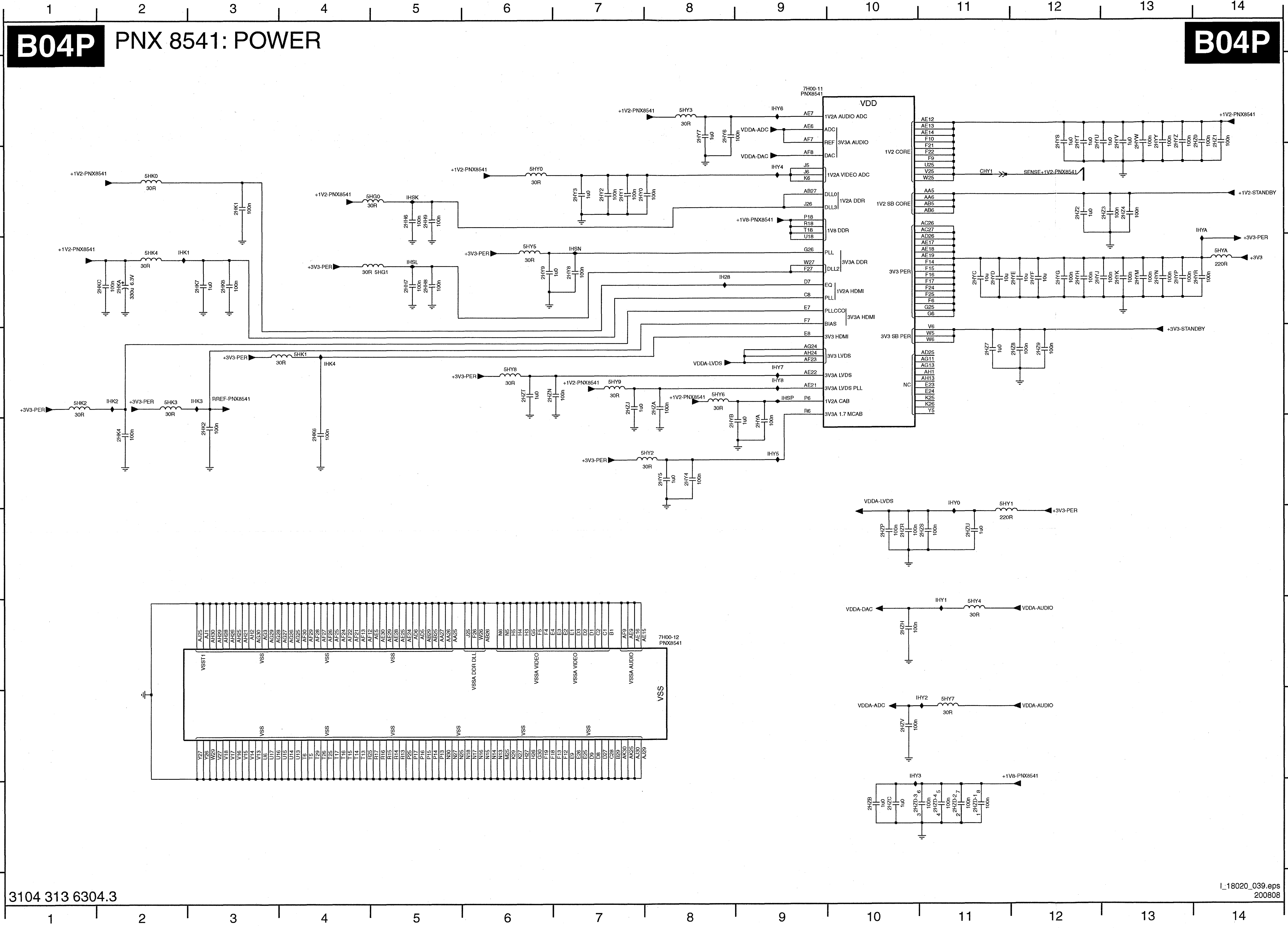
3HWK	D2
3HWN-1	C6
3HWN-2	B6
3HWP	C7
3HWR-1	B7
3HWR-2	B6
3HWR-3	B7
3HWR-4	B6
3HWV-1	B6
3HWV-2	B7
3HWV-3	B7
3HWV-4	B7
7H00-10	A5
9HW0	D2
IHW0	D2

SSB: PNX8541: Digital Video Out / LVDS


B04O
PNX8541: DIGITAL VIDEO OUT / LVDS
B040
7H00-8
PNX8541
VID_OUT_TTL
R_OUT
G_OUT
PD_DATA
UA2_RX
UA2_TX
B_OUT
CLK
PD_CLKIVSYNC
PD_PROBEIHSYNC
PD_DMIFID
AJ19 3HW0-1 DV-R0 Y2
AH19 3HW0-2 DV-R1 Y3
AG19 3HW1-1 DV-R2 Y4
AF19 3HW1-2 DV-R3 Y5
AK20 3HW0-3 DV-R4 Y6
AJ20 3HW0-4 DV-R5 Y7
AH20 3HW1-3 DV-R6 Y8
AG20 3HW1-4 DV-R7 Y9
AG17 3HW6-3 DV-G0 UV2
AF17 3HW5 DV-G1 UV3
AK18 3HW2-1 DV-G2 UV4
AJ18 3HW2-2 DV-G3 UV5
AH18 3HW2-3 DV-G4 UV6
AG18 3HW2-4 DV-G5 UV7
AF18 3HW7-3 DV-G6 UV8
AK19 3HW7-4 DV-G7 UV9
AF15 IHPA
AK16 IHPB
AJ16 IHPH
AH16 IHPK
AG16 3HW3-3 DV-B4 UV0
AF16 3HW3-4 DV-B5 UV1
AJ17 3HW6-1 DV-B6 Y0
AH17 3HW6-2 DV-B7 Y1
AK17 3HPA DV-CLK
AH15 3HW3-1 22R DV-VS
AG15 3HW4-1 DV-HS
AF20 3HW4-3 DV-FF DE
10R
7H00-7
PNX8541
LVDS
IREF AG21
IHPG
3HP9
12K
VDDA-LVDS
CLK P AK23 N AJ23
A P AK21 N AJ21
B P AK22 N AJ22
C P AH22 N AG22
D P AH23 N AG23
E P AK24 N AJ24
3104 313 6304.3
I_18020_038.eps
200808

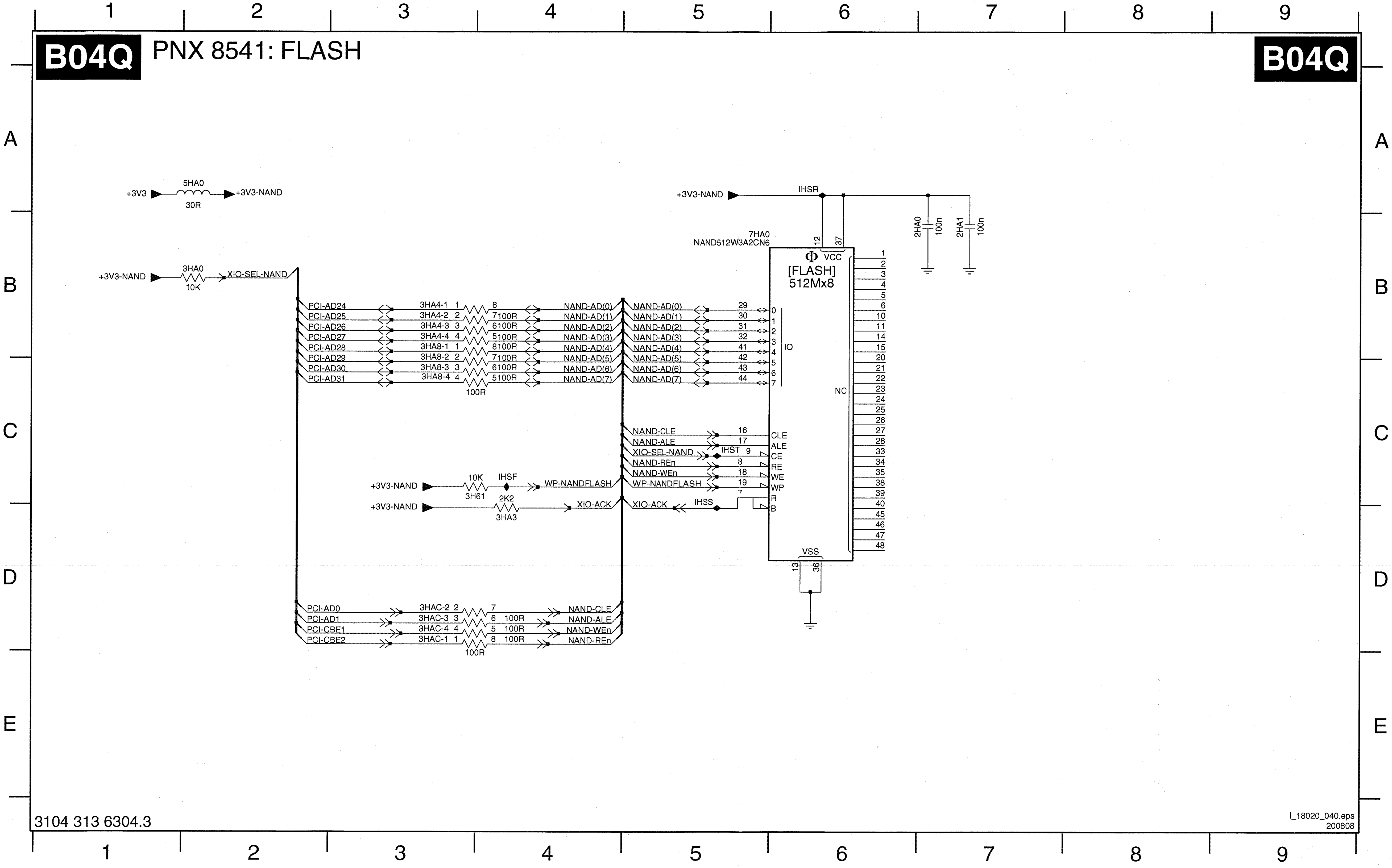
3HP9	B5
3HPA	D2
3HW0-1	B2
3HW0-2	B2
3HW0-3	B2
3HW0-4	B2
3HW1-1	B2
3HW1-2	B2
3HW1-3	B2
3HW1-4	B2
3HW2-1	B2
3HW2-2	C2
3HW2-3	C2
3HW2-4	C2
3HW3-1	D2
3HW3-3	C2
3HW3-4	C2
3HW4-1	D2
3HW4-4	D2
3HW5	B2
3HW6-1	C2
3HW6-2	B2
3HW6-3	C2
3HW7-3	C2
3HW7-4	C2
7H00-7	B4
7H00-8	A1
IHPA	C3
IHPB	C3
IHPG	B5
IHPH	C3
IHPK	C3

SSB: PNX8541: Power


B04P
PNX 8541: POWER
B04P
7H00-11
PNX8541
VDD
1V2A AUDIO ADC
3V3A AUDIO
1V2A VIDEO ADC
1V2A DDR
1V8 DDR
3V3A DDR
1V2A HDMI
3V3A HDMI
3V3 HDMI
3V3 LVDS
3V3A LVDS
3V3A LVDS PLL
1V2A CAB
3V3A 1.7 MCAB
1V2 CORE
1V2 SB CORE
3V3 PER
3V3 SB PER
NC
+1V2-PNX8541
+1V8-PNX8541
+3V3-PER
+3V3
+1V2-STANDBY
+3V3-STANDBY
VDDA-ADC
VDDA-DAC
VDDA-LVDS
VDDA-AUDIO
RREF-PNX8541
SENSE+1V2-PNX8541
CHY1
7H00-12
PNX8541
VSS
VSSA DDR DLL
VSSA VIDEO
VSSA AUDIO
VSST1
3104 313 6304.3
I_18020_039.eps
200808

2HH6	B5
2HH7	C5
2HH8	C5
2HH9	B5
2HK1	B3
2HK2	E3
2HK4	E2
2HK6	E4
2HK7	C3
2HK8	C3
2HKA	C2
2HKC	C2
2HY0	B7
2HY1	B7
2HY2	B7
2HY3	B7
2HY4	E8
2HY5	E8
2HY6	A8
2HY7	A8
2HY8	C7
2HY9	C6
2HYA	E9
2HYB	E8
2HYC	C11
2HYD	C11
2HYE	C12
2HYF	C12
2HYG	C12
2HYH	C12
2HYJ	C12
2HYK	C13
2HYM	C13
2HYN	C13
2HYP	C13
2HYR	C14
2HYS	A12
2HYT	A12
2HYU	A12
2HYV	A13
2HYW	A13
2HYY	A13
2HYZ	A13
2HZ0	A14
2HZ1	A14
2HZ2	B12
2HZ3	B13
2HZ4	B13
2HZ7	D11
2HZ8	D12
2HZ9	D12
2HZA	D8
2HZB	I10
2HZC	I10
2HZD-1	I11
2HZD-2	I11
2HZD-3	I10
2HZD-4	I11
2HZH	G10
2HZJ	D7
2HZN	D6
2HZP	F10
2HZR	F10
2HZS	F11
2HZT	D6
2HZU	F11
2HZV	H10
5HG0	B5
5HG1	C5
5HK0	B2
5HK1	D4
5HK2	D1
5HK3	D2
5HK4	C2
5HY0	B6
5HY1	E11
5HY2	E8
5HY3	A8
5HY4	G11
5HY5	C6
5HY6	D8
5HY7	H11
5HY8	D6
5HY9	D7
5HYA	C14
7H00-11	A9
7H00-12	G8
CHY1	B11
IH28	C8
IHK1	C2
IHK2	D2
IHK3	D3
IHK4	D4
IHSK	B5
IHSL	C5
IHSN	C7
IHSP	D9
IHY0	E11
IHY1	G11
IHY2	H11
IHY3	H10
IHY4	B9
IHY5	E9
IHY6	A9
IHY7	D9
IHY8	D9
IHYA	B14

SSB: PNX8541: Flash


B04Q
PNX 8541: FLASH
B04Q
+3V3
5HA0
30R
+3V3-NAND
+3V3-NAND
3HA0
10K
XIO-SEL-NAND
PCI-AD24
PCI-AD25
PCI-AD26
PCI-AD27
PCI-AD28
PCI-AD29
PCI-AD30
PCI-AD31
3HA4-1
3HA4-2
3HA4-3
3HA4-4
3HA8-1
3HA8-2
3HA8-3
3HA8-4
100R
NAND-AD(0)
NAND-AD(1)
NAND-AD(2)
NAND-AD(3)
NAND-AD(4)
NAND-AD(5)
NAND-AD(6)
NAND-AD(7)
+3V3-NAND
IHSR
7HA0
NAND512W3A2CN6
VCC
[FLASH]
512Mx8
IO
NC
VSS
CLE
ALE
CE
RE
WE
WP
R
B
2HA0
100n
2HA1
100n
NAND-CLE
NAND-ALE
XIO-SEL-NAND
NAND-REn
NAND-WEn
WP-NANDFLASH
XIO-ACK
IHST
IHSS
+3V3-NAND
10K
3H61
IHSF
WP-NANDFLASH
+3V3-NAND
2K2
3HA3
XIO-ACK
PCI-AD0
PCI-AD1
PCI-CBE1
PCI-CBE2
3HAC-2
3HAC-3
3HAC-4
3HAC-1
100R
NAND-CLE
NAND-ALE
NAND-WEn
NAND-REn
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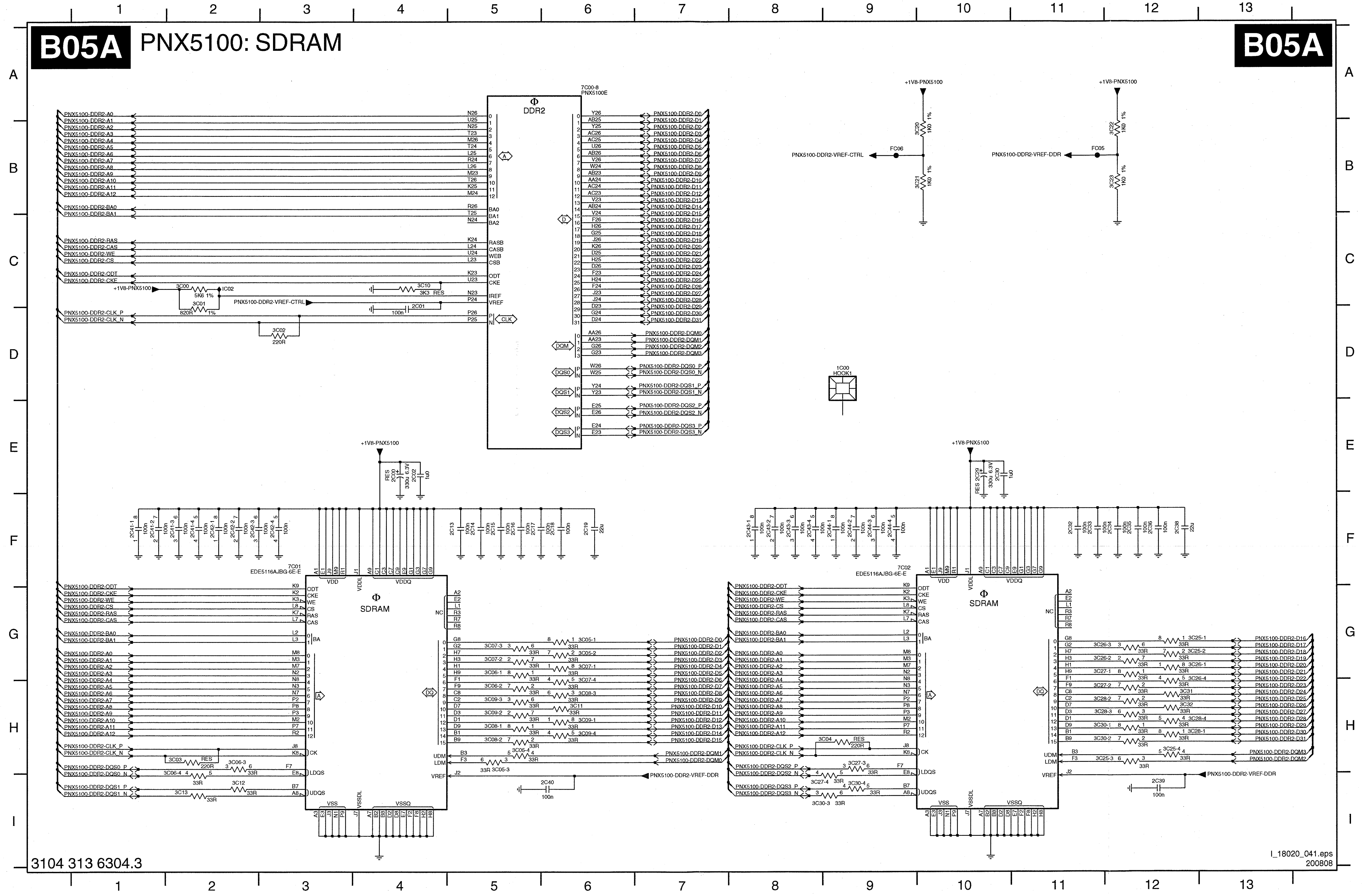
2HA0	B7
2HA1	B7
3H61	C3
3HA0	B2
3HA3	D4
3HA4-1	B3
3HA4-2	B3
3HA4-3	B3
3HA4-4	B3
3HA8-1	B3
3HA8-2	C3
3HA8-3	C3
3HA8-4	C3
3HAC-1	D3
3HAC-2	D3
3HAC-3	D3
3HAC-4	D3
5HA0	A2
7HA0	B5
IHSF	C4
IHSR	A6
IHSS	C5
IHST	C5

SSB: PNX5100: SDRAM


B05A
PNX5100: SDRAM
B05A
7C00-8
PNX5100E
DDR2
PNX5100-DDR2-A0 … PNX5100-DDR2-A12
PNX5100-DDR2-BA0
PNX5100-DDR2-BA1
PNX5100-DDR2-RAS
PNX5100-DDR2-CAS
PNX5100-DDR2-WE
PNX5100-DDR2-CS
PNX5100-DDR2-ODT
PNX5100-DDR2-CKE
PNX5100-DDR2-CLK_P
PNX5100-DDR2-CLK_N
PNX5100-DDR2-D0 … PNX5100-DDR2-D31
PNX5100-DDR2-DQM0 … PNX5100-DDR2-DQM3
PNX5100-DDR2-DQS0_P … PNX5100-DDR2-DQS3_N
PNX5100-DDR2-VREF-CTRL
PNX5100-DDR2-VREF-DDR
+1V8-PNX5100
1C00
HOOK1
7C01
EDE5116AJBG-6E-E
7C02
EDE5116AJBG-6E-E
SDRAM
VDD
VDDL
VDDQ
VSS
VSSDL
VSSQ
LDQS
UDQS
LDM
UDM
VREF
3104 313 6304.3
I_18020_041.eps
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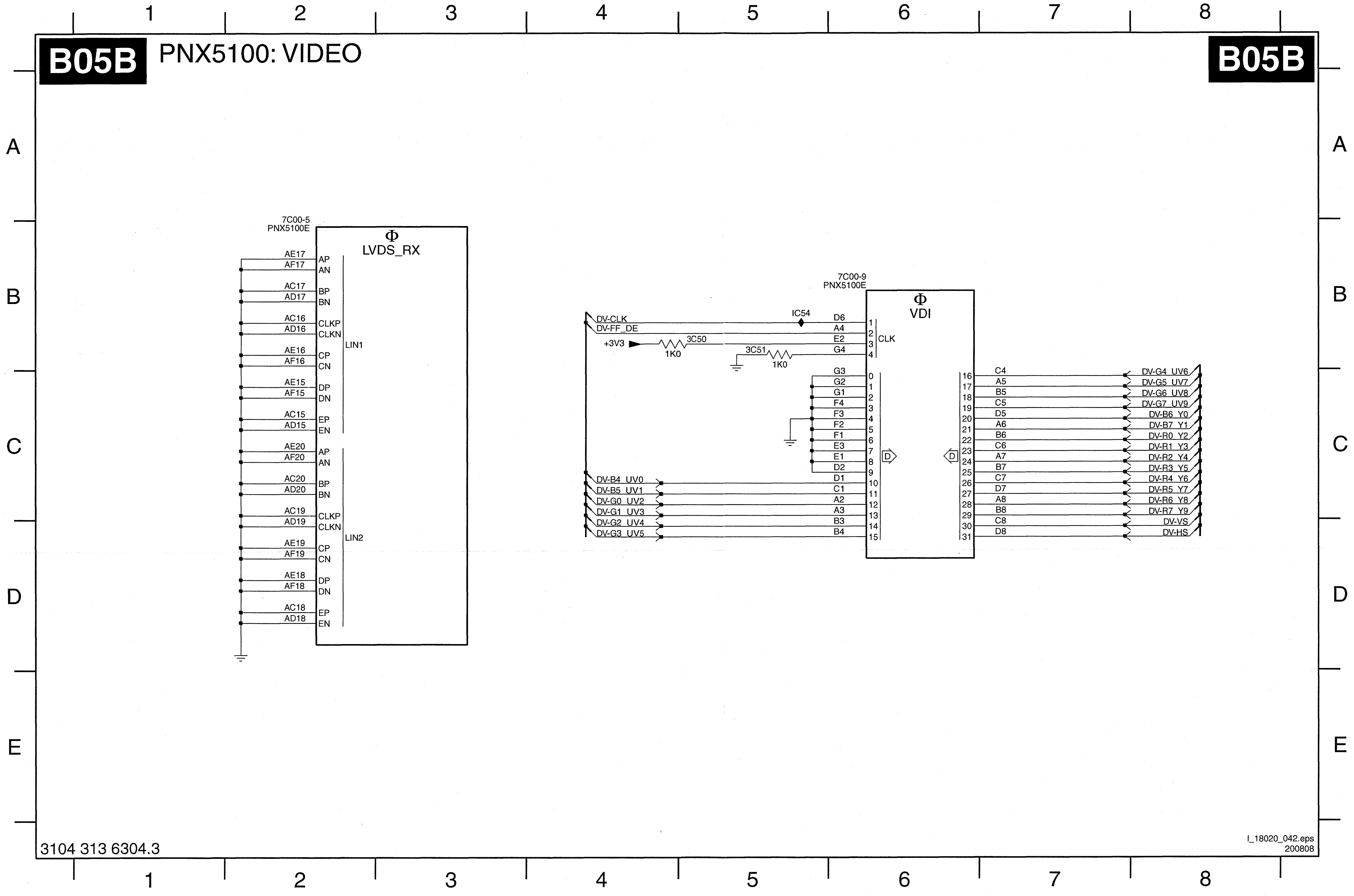
1C00	D9
2C00	E4
2C01	D4
2C02	E4
2C13	F5
2C14	F5
2C15	F5
2C16	F5
2C17	F5
2C18	F6
2C19	F6
2C29	E10
2C30	E10
2C32	F11
2C33	F11
2C34	F12
2C35	F12
2C36	F12
2C38	F12
2C39	I12
2C40	I6
2C41-1	F1
2C41-2	F1
2C41-3	F2
2C41-4	F2
2C42-1	F2
2C42-2	F2
2C42-3	F2
2C42-4	F3
2C43-1	F8
2C43-2	F8
2C43-3	F8
2C43-4	F8
2C44-1	F9
2C44-2	F9
2C44-3	F9
2C44-4	F9
3C00	C2
3C01	C2
3C02	D3
3C03	H2
3C04	H9
3C05-1	G6
3C05-2	G6
3C05-3	H5
3C05-4	H5
3C06-1	G5
3C06-2	H5
3C06-3	H2
3C06-4	I2
3C07-1	G6
3C07-2	G5
3C07-3	G5
3C07-4	H6
3C08-1	H5
3C08-2	H5
3C08-3	H6
3C09-1	H6
3C09-2	H5
3C09-3	H5
3C09-4	H6
3C10	C4
3C11	H6
3C12	I2
3C13	I2
3C20	B10
3C21	B10
3C22	B12
3C23	B12
3C25-1	G12
3C25-2	G12
3C25-3	H11
3C25-4	H12
3C26-1	G12
3C26-2	G11
3C26-3	G11
3C26-4	H12
3C27-1	G11
3C27-2	H11
3C27-3	H9
3C27-4	I8
3C28-1	H12
3C28-2	H11
3C28-3	H11
3C28-4	H12
3C30-1	H11
3C30-2	H11
3C30-3	I8
3C30-4	I9
3C31	H12
3C32	H12
7C00-8	A6
7C01	F3
7C02	F9
FC05	B11
FC06	B9
IC02	C2

SSB: PNX5100: Video


B05B
PNX5100: VIDEO
B05B
1
2
3
4
5
6
7
8
A
B
C
D
E
7C00-5
PNX5100E
Φ
LVDS_RX
AE17
AF17
AC17
AD17
AC16
AD16
AE16
AF16
AE15
AF15
AC15
AD15
AE20
AF20
AC20
AD20
AC19
AD19
AE19
AF19
AE18
AF18
AC18
AD18
AP
AN
BP
BN
CLKP
CLKN
CP
CN
DP
DN
EP
EN
LIN1
AP
AN
BP
BN
CLKP
CLKN
CP
CN
DP
DN
EP
EN
LIN2
7C00-9
PNX5100E
Φ
VDI
DV-CLK
DV-FF_DE
+3V3
3C50
1K0
3C51
1K0
IC54
D6
A4
E2
G4
1
2
3
4
CLK
G3
G2
G1
F4
F3
F2
F1
E3
E1
D2
D1
C1
A2
A3
B3
B4
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
D
DV-B4_UV0
DV-B5_UV1
DV-G0_UV2
DV-G1_UV3
DV-G2_UV4
DV-G3_UV5
D
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
C4
A5
B5
C5
D5
A6
B6
C6
A7
B7
C7
D7
A8
B8
C8
D8
DV-G4_UV6
DV-G5_UV7
DV-G6_UV8
DV-G7_UV9
DV-B6_Y0
DV-B7_Y1
DV-R0_Y2
DV-R1_Y3
DV-R2_Y4
DV-R3_Y5
DV-R4_Y6
DV-R5_Y7
DV-R6_Y8
DV-R7_Y9
DV-VS
DV-HS
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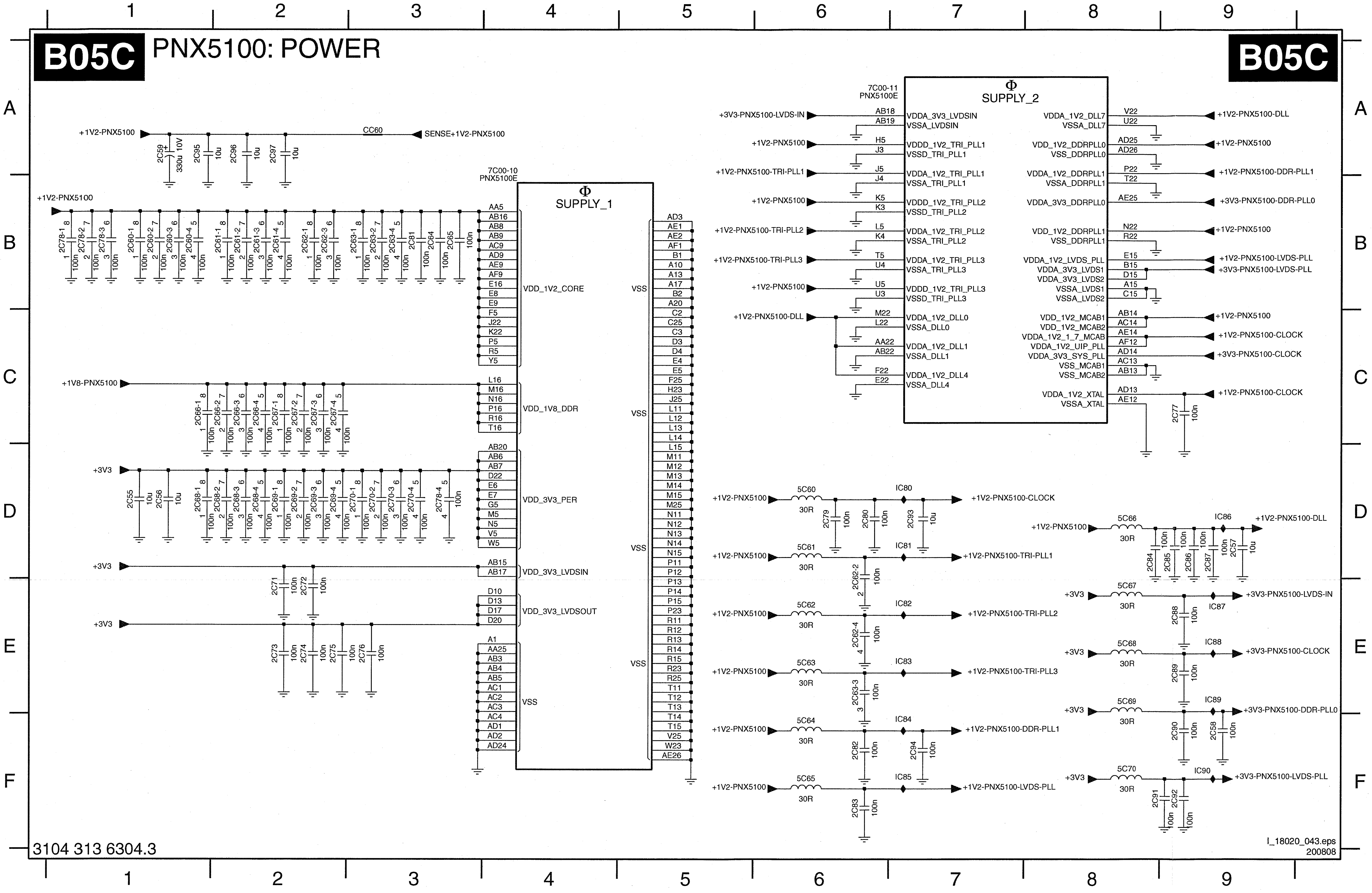
200808

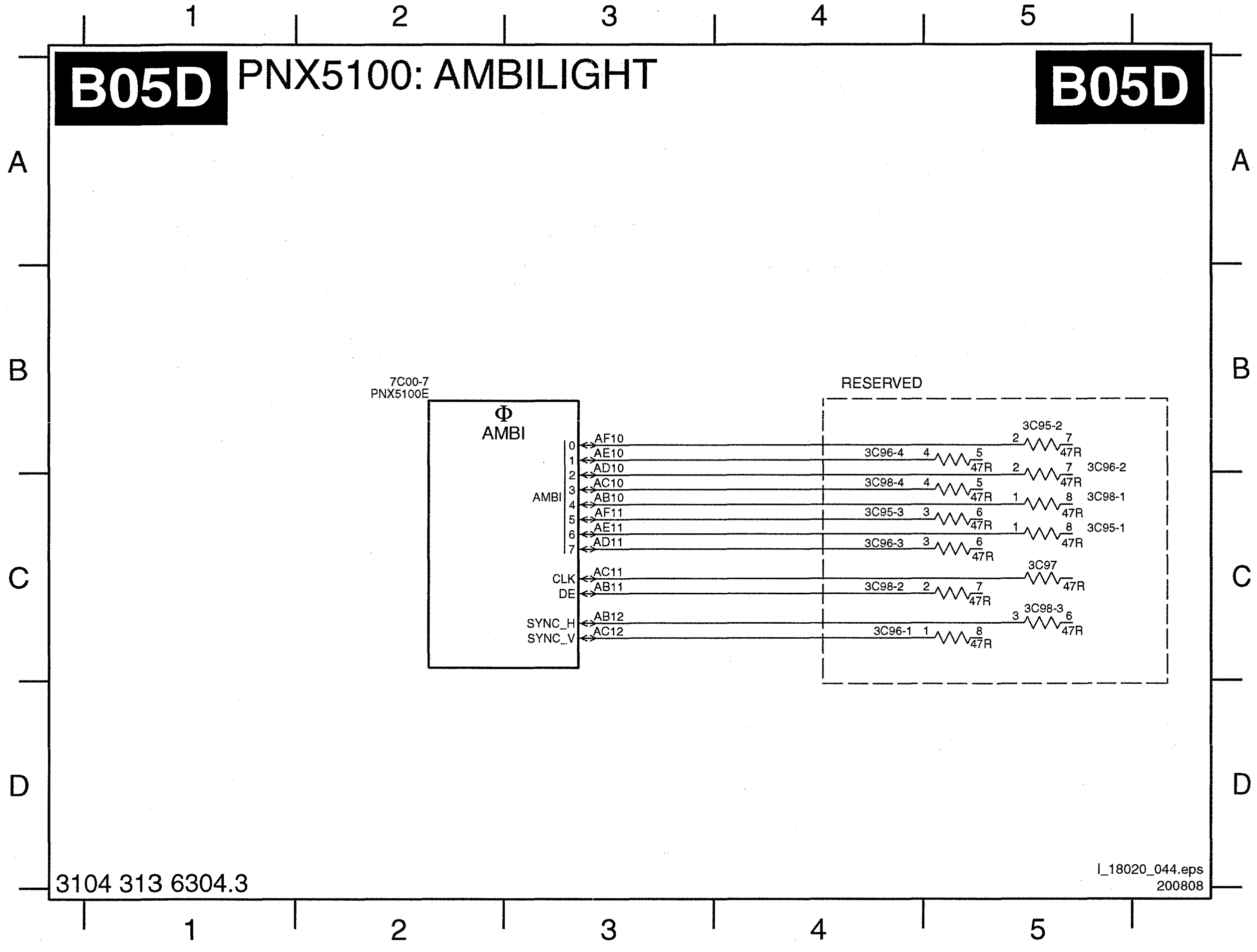
3C50 B5
3C51 B5
7C00-5 B2
7C00-9 B6
IC54 B5

SSB: PNX5100: Power


B05C
PNX5100: POWER
B05C
1 2 3 4 5 6 7 8 9
A B C D E F
7C00-10
PNX5100E
SUPPLY_1
VDD_1V2_CORE
VDD_1V8_DDR
VDD_3V3_PER
VDD_3V3_LVDSIN
VDD_3V3_LVDSOUT
VSS
7C00-11
PNX5100E
SUPPLY_2
+1V2-PNX5100
SENSE+1V2-PNX5100
CC60
+1V8-PNX5100
+3V3
+3V3-PNX5100-LVDS-IN
+1V2-PNX5100-TRI-PLL1
+1V2-PNX5100-TRI-PLL2
+1V2-PNX5100-TRI-PLL3
+1V2-PNX5100-DLL
+1V2-PNX5100-DDR-PLL1
+3V3-PNX5100-DDR-PLL0
+1V2-PNX5100-LVDS-PLL
+3V3-PNX5100-LVDS-PLL
+1V2-PNX5100-CLOCK
+3V3-PNX5100-CLOCK
VDDA_3V3_LVDSIN
VSSA_LVDSIN
VDDD_1V2_TRI_PLL1
VSSD_TRI_PLL1
VDDA_1V2_TRI_PLL1
VSSA_TRI_PLL1
VDDD_1V2_TRI_PLL2
VSSD_TRI_PLL2
VDDA_1V2_TRI_PLL2
VSSA_TRI_PLL2
VDDA_1V2_TRI_PLL3
VSSA_TRI_PLL3
VDDD_1V2_TRI_PLL3
VSSD_TRI_PLL3
VDDA_1V2_DLL0
VSSA_DLL0
VDDA_1V2_DLL1
VSSA_DLL1
VDDA_1V2_DLL4
VSSA_DLL4
VDDA_1V2_DLL7
VSSA_DLL7
VDD_1V2_DDRPLL0
VSS_DDRPLL0
VDDA_1V2_DDRPLL1
VSSA_DDRPLL1
VDDA_3V3_DDRPLL0
VDD_1V2_DDRPLL1
VSS_DDRPLL1
VDDA_1V2_LVDS_PLL
VDDA_3V3_LVDS1
VDDA_3V3_LVDS2
VSSA_LVDS1
VSSA_LVDS2
VDD_1V2_MCAB1
VDD_1V2_MCAB2
VDDA_1V2_1_7_MCAB
VDDA_1V2_UIP_PLL
VDDA_3V3_SYS_PLL
VSS_MCAB1
VSS_MCAB2
VDDA_1V2_XTAL
VSSA_XTAL
5C60 5C61 5C62 5C63 5C64 5C65 5C66 5C67 5C68 5C69 5C70
30R
IC80 IC81 IC82 IC83 IC84 IC85 IC86 IC87 IC88 IC89 IC90
2C59 330u 10V
2C95 10u
2C96 10u
2C97 10u
2C55 10u
2C56 10u
100n
3104 313 6304.3
I_18020_043.eps
200808

2C55	D1
2C56	D1
2C57	D9
2C58	F9
2C59	A1
2C60-1	B1
2C60-2	B1
2C60-3	B1
2C60-4	B1
2C61-1	B2
2C61-2	B2
2C61-3	B2
2C61-4	B2
2C62-1	B2
2C62-2	D6
2C62-3	B2
2C62-4	E6
2C63-1	B3
2C63-2	B3
2C63-3	E6
2C63-4	B3
2C64	B3
2C65	B3
2C66-1	C1
2C66-2	C2
2C66-3	C2
2C66-4	C2
2C67-1	C2
2C67-2	C2
2C67-3	C2
2C67-4	C2
2C68-1	D1
2C68-2	D2
2C68-3	D2
2C68-4	D2
2C69-1	D2
2C69-2	D2
2C69-3	D2
2C69-4	D2
2C70-1	D3
2C70-2	D3
2C70-3	D3
2C70-4	D3
2C71	E2
2C72	E2
2C73	E2
2C74	E2
2C75	E2
2C76	E3
2C77	C9
2C78-1	B1
2C78-2	B1
2C78-3	B1
2C78-4	D3
2C79	D6
2C80	D6
2C81	B3
2C82	F6
2C83	F6
2C84	D8
2C85	D9
2C86	D9
2C87	D9
2C88	E9
2C89	E9
2C90	F9
2C91	F8
2C92	F9
2C93	D7
2C94	F7
2C95	A1
2C96	A2
2C97	A2
5C60	D6
5C61	D6
5C62	E6
5C63	E6
5C64	F6
5C65	F6
5C66	D8
5C67	E8
5C68	E8
5C69	E8
5C70	F8
7C00-10	A4
7C00-11	A7
CC60	A3
IC80	D7
IC81	D7
IC82	E7
IC83	E7
IC84	F7
IC85	F7
IC86	D9
IC87	E9
IC88	E9
IC89	E9
IC90	F9

SSB: PNX5100: AmbiLight

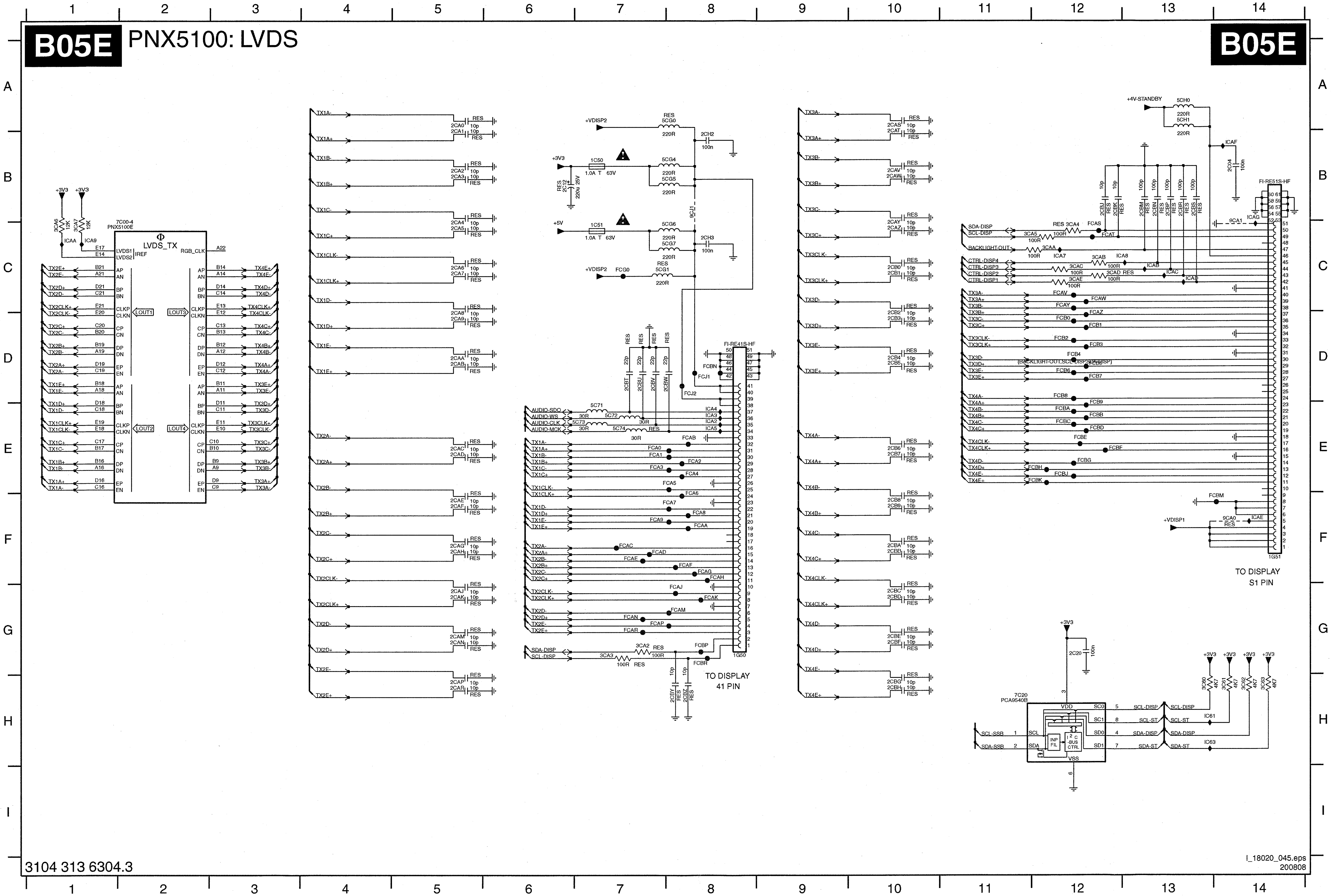

1
2
3
4
5
A
B
C
D
B05D
PNX5100: AMBILIGHT
B05D
7C00-7
PNX5100E
Φ
AMBI
AMBI
0
1
2
3
4
5
6
7
CLK
DE
SYNC_H
SYNC_V
AF10
AE10
AD10
AC10
AB10
AF11
AE11
AD11
AC11
AB11
AB12
AC12
RESERVED
3C95-2
2
7
47R
3C96-4
4
5
47R
2
7
47R
3C96-2
3C98-4
4
5
47R
1
8
47R
3C98-1
3C95-3
3
6
47R
1
8
47R
3C95-1
3C96-3
3
6
47R
3C97
47R
3C98-2
2
7
47R
3C98-3
3
6
47R
3C96-1
1
8
47R
3104 313 6304.3
I_18020_044.eps
200808

3C95-1	B5
3C95-2	B4
3C95-3	B5
3C95-4	B4
3C96-1	B5
3C96-2	B4
3C96-3	B5
3C96-4	B4
3C97	B5
3C98-2	C4
3C98-3	C5
3C98-4	C4
7C00-7	B3

Personal Notes:

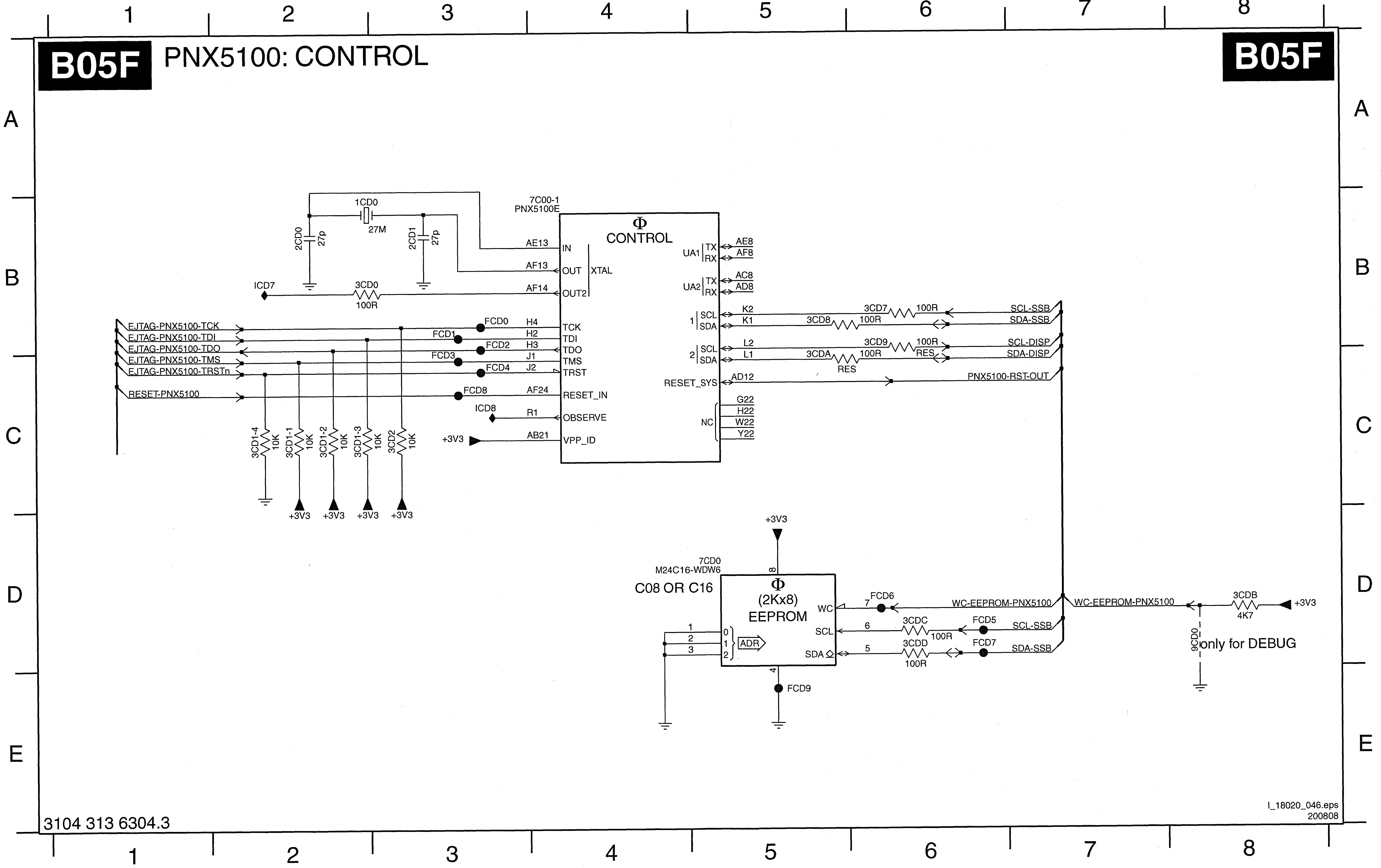
E_06532_012.eps
131004

SSB: PNX5100: LVDS


B05E
PNX5100: LVDS
B05E
7C00-4
PNX5100E
LVDS_TX
LOUT1
LOUT2
LOUT3
LOUT4
FI-RE41S-HF
1G50
TO DISPLAY
41 PIN
FI-RE51S-HF
1G51
TO DISPLAY
S1 PIN
7C20
PCA9540B
+VDISP2
+3V3
+5V
+4V-STANDBY
+VDISP1
AUDIO-SDO
AUDIO-WS
AUDIO-CLK
AUDIO-MCK
SDA-DISP
SCL-DISP
BACKLIGHT-OUT
CTRL-DISP4
CTRL-DISP3
CTRL-DISP2
CTRL-DISP1
SCL-SSB
SDA-SSB
SCL-ST
SDA-ST
3104 313 6304.3
I_18020_045.eps
200808

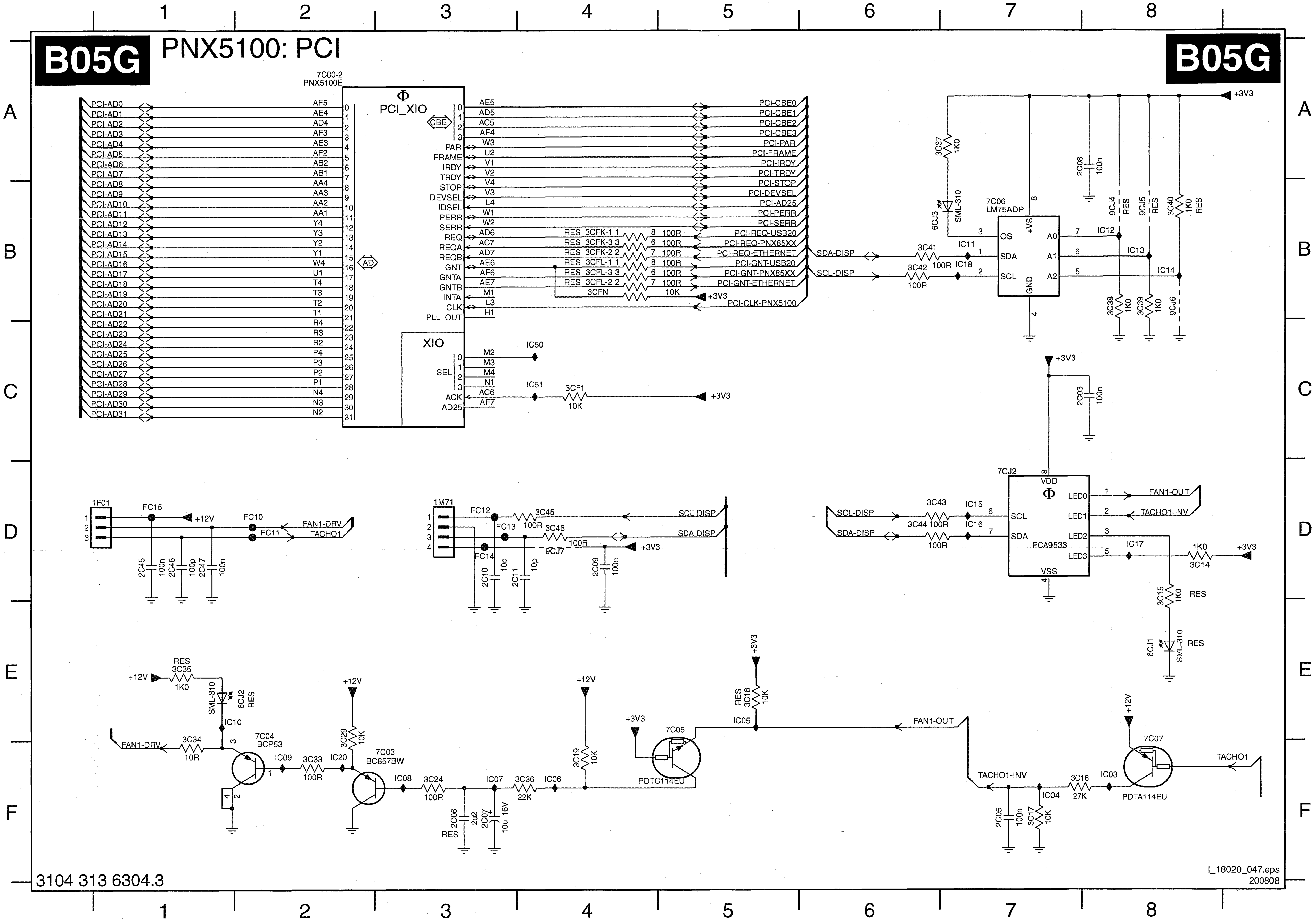
1C50	B7
1C51	C7
1CAA	H9
1G50	G8
1G51	F14
2C04	B14
2C12	B7
2C20	G12
2CA0	A5
2CA1	B5
2CA2	B5
2CA3	B5
2CA4	C5
2CA5	C5
2CA6	C5
2CA7	C5
2CA8	D5
2CA9	D5
2CAA	D5
2CAB	D5
2CAC	E5
2CAD	E5
2CAE	F5
2CAF	F5
2CAG	F5
2CAH	F5
2CAJ	G5
2CAK	G5
2CAM	G5
2CAN	G5
2CAP	H5
2CAR	H5
2CAS	A10
2CAT	B10
2CAV	B10
2CAW	B10
2CAY	C10
2CAZ	C10
2CB0	C10
2CB1	C10
2CB2	D10
2CB3	D10
2CB4	D10
2CB5	D10
2CB6	E10
2CB7	E10
2CB8	F10
2CB9	F10
2CBA	F10
2CBB	F10
2CBC	G10
2CBD	G10
2CBE	G10
2CBF	G10
2CBG	H10
2CBH	H10
2CBJ	B12
2CBK	B12
2CBM	B13
2CBN	B13
2CBP	B13
2CBR	B13
2CBS	B13
2CBT	D7
2CBU	D7
2CBV	D7
2CBW	D8
2CBY	H8
2CBZ	H8
2CH2	B8
2CH3	C8
3C60	H13
3C61	H14
3C62	H14
3C63	H14
3CA2	G7
3CA3	G7
3CA4	C12
3CA5	C11
3CA6	C1
3CA7	C1
3CAA	C12
3CAB	C12
3CAC	C12
3CAD	C12
3CAE	C12
5C71	E7
5C72	E7
5C73	E7
5C74	E7
5CG0	A8
5CG1	C7
5CG4	B8
5CG5	B8
5CG6	C8
5CG7	C8
5CH0	A13
5CH1	A13
7C00-4	C2
7C20	H11
9CA0	F14
9CA1	C14
9CJ1	B8
FCA0	E7
FCA1	E7
FCA2	E8
FCA3	E7
FCA4	E8
FCA5	E8
FCA6	F8
FCA7	F8
FCA8	F8
FCA9	F7
FCAA	F8
FCAB	E8
FCAC	F7
FCAD	F7
FCAE	F7
FCAF	F8
FCAG	F8
FCAH	F8
FCAJ	G8
FCAK	G8
FCAM	G8
FCAN	G7
FCAP	G7
FCAR	G7
FCAS	C12
FCAT	C12
FCAV	C12
FCAW	C12
FCAY	C12
FCAZ	D12
FCB0	D12
FCB1	D12
FCB2	D12
FCB3	D12
FCB4	D12
FCB5	D12
FCB6	D12
FCB7	D12
FCB8	D12
FCB9	E12
FCBA	E12
FCBB	E12
FCBC	E12
FCBD	E12
FCBE	E12
FCBF	E12
FCBG	E12
FCBH	E12
FCBJ	E12
FCBK	E12
FCBM	F14
FCBN	D8
FCBP	G8
FCBR	G8
FCG0	C7
FCJ1	D8
FCJ2	D8
IC61	H13
IC63	H13
ICA2	E8
ICA3	E8
ICA4	E8
ICA5	E8
ICA7	C12
ICA8	C12
ICA9	C1
ICAA	C1
ICAB	C13
ICAC	C13
ICAD	C13
ICAE	F14
ICAF	B14
ICAG	B14

SSB: PNX5100: Control


B05F
PNX5100: CONTROL
B05F
7C00-1
PNX5100E
Φ
CONTROL
1CD0
27M
2CD0
27p
2CD1
27p
ICD7
3CD0
100R
AE13
IN
AF13
OUT
XTAL
AF14
OUT2
UA1
TX
RX
AE8
AF8
UA2
TX
RX
AC8
AD8
EJTAG-PNX5100-TCK
EJTAG-PNX5100-TDI
EJTAG-PNX5100-TDO
EJTAG-PNX5100-TMS
EJTAG-PNX5100-TRSTn
RESET-PNX5100
FCD0
FCD1
FCD2
FCD3
FCD4
FCD8
H4
H2
H3
J1
J2
AF24
TCK
TDI
TDO
TMS
TRST
RESET_IN
ICD8
R1
OBSERVE
+3V3
AB21
VPP_ID
3CD1-4
10K
3CD1-1
10K
3CD1-2
10K
3CD1-3
10K
3CD2
10K
+3V3
+3V3
+3V3
+3V3
1
SCL
SDA
K2
K1
3CD7
100R
3CD8
100R
SCL-SSB
SDA-SSB
2
SCL
SDA
L2
L1
3CD9
100R
RES
3CDA
100R
RES
SCL-DISP
SDA-DISP
RESET_SYS
AD12
PNX5100-RST-OUT
NC
G22
H22
W22
Y22
+3V3
7CD0
M24C16-WDW6
C08 OR C16
8
Φ
(2Kx8)
EEPROM
WC
SCL
SDA
ADR
0
1
2
1
2
3
4
FCD9
7
FCD6
WC-EEPROM-PNX5100
6
3CDC
100R
FCD5
SCL-SSB
5
3CDD
100R
FCD7
SDA-SSB
WC-EEPROM-PNX5100
3CDB
4K7
+3V3
9CD0
only for DEBUG
3104 313 6304.3
I_18020_046.eps
200808
1
2
3
4
5
6
7
8
A
B
C
D
E

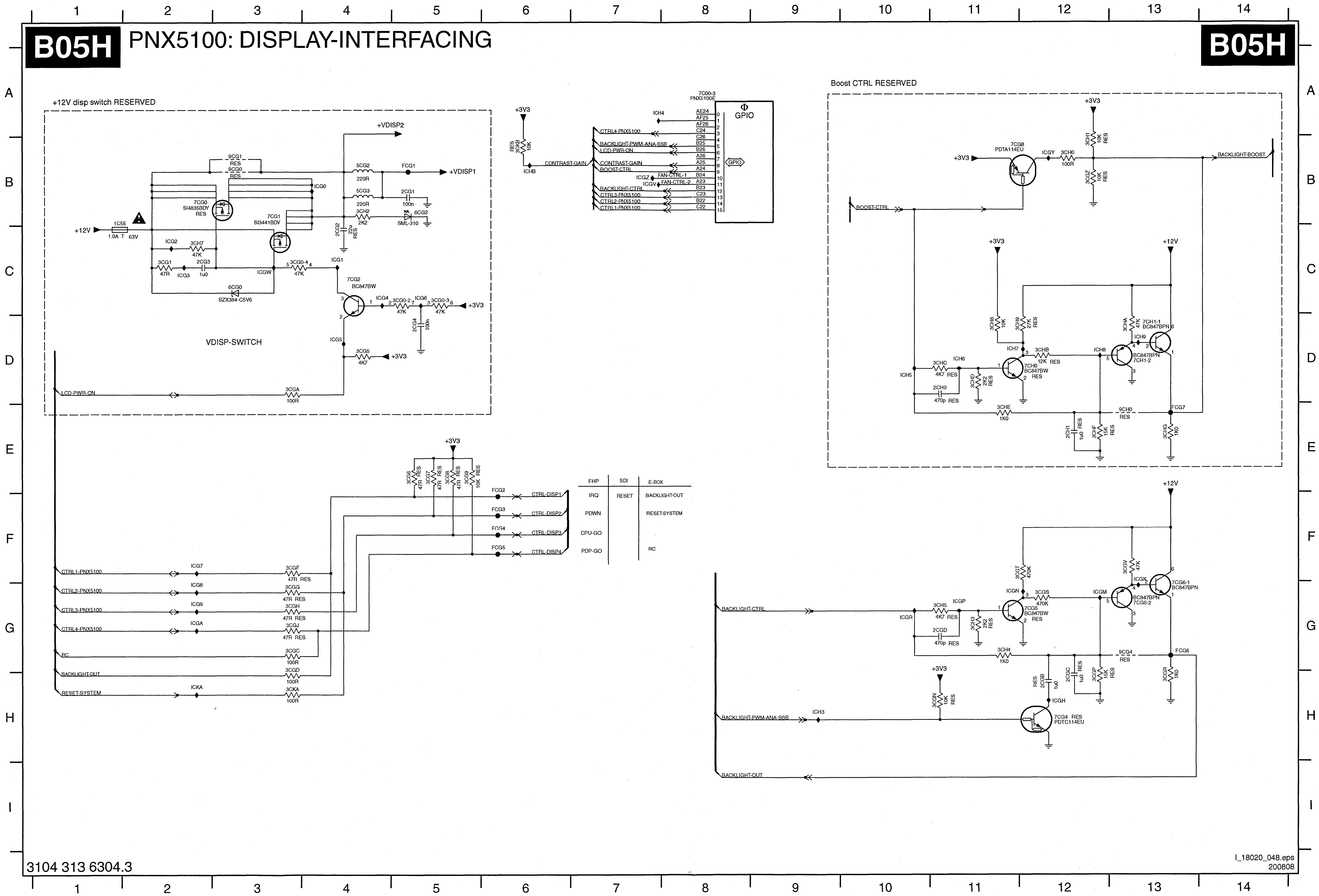
1CD0	B2
2CD0	B2
2CD1	B3
3CD0	B2
3CD1-1	C2
3CD1-2	C2
3CD1-3	C2
3CD1-4	C2
3CD2	C3
3CD7	B6
3CD8	B5
3CD9	B6
3CDA	C5
3CDB	D8
3CDC	D6
3CDD	D6
7C00-1	B4
7CD0	D5
9CD0	D8
FCD0	B3
FCD1	B3
FCD2	B3
FCD3	C3
FCD4	C3
FCD5	D6
FCD6	D6
FCD7	D6
FCD8	C3
FCD9	E5
ICD7	B2
ICD8	C3

SSB: PNX5100: PCI


B05G
PNX5100: PCI
B05G
7C00-2
PNX5100E
PCI_XIO
XIO
CBE
AD
SEL
PAR
FRAME
IRDY
TRDY
STOP
DEVSEL
IDSEL
PERR
SERR
REQ
REQA
REQB
GNT
GNTA
GNTB
INTA
CLK
PLL_OUT
ACK
AD25
PCI-AD0 … PCI-AD31
PCI-CBE0
PCI-CBE1
PCI-CBE2
PCI-CBE3
PCI-PAR
PCI-FRAME
PCI-IRDY
PCI-TRDY
PCI-STOP
PCI-DEVSEL
PCI-AD25
PCI-PERR
PCI-SERR
PCI-REQ-USB20
PCI-REQ-PNX85XX
PCI-REQ-ETHERNET
PCI-GNT-USB20
PCI-GNT-PNX85XX
PCI-GNT-ETHERNET
PCI-CLK-PNX5100
SDA-DISP
SCL-DISP
7C06
LM75ADP
OS
SDA
SCL
GND
+VS
A0
A1
A2
7CJ2
PCA9533
VDD
VSS
LED0
LED1
LED2
LED3
FAN1-OUT
TACHO1-INV
FAN1-DRV
TACHO1
1F01
1M71
7C04
BCP53
7C03
BC857BW
7C05
PDTC114EU
7C07
PDTA114EU
+3V3
+12V
RES
SML-310
3104 313 6304.3
I_18020_047.eps
200808

1F01	D1
1M71	D3
2C03	C8
2C05	F7
2C06	F3
2C07	F3
2C08	A8
2C09	D4
2C10	D3
2C11	D4
2C45	D1
2C46	D1
2C47	D1
3C14	D8
3C15	D8
3C16	F7
3C17	F7
3C18	E5
3C19	F4
3C24	F3
3C29	E2
3C33	F2
3C34	F1
3C35	E1
3C36	F4
3C37	A7
3C38	B8
3C39	B8
3C40	B8
3C41	B6
3C42	B6
3C43	D6
3C44	D6
3C45	D4
3C46	D4
3CF1	C4
3CFK-1	B4
3CFK-2	B4
3CFK-3	B4
3CFL-1	B4
3CFL-2	B4
3CFL-3	B4
3CFN	B4
6CJ1	E8
6CJ2	E2
6CJ3	B6
7C00-2	A2
7C03	F3
7C04	E2
7C05	E5
7C06	B7
7C07	E8
7CJ2	D7
9CJ4	B8
9CJ5	B8
9CJ6	B8
9CJ7	D4
FC10	D2
FC11	D2
FC12	D3
FC13	D3
FC14	D3
FC15	D1
IC03	F8
IC04	F7
IC05	E5
IC06	F4
IC07	F3
IC08	F3
IC09	F2
IC10	E1
IC11	B7
IC12	B8
IC13	B8
IC14	B8
IC15	D7
IC16	D7
IC17	D8
IC18	B7
IC20	F2
IC50	C4
IC51	C4

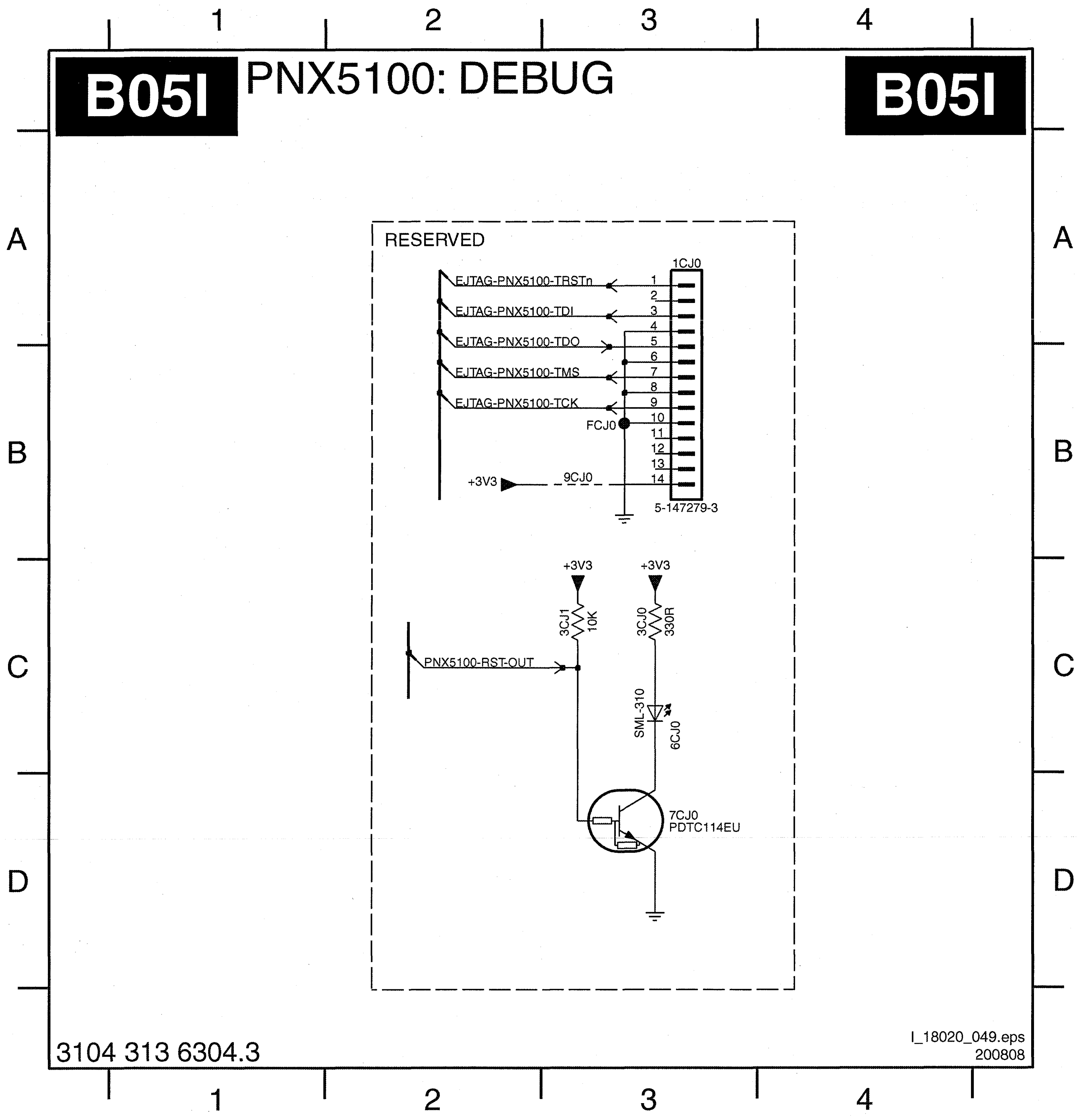
SSB: PNX5100: Display Interfacing


B05H
PNX5100: DISPLAY-INTERFACING
B05H
+12V disp switch RESERVED
+VDISP2
+VDISP1
+12V
1C55
1.0A T 63V
9CG1 RES
9CG0 RES
5CG2 220R
5CG3 220R
FCG1
2CG1 100n
3CH2 2K2
6CG2 SML-310
2CG2 22u RES
7CG0 SI4835BDY RES
7CG1 SI3441BDV
ICG0
ICG2
3CH7 47K
3CG1 47R
ICG3
2CG3 1u0
ICGW
3CG0-4 47K
ICG1
7CG2 BC847BW
6CG0 BZX384-C5V6
ICG4
3CG0-2 47K
ICG6
3CG0-3 47K
+3V3
2CG4 100n
ICG5
3CG5 4K7
VDISP-SWITCH
LCD-PWR-ON
3CGA 100R
+3V3
3CKB 10K RES
ICHB
CONTRAST-GAIN
ICH4
7C00-3 PNX5100E
GPIO
AE24 AF25 AF26 C24 C26 B25 B26 A26 A25 A24 B24 A23 B23 C23 B22 C22
CTRL4-PNX5100
BACKLIGHT-PWM-ANA-SSB
LCD-PWR-ON
CONTRAST-GAIN
BOOST-CTRL
ICGZ FAN-CTRL-1
ICGV FAN-CTRL-2
BACKLIGHT-CTRL
CTRL3-PNX5100
CTRL2-PNX5100
CTRL1-PNX5100
+3V3
3CG6 47R RES
3CG7 47R RES
3CG8 47R RES
3CG9 10K RES
FCG2 CTRL-DISP1
FCG3 CTRL-DISP2
FCG4 CTRL-DISP3
FCG5 CTRL-DISP4
FHP | SDI | E-BOX
IRQ | RESET | BACKLIGHT-OUT
PDWN | | RESET-SYSTEM
CPU-GO
PDP-GO | | RC
CTRL1-PNX5100 ICG7 3CGF 47R RES
CTRL2-PNX5100 ICG8 3CGG 47R RES
CTRL3-PNX5100 ICG9 3CGH 47R RES
CTRL4-PNX5100 ICGA 3CGJ 47R RES
RC 3CGC 100R
BACKLIGHT-OUT 3CGD 100R
RESET-SYSTEM ICKA 3CKA 100R
Boost CTRL RESERVED
+3V3
3CH1 10K RES
7CG8 PDTA114EU
ICGY 3CH0 100R
3CGZ 10K RES
BACKLIGHT-BOOST
BOOST-CTRL
+3V3
+12V
3CH8 10K
3CH9 27K RES
3CHA 47K
7CH1-1 BC847BPN
ICH9
ICH7 3CHB 12K RES
ICH8
7CH1-2 BC847BPN
7CH0 BC847BW RES
ICH6
3CHC 4K7 RES
ICH5
3CHD 2K2 RES
2CH0 470p RES
3CHE 1K0
2CH1 1u0 RES
3CHF 15K RES
9CH0 RES
FCG7
3CHG 1K0
+12V
3CGT 470K
3CGV 47K
ICGK
7CG6-1 BC847BPN
ICGN 3CGS 470K
ICGM
7CG6-2 BC847BPN
7CG5 BC847BW RES
3CH5 4K7 RES
ICGP
ICGR
3CH3 2K2 RES
2CGD 470p RES
3CH4 1K0
9CG4 RES
FCG6
BACKLIGHT-CTRL
+3V3
3CGN 10K RES
2CGB 1u0 RES
2CGC 1u0 RES
3CGP 15K RES
3CGR 1K0
ICGH
7CG4 RES PDTC114EU
BACKLIGHT-PWM-ANA-SSB
ICH3
BACKLIGHT-OUT
3104 313 6304.3
I_18020_048.eps
200808
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A B C D E F G H I

1C55	B1
2CG1	B5
2CG2	C4
2CG3	C2
2CG4	D5
2CGB	H12
2CGC	H12
2CGD	G11
2CH0	D11
2CH1	E12
3CG0-2	C5
3CG0-3	C5
3CG0-4	C3
3CG1	C2
3CG5	D4
3CG6	E5
3CG7	E5
3CG8	E5
3CG9	E5
3CGA	D3
3CGC	G3
3CGD	G3
3CGF	F3
3CGG	G3
3CGH	G3
3CGJ	G3
3CGN	H11
3CGP	H12
3CGR	H13
3CGS	G12
3CGT	F11
3CGV	F13
3CGZ	B12
3CH0	B12
3CH1	B12
3CH2	B4
3CH3	G11
3CH4	G11
3CH5	G11
3CH7	C2
3CH8	D11
3CH9	D11
3CHA	D13
3CHB	D12
3CHC	D11
3CHD	D11
3CHE	E11
3CHF	E12
3CHG	E13
3CKA	H3
3CKB	B6
5CG2	B4
5CG3	B4
6CG0	C3
6CG2	B5
7C00-3	A8
7CG0	B2
7CG1	B3
7CG2	C4
7CG4	H12
7CG5	G12
7CG6-1	G13
7CG6-2	G13
7CG8	B12
7CH0	D12
7CH1-1	D13
7CH1-2	D13
9CG0	B3
9CG1	B3
9CG4	G13
9CH0	E13
FCG1	B5
FCG2	E6
FCG3	F6
FCG4	F6
FCG5	F6
FCG6	G13
FCG7	E13
ICG0	B4
ICG1	C4
ICG2	C2
ICG3	C2
ICG4	C4
ICG5	D4
ICG6	C5
ICG7	F2
ICG8	G2
ICG9	G2
ICGA	G2
ICGH	H12
ICGK	F13
ICGM	G12
ICGN	G11
ICGP	G11
ICGR	G10
ICGV	B7
ICGW	C3
ICGY	B12
ICGZ	B7
ICH3	H9
ICH4	A7
ICH5	D10
ICH6	D11
ICH7	D11
ICH8	D12
ICH9	D13
ICHB	B6
ICKA	H2

SSB: PNX5100: Debug

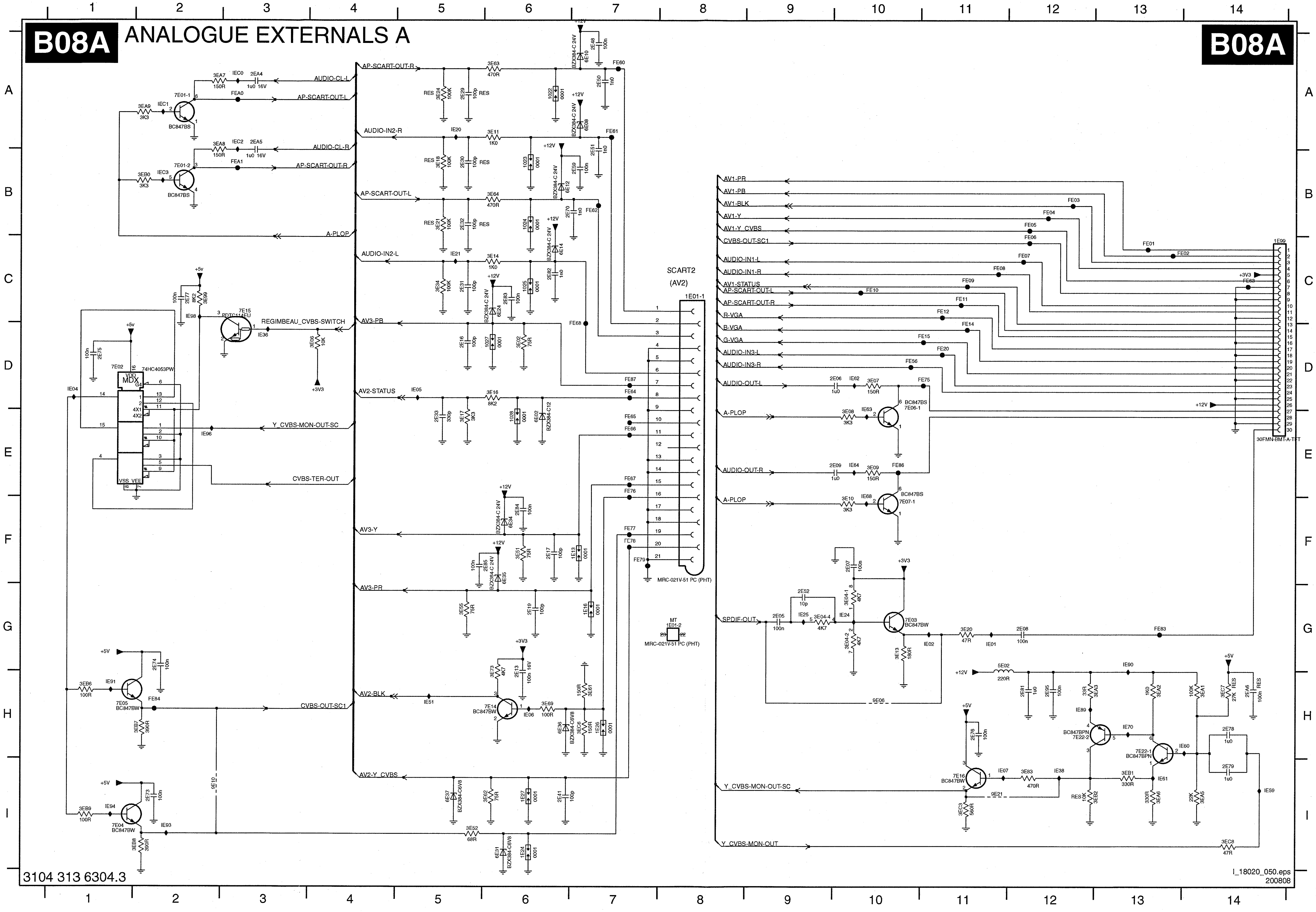
1CJ0 A3 3CJ0 C3 3CJ1 C3 6CJ0 C3 7CJ0 D3 9CJ0 B3 FCJ0 B3


1
2
3
4
A
B
C
D
B05I
PNX5100: DEBUG
B05I
RESERVED
1CJ0
EJTAG-PNX5100-TRSTn
EJTAG-PNX5100-TDI
EJTAG-PNX5100-TDO
EJTAG-PNX5100-TMS
EJTAG-PNX5100-TCK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
FCJ0
+3V3
9CJ0
5-147279-3
+3V3
+3V3
3CJ1
10K
3CJ0
330R
PNX5100-RST-OUT
SML-310
6CJ0
7CJ0
PDTC114EU
3104 313 6304.3
I_18020_049.eps
200808

Personal Notes:

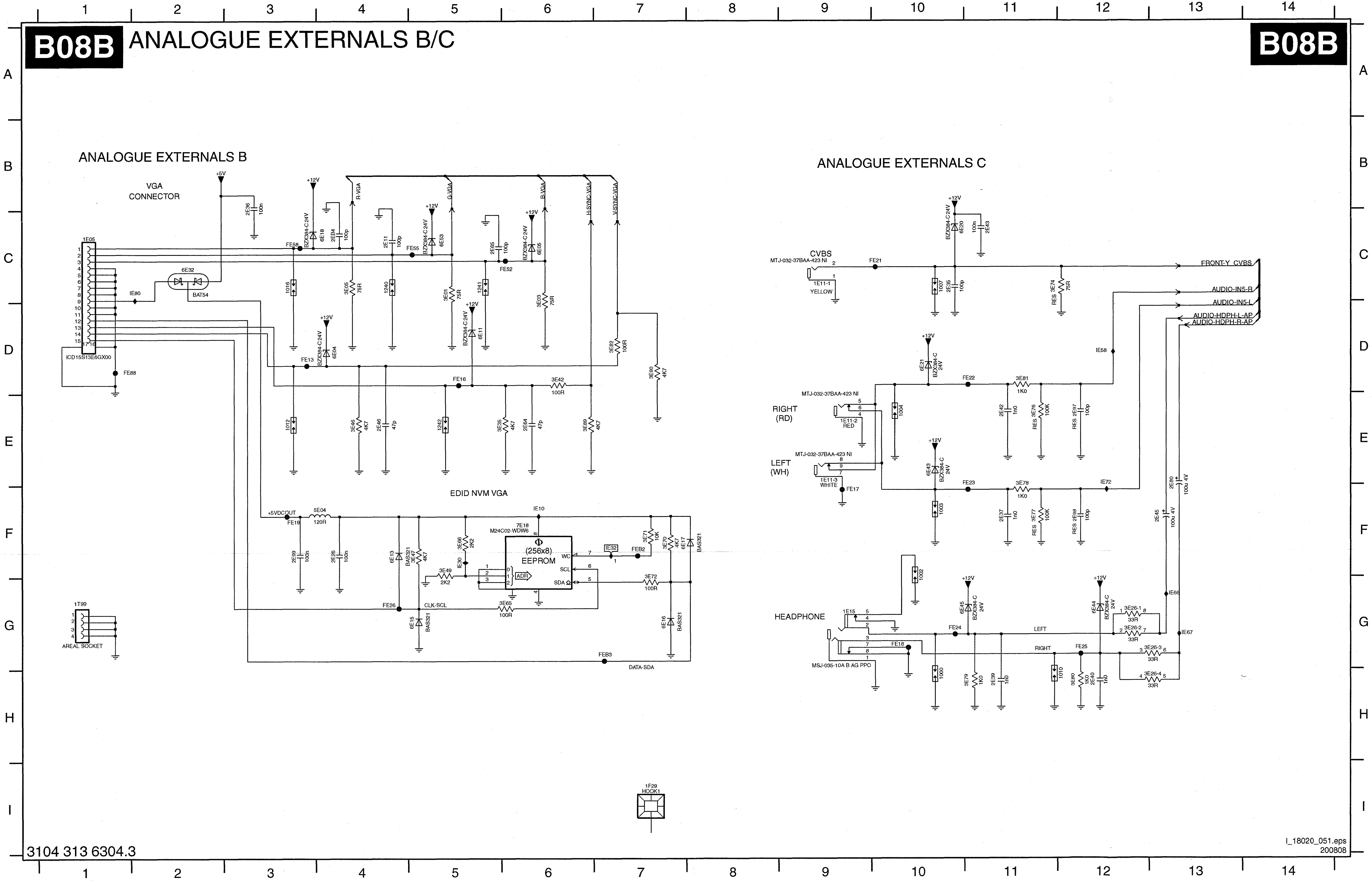
E_06532_012.eps
131004

SSB: Analogue Externals A


B08A
ANALOGUE EXTERNALS A
B08A
AUDIO-CL-L
AP-SCART-OUT-L
AUDIO-CL-R
AP-SCART-OUT-R
A-PLOP
AP-SCART-OUT-R
AUDIO-IN2-R
AP-SCART-OUT-L
AUDIO-IN2-L
AV3-PB
AV2-STATUS
Y_CVBS-MON-OUT-SC
CVBS-TER-OUT
AV3-Y
AV3-PR
AV2-BLK
CVBS-OUT-SC1
AV2-Y_CVBS
REGIMBEAU_CVBS-SWITCH
74HC4053PW
MDX
SCART2
(AV2)
1E01-1
MRC-021V-51 PC (PHT)
MT
1E01-2
AV1-PR
AV1-PB
AV1-BLK
AV1-Y
AV1-Y_CVBS
CVBS-OUT-SC1
AUDIO-IN1-L
AUDIO-IN1-R
AV1-STATUS
AP-SCART-OUT-L
AP-SCART-OUT-R
R-VGA
B-VGA
G-VGA
AUDIO-IN3-L
AUDIO-IN3-R
AUDIO-OUT-L
A-PLOP
AUDIO-OUT-R
A-PLOP
SPDIF-OUT
Y_CVBS-MON-OUT-SC
Y_CVBS-MON-OUT
1E99
30FMN-BMT-A-TFT
BC847BS
BC847BW
BC847BPN
PDTC114EU
BZX384-C24V
BZX384-C6V8
+12V
+5V
+3V3
3104 313 6304.3
I_18020_050.eps
200808

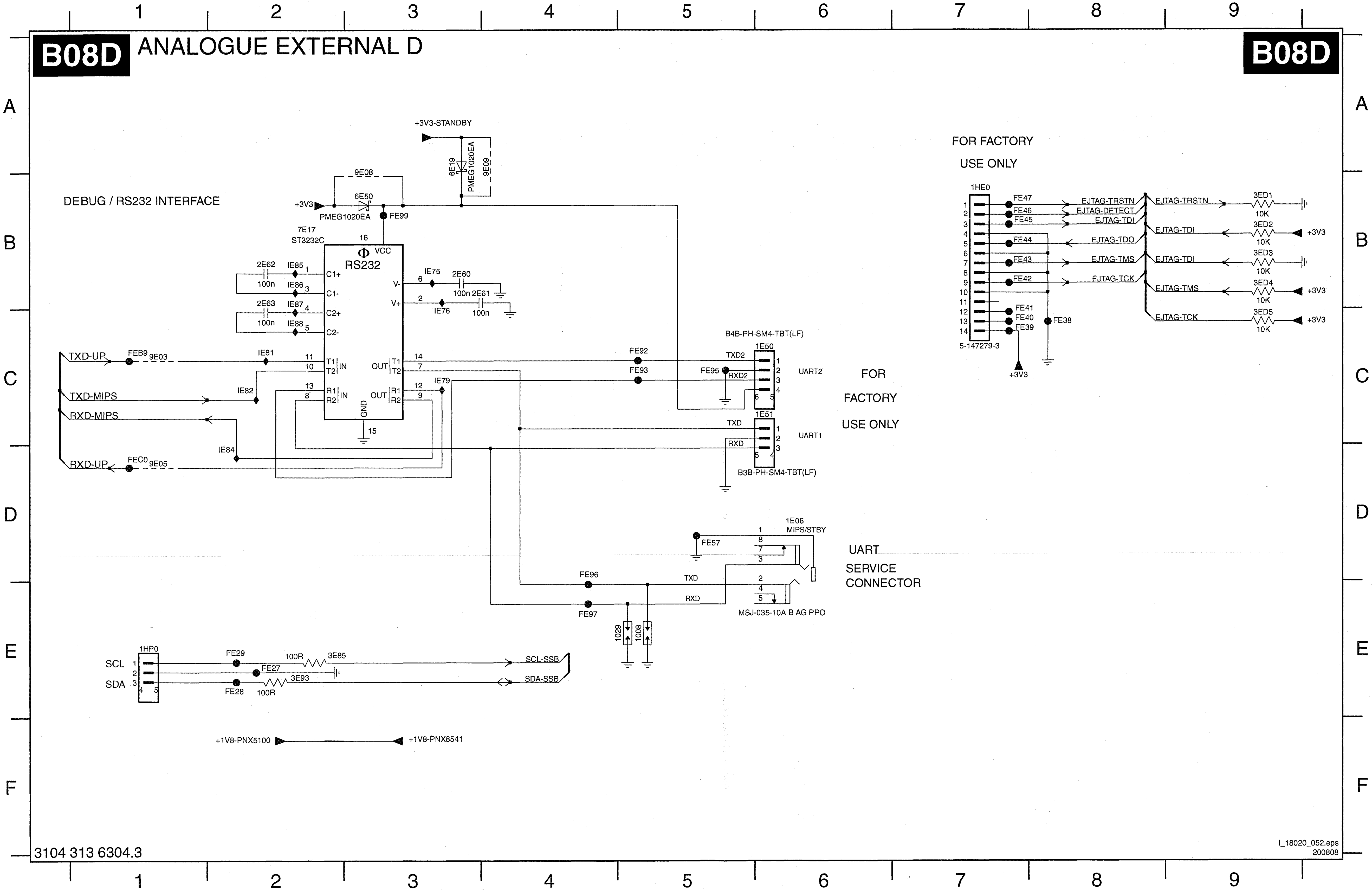
1022	A6
1023	B6
1024	B6
1025	C6
1027	D6
1028	E6
1E01-1	C8
1E01-2	G8
1E13	F7
1E16	G7
1E24	I6
1E26	H7
1E27	I6
1E99	C14
2E05	G9
2E06	D10
2E07	F10
2E08	G12
2E09	E10
2E13	H6
2E16	D5
2E17	F6
2E19	G6
2E29	A5
2E30	B5
2E31	C5
2E32	B5
2E33	E5
2E41	I6
2E48	A7
2E50	A7
2E51	B7
2E52	G9
2E59	B7
2E70	B6
2E73	I2
2E74	G2
2E75	D1
2E76	H11
2E77	C2
2E78	H14
2E79	I14
2E81	H12
2E82	C6
2E83	C6
2E84	F6
2E85	F6
2E95	H12
2EA4	A3
2EA5	A3
2EA6	H14
3E02	D6
3E04-1	G10
3E04-2	G10
3E04-4	G9
3E06	D4
3E07	D10
3E08	E10
3E09	E10
3E10	F10
3E11	A6
3E13	G10
3E14	C6
3E16	D6
3E17	E5
3E18	B5
3E20	G11
3E21	B5
3E24	A5
3E34	C5
3E51	F6
3E52	I5
3E55	G5
3E61	H7
3E62	I6
3E63	A6
3E64	B6
3E69	H6
3E73	H6
3E83	I12
3E99	C2
3EA1	H14
3EA2	H13
3EA3	H12
3EA5	I14
3EA6	I13
3EA7	A2
3EA8	A2
3EA9	A2
3EB0	B2
3EB1	I13
3EB2	I12
3EB6	H1
3EB7	H2
3EB8	I1
3EB9	I1
3EC3	I11
3EC6	H7
3EC7	H14
3EC8	I14
5E02	G11
6E02	E6
6E08	A7
6E10	A7
6E12	B6
6E14	C6
6E24	C6
6E31	I6
6E34	F6
6E35	F6
6E36	H6
6E37	I5
7E01-1	A2
7E01-2	B2
7E02	D1
7E03	G10
7E04	I1
7E05	H1
7E06-1	D10
7E07-1	F10
7E14	H6
7E15	C3
7E16	I11
7E22-1	H13
7E22-2	H12
9E06	H10
9E10	I2
9E21	I11
FE01	C13
FE02	C13
FE03	B12
FE04	B12
FE05	B12
FE06	C12
FE07	C12
FE08	C11
FE09	C11
FE10	C10
FE11	C11
FE12	C11
FE14	D11
FE15	D11
FE20	D11
FE56	D10
FE60	A7
FE61	A7
FE62	B7
FE63	C14
FE64	D7
FE65	E7
FE66	E7
FE67	E7
FE68	D7
FE75	D11
FE76	E7
FE77	F7
FE78	F7
FE79	F7
FE83	G13
FE84	H2
FE86	E10
FE87	D7
FEA0	A3
FEA1	B3
IE01	G11
IE02	G11
IE04	D1
IE05	D5
IE06	H6
IE07	I11
IE20	A5
IE21	C5
IE24	G10
IE25	G9
IE36	D3
IE38	I12
IE51	H5
IE59	I14
IE60	H14
IE61	I13
IE62	D10
IE63	D10
IE64	E10
IE68	E10
IE70	H13
IE89	H12
IE90	G13
IE91	H1
IE93	I2
IE94	I1
IE96	E2
IE98	C2
IEC0	A3
IEC1	A2
IEC2	A3
IEC3	B2

SSB: Analogue Externals B/C


B08B
ANALOGUE EXTERNALS B/C
B08B
ANALOGUE EXTERNALS B
VGA CONNECTOR
1E05
ICD15S13E6GX00
6E32
BAT54
R-VGA
G-VGA
B-VGA
H-SYNC-VGA
V-SYNC-VGA
+5V
+12V
EDID NVM VGA
+5VDCOUT
7E18
M24C02-WDW6
(256x8)
EEPROM
CLK-SCL
DATA-SDA
1T99
AREAL SOCKET
1F29
HOOK1
ANALOGUE EXTERNALS C
CVBS
MTJ-032-37BAA-423 NI
1E11-1
YELLOW
RIGHT
(RD)
1E11-2
RED
LEFT
(WH)
1E11-3
WHITE
HEADPHONE
1E15
MSJ-035-10A B AG PPO
LEFT
RIGHT
FRONT-Y_CVBS
AUDIO-IN5-R
AUDIO-IN5-L
AUDIO-HDPH-L-AP
AUDIO-HDPH-R-AP
3104 313 6304.3
I_18020_051.eps
200808

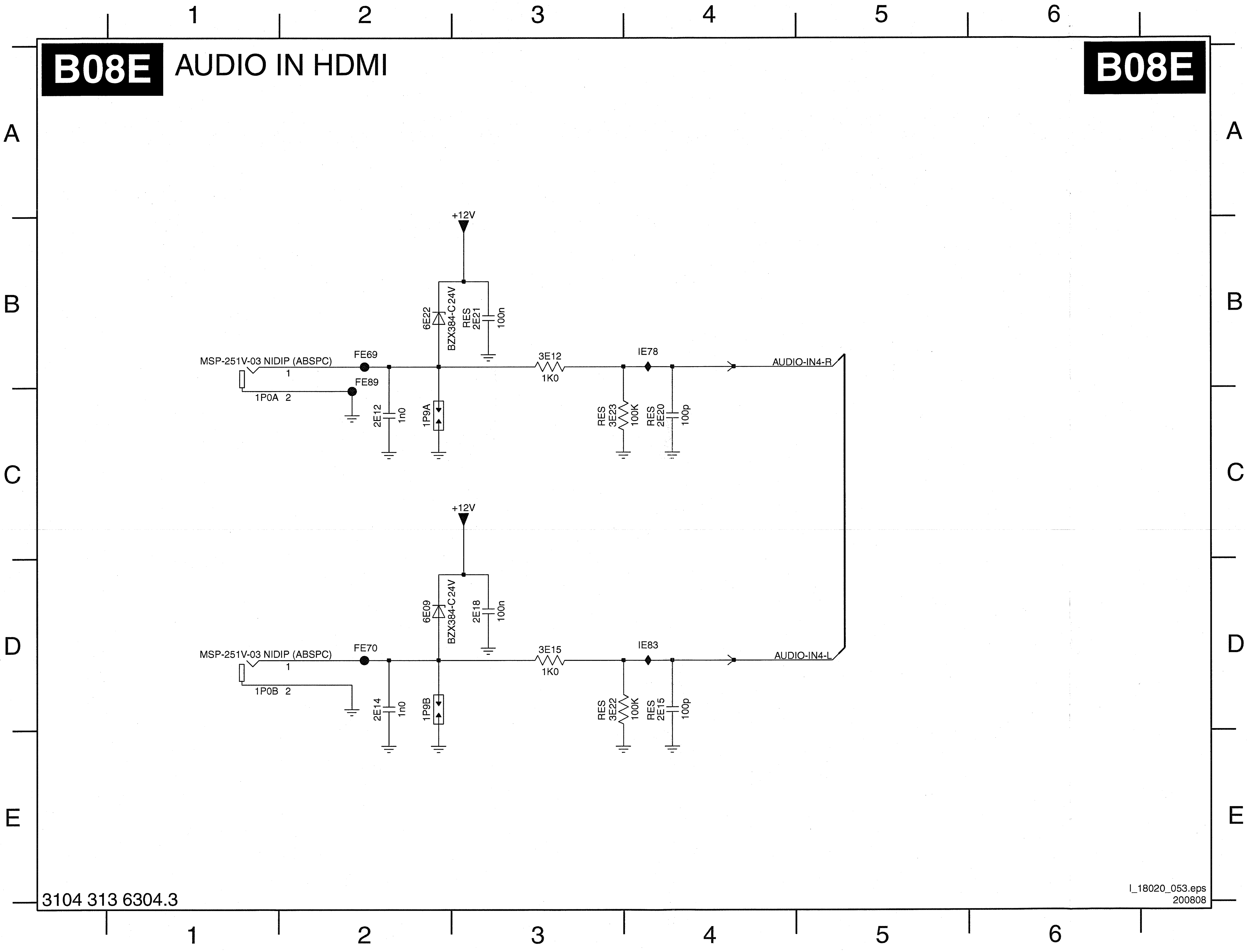
1000	H10
1002	F10
1003	F10
1004	E10
1007	C10
1010	H12
1012	E3
1016	C3
1240	C4
1241	C5
1242	E5
1E05	C1
1E11-1	C9
1E11-2	E9
1E11-3	E9
1E15	G9
1F29	I7
1T99	G1
2E11	C4
2E26	F4
2E35	C10
2E36	B3
2E37	F11
2E39	H11
2E40	H12
2E42	E11
2E43	C11
2E45	F13
2E46	E4
2E64	E6
2E65	C5
2E80	E13
2E97	E12
2E98	F12
2E99	F3
2EB4	C4
3E01	C5
3E03	C6
3E05	C4
3E26-1	G12
3E26-2	G12
3E26-3	G13
3E26-4	H13
3E35	E5
3E42	D6
3E46	E4
3E47	F5
3E49	F5
3E65	G6
3E66	F5
3E70	F7
3E71	F7
3E72	G7
3E74	C11
3E76	E11
3E77	F11
3E78	F11
3E79	H10
3E80	H12
3E81	D11
3E82	D7
3E89	E6
3E90	D7
5E04	F4
6E04	D4
6E05	C6
6E11	D5
6E13	F4
6E15	G5
6E16	G7
6E17	F7
6E18	C4
6E20	C10
6E21	D10
6E32	C2
6E43	E10
6E44	G12
6E45	G10
6E53	C5
7E18	F6
FE13	D3
FE16	D5
FE17	F9
FE18	G10
FE19	F3
FE21	C10
FE22	D11
FE23	E11
FE24	G10
FE25	G12
FE26	G4
FE52	C6
FE55	C5
FE58	C3
FE88	D1
FEB2	F7
FEB3	G7
IE10	F6
IE30	F5
IE32	F7
IE58	D12
IE66	G13
IE67	G13
IE72	E12
IE80	C2

SSB: Analogue Externals D


B08D
ANALOGUE EXTERNAL D
B08D
DEBUG / RS232 INTERFACE
+3V3-STANDBY
6E19
PMEG1020EA
9E09
9E08
6E50
+3V3
PMEG1020EA
FE99
7E17
ST3232C
16
RS232
VCC
2E62
100n
IE85
IE86
2E63
100n
IE87
IE88
C1+
C1-
C2+
C2-
IE75
2E60
100n
2E61
100n
IE76
V-
V+
TXD-UP
FEB9
9E03
IE81
TXD-MIPS
IE82
RXD-MIPS
IE84
RXD-UP
FEC0
9E05
T1
T2
IN
OUT
R1
R2
GND
15
IE79
FE92
FE93
FE95
B4B-PH-SM4-TBT(LF)
1E50
TXD2
RXD2
UART2
TXD
RXD
1E51
UART1
B3B-PH-SM4-TBT(LF)
FOR
FACTORY
USE ONLY
1E06
MIPS/STBY
FE57
UART
SERVICE
CONNECTOR
FE96
FE97
MSJ-035-10A B AG PPO
1029
1008
1HP0
SCL
SDA
FE29
FE27
FE28
100R
3E85
3E93
100R
SCL-SSB
SDA-SSB
+1V8-PNX5100
+1V8-PNX8541
FOR FACTORY
USE ONLY
1HE0
5-147279-3
FE47
FE46
FE45
FE44
FE43
FE42
FE41
FE40
FE39
FE38
+3V3
EJTAG-TRSTN
EJTAG-DETECT
EJTAG-TDI
EJTAG-TDO
EJTAG-TMS
EJTAG-TCK
3ED1
10K
3ED2
10K
3ED3
10K
3ED4
10K
3ED5
10K
+3V3
3104 313 6304.3
I_18020_052.eps
200808

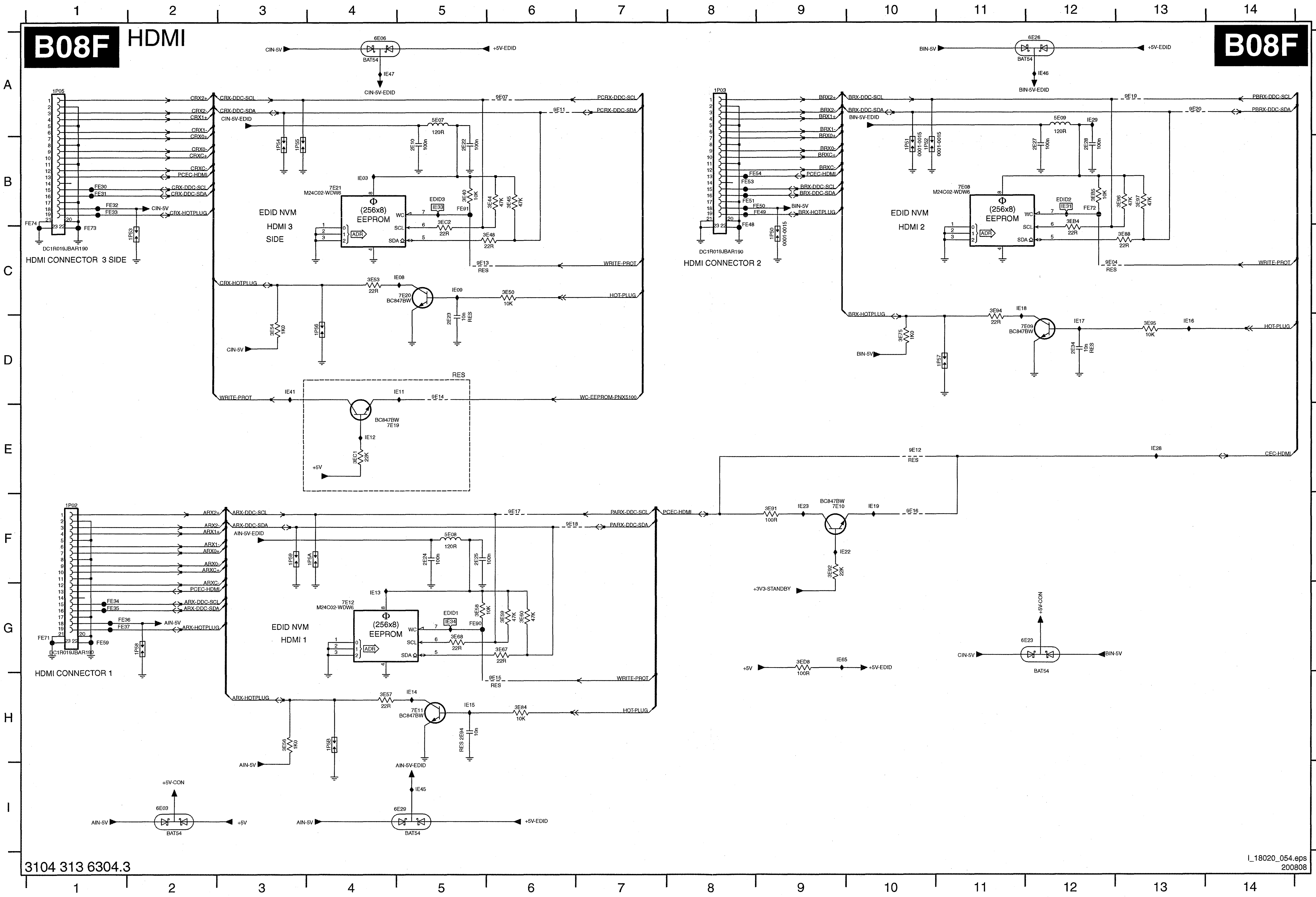
1008	E5
1029	E5
1E06	D6
1E50	C6
1E51	C6
1HE0	B7
1HP0	E1
2E60	B3
2E61	B3
2E62	B2
2E63	B2
3E85	E2
3E93	E2
3ED1	B9
3ED2	B9
3ED3	B9
3ED4	B9
3ED5	C9
6E19	A3
6E50	B3
7E17	B2
9E03	C1
9E05	D1
9E08	B3
9E09	A4
FE27	E2
FE28	E2
FE29	E2
FE38	C8
FE39	C7
FE40	C7
FE41	C7
FE42	B7
FE43	B7
FE44	B7
FE45	B7
FE46	B7
FE47	B7
FE57	D5
FE92	C5
FE93	C5
FE95	C5
FE96	D4
FE97	E4
FE99	B3
FEB9	C1
FEC0	D1
IE75	B3
IE76	C3
IE79	C3
IE81	C2
IE82	C2
IE84	D2
IE85	B2
IE86	B2
IE87	B2
IE88	C2

SSB: Audio in HDMI


B08E
AUDIO IN HDMI
B08E
1
2
3
4
5
6
A
B
C
D
E
+12V
6E22
BZX384-C24V
RES
2E21
100n
MSP-251V-03 NIDIP (ABSPC)
FE69
1
FE89
1P0A 2
2E12
1n0
1P9A
3E12
1K0
IE78
RES
3E23
100K
RES
2E20
100p
AUDIO-IN4-R
+12V
6E09
BZX384-C24V
2E18
100n
MSP-251V-03 NIDIP (ABSPC)
FE70
1
1P0B 2
2E14
1n0
1P9B
3E15
1K0
IE83
RES
3E22
100K
RES
2E15
100p
AUDIO-IN4-L
3104 313 6304.3
I_18020_053.eps
200808

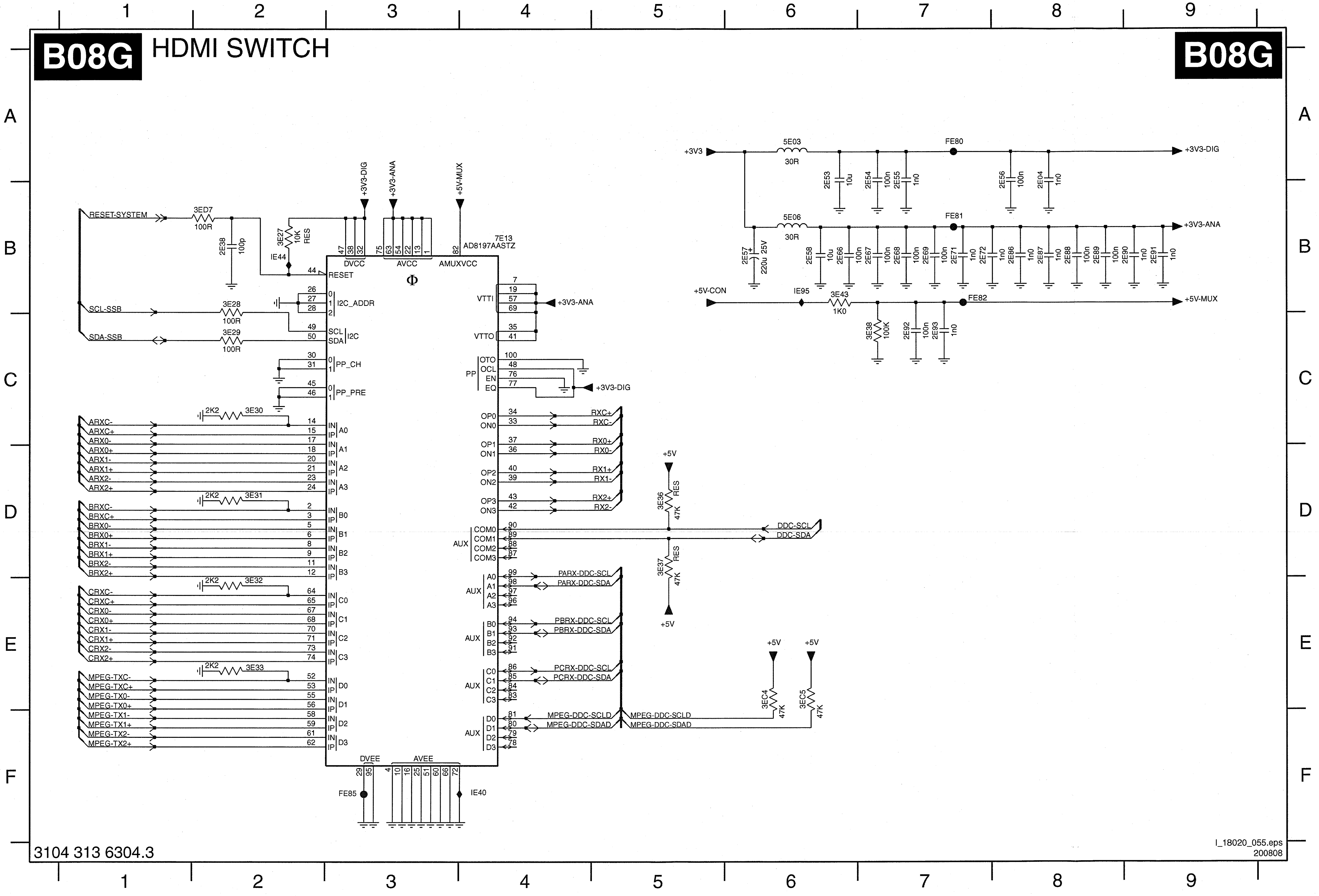
1P0A	C2
1P0B	D2
1P9A	C2
1P9B	D2
2E12	C2
2E14	D2
2E15	D4
2E18	D3
2E20	C4
2E21	B3
3E12	B3
3E15	D3
3E22	D3
3E23	C3
6E09	D2
6E22	B2
FE69	B2
FE70	D2
IE78	B4
IE83	D4

SSB: HDMI


B08F
HDMI
B08F
HDMI CONNECTOR 3 SIDE
HDMI CONNECTOR 2
HDMI CONNECTOR 1
EDID NVM
HDMI 3
SIDE
EDID NVM
HDMI 2
EDID NVM
HDMI 1
EEPROM
(256x8)
M24C02-WDW6
BC847BW
BAT54
DC1R019JBAR190
CIN-5V
+5V-EDID
CIN-5V-EDID
BIN-5V
BIN-5V-EDID
AIN-5V
AIN-5V-EDID
CRX-DDC-SCL
CRX-DDC-SDA
PCRX-DDC-SCL
PCRX-DDC-SDA
CRX-HOTPLUG
HOT-PLUG
WRITE-PROT
WC-EEPROM-PNX5100
BRX-DDC-SCL
BRX-DDC-SDA
PBRX-DDC-SCL
PBRX-DDC-SDA
BRX-HOTPLUG
ARX-DDC-SCL
ARX-DDC-SDA
PARX-DDC-SCL
PARX-DDC-SDA
ARX-HOTPLUG
PCEC-HDMI
CEC-HDMI
+3V3-STANDBY
+5V-CON
RES
3104 313 6304.3
I_18020_054.eps
200808

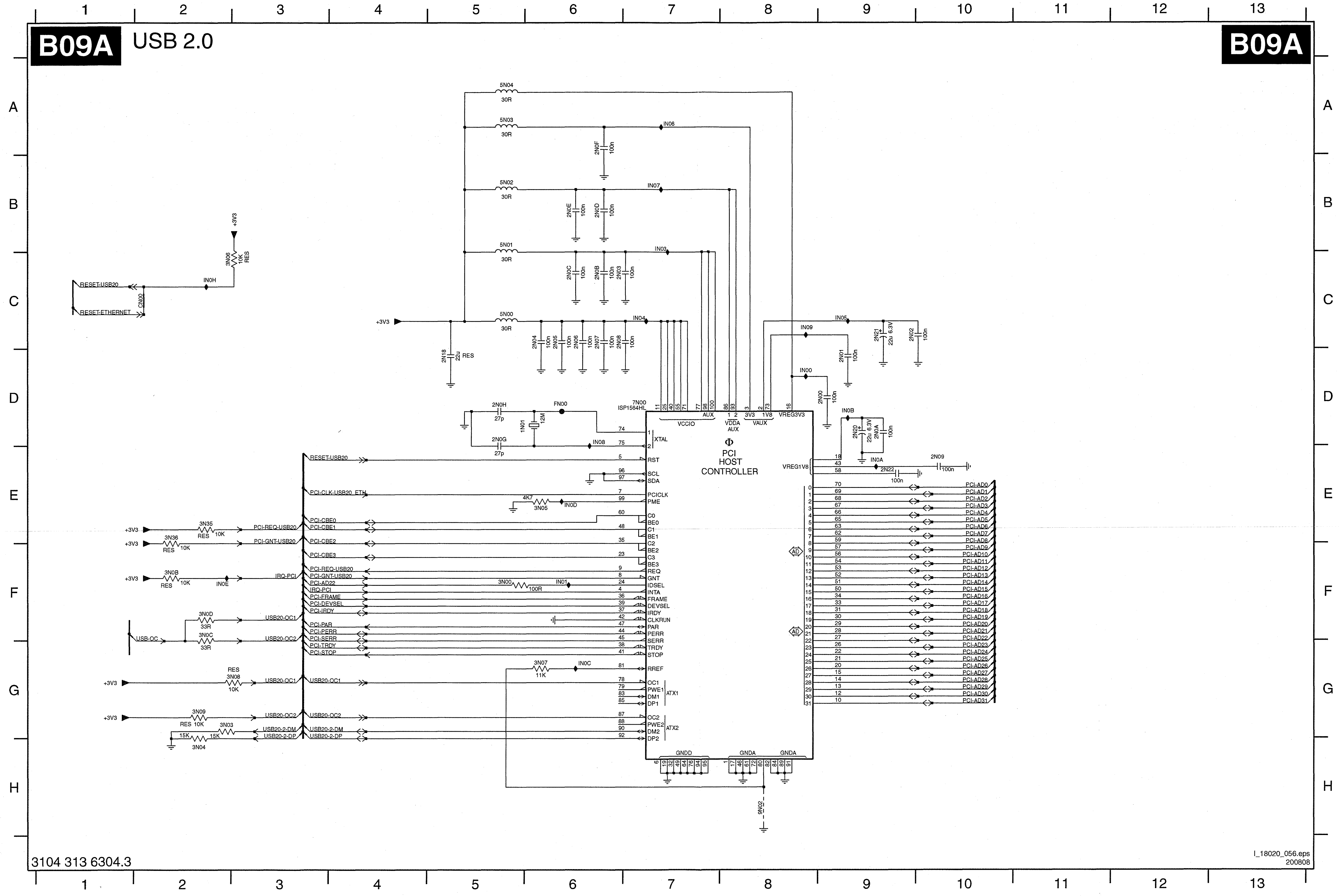
1P02	F1
1P03	A8
1P05	A1
1P50	C9
1P51	B10
1P52	B10
1P53	C2
1P54	B3
1P55	B3
1P56	D4
1P57	D11
1P58	G2
1P59	F3
1P5A	F4
1P5B	H4
2E10	B5
2E22	B5
2E23	D5
2E24	F5
2E25	F5
2E27	B12
2E28	B12
2E34	D12
2E94	H5
3E40	B5
3E44	B6
3E45	B6
3E48	C6
3E50	C6
3E53	C4
3E54	D3
3E56	H3
3E57	H4
3E58	G5
3E59	G6
3E60	G6
3E67	G6
3E68	G5
3E75	D10
3E84	H6
3E88	C13
3E91	F9
3E92	F9
3E94	C11
3E95	D13
3E96	B13
3E97	B13
3EB4	B12
3EB5	B12
3EC1	E4
3EC2	B5
3ED8	G9
5E07	A5
5E08	F5
5E09	A12
6E03	I2
6E06	A4
6E23	G12
6E26	A12
6E29	I5
7E08	B11
7E09	D12
7E10	F9
7E11	H5
7E12	G4
7E19	E5
7E20	C5
7E21	B4
9E04	C12
9E07	A6
9E11	A6
9E12	E10
9E13	C5
9E14	D5
9E15	H6
9E16	F10
9E17	F6
9E18	F6
9E19	A13
9E20	A13
FE30	B1
FE31	B1
FE32	B1
FE33	B1
FE34	G1
FE35	G1
FE36	G1
FE37	G1
FE48	C8
FE49	B9
FE50	B9
FE51	B8
FE53	B8
FE54	B8
FE59	G1
FE71	G1
FE72	B12
FE73	C1
FE74	B1
FE90	G5
FE91	B5
IE03	B4
IE08	C5
IE09	C5
IE11	D5
IE12	E4
IE13	G4
IE14	H5
IE15	H5
IE16	D13
IE17	D12
IE18	C11
IE19	F10
IE22	F9
IE23	F9
IE28	E13
IE29	A12
IE31	B12
IE33	B5
IE34	G5
IE41	D3
IE45	I5
IE46	A12
IE47	A4
IE65	G9

SSB: HDMI


B08G
HDMI SWITCH
B08G
1 2 3 4 5 6 7 8 9
A B C D E F
RESET-SYSTEM
3ED7 100R
2E38 100p
3E27 10K RES
IE44
+3V3-DIG
+3V3-ANA
+5V-MUX
7E13
AD8197AASTZ
DVCC
AVCC
AMUXVCC
RESET
Φ
I2C_ADDR
SCL-SSB
3E28 100R
SDA-SSB
3E29 100R
SCL
SDA
I2C
PP_CH
PP_PRE
VTTI
VTTO
+3V3-ANA
OTO
OCL
EN
EQ
PP
+3V3-DIG
2K2 3E30
ARXC-
ARXC+
ARX0-
ARX0+
ARX1-
ARX1+
ARX2-
ARX2+
A0 A1 A2 A3
2K2 3E31
BRXC-
BRXC+
BRX0-
BRX0+
BRX1-
BRX1+
BRX2-
BRX2+
B0 B1 B2 B3
2K2 3E32
CRXC-
CRXC+
CRX0-
CRX0+
CRX1-
CRX1+
CRX2-
CRX2+
C0 C1 C2 C3
2K2 3E33
MPEG-TXC-
MPEG-TXC+
MPEG-TX0-
MPEG-TX0+
MPEG-TX1-
MPEG-TX1+
MPEG-TX2-
MPEG-TX2+
D0 D1 D2 D3
OP0 ON0 OP1 ON1 OP2 ON2 OP3 ON3
RXC+
RXC-
RX0+
RX0-
RX1+
RX1-
RX2+
RX2-
AUX
COM0 COM1 COM2 COM3
DDC-SCL
DDC-SDA
+5V
3E36 47K RES
3E37 47K RES
PARX-DDC-SCL
PARX-DDC-SDA
PBRX-DDC-SCL
PBRX-DDC-SDA
PCRX-DDC-SCL
PCRX-DDC-SDA
MPEG-DDC-SCLD
MPEG-DDC-SDAD
3EC4 47K
3EC5 47K
DVEE
AVEE
FE85
IE40
+3V3
5E03 30R
FE80
+3V3-DIG
2E53 10u
2E54 100n
2E55 1n0
2E56 100n
2E04 1n0
5E06 30R
FE81
+3V3-ANA
2E57 220u 25V
2E58 10u
2E66 100n
2E67 1n0
2E68 100n
2E69 1n0
2E71 100n
2E72 1n0
2E86 100n
2E87 1n0
2E88 100n
2E89 1n0
2E90 100n
2E91 1n0
+5V-CON
IE95
3E43 1K0
FE82
+5V-MUX
3E38 100K
2E92 100n
2E93 1n0
3104 313 6304.3
I_18020_055.eps
200808

2E04	A8
2E38	B2
2E53	A6
2E54	A7
2E55	A7
2E56	A8
2E57	B6
2E58	B6
2E66	B6
2E67	B7
2E68	B7
2E69	B7
2E71	B7
2E72	B7
2E86	B8
2E87	B8
2E88	B8
2E89	B8
2E90	B9
2E91	B9
2E92	C7
2E93	C7
3E27	B2
3E28	B2
3E29	C2
3E30	C2
3E31	D2
3E32	E2
3E33	E2
3E36	D5
3E37	D5
3E38	C7
3E43	B6
3EC4	E6
3EC5	E6
3ED7	B2
5E03	A6
5E06	B6
7E13	B4
FE80	A7
FE81	B7
FE82	B7
FE85	F3
IE40	F4
IE44	B2
IE95	B6

SSB: USB 2.0


B09A
USB 2.0
B09A
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H
7N00
ISP1564HL
PCI
HOST
CONTROLLER
VCCIO
AUX
VDDA AUX
3V3
1V8
VAUX
VREG3V3
VREG1V8
XTAL
RST
SCL
SDA
PCICLK
PME
C0 BE0
C1 BE1
C2 BE2
C3 BE3
REQ
GNT
IDSEL
INTA
FRAME
DEVSEL
IRDY
CLKRUN
PAR
PERR
SERR
TRDY
STOP
RREF
OC1
PWE1
DM1
DP1
ATX1
OC2
PWE2
DM2
DP2
ATX2
GNDD
GNDA
GNDA
AD
5N04 30R
5N03 30R
5N02 30R
5N01 30R
5N00 30R
+3V3
2N18 22u RES
IN06
IN07
IN03
IN04
IN05
IN09
IN00
IN0B
IN0A
IN08
IN0D
IN01
IN0C
IN0E
IN0H
2N0F 100n
2N0E 100n
2N0D 100n
2N0C 100n
2N0B 100n
2N03 100n
2N04 100n
2N05 100n
2N06 100n
2N07 100n
2N08 100n
2N21 22u 6.3V
2N02 100n
2N01 100n
2N00 100n
2N20 22u 6.3V
2N0A 100n
2N09 100n
2N22 100n
2N0H 27p
2N0G 27p
FN00
1N01 12M
3N06 10K RES
RESET-USB20
RESET-ETHERNET
CN00
PCI-CLK-USB20_ETH
4K7
3N05
PCI-CBE0
PCI-CBE1
PCI-CBE2
PCI-CBE3
3N35 RES 10K
3N36 RES 10K
PCI-REQ-USB20
PCI-GNT-USB20
3N0B RES 10K
IRQ-PCI
PCI-AD22
PCI-FRAME
PCI-DEVSEL
PCI-IRDY
3N00 100R
3N0D 33R
3N0C 33R
USB-OC
USB20-OC1
USB20-OC2
PCI-PAR
PCI-PERR
PCI-SERR
PCI-TRDY
PCI-STOP
3N07 11K
3N08 RES 10K
3N09 RES 10K
3N03 15K
3N04 15K
USB20-2-DM
USB20-2-DP
PCI-AD0 … PCI-AD31
9N02
3104 313 6304.3
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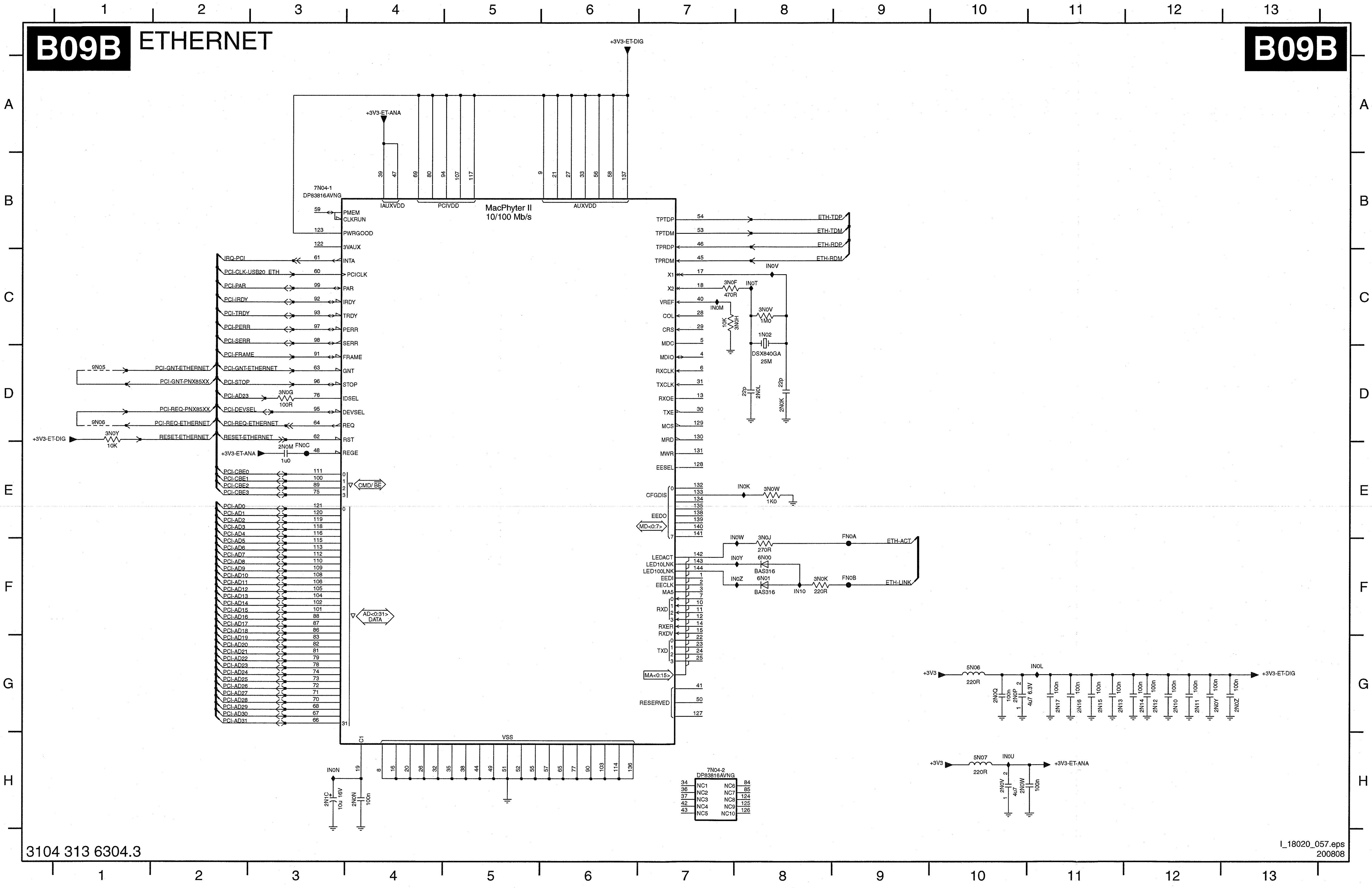
1N01	D5
2N00	D9
2N01	D9
2N02	C9
2N03	C6
2N04	C6
2N05	C6
2N06	C6
2N07	C6
2N08	C6
2N09	E10
2N0A	D9
2N0B	C6
2N0C	C6
2N0D	B6
2N0E	B6
2N0F	A6
2N0G	D5
2N0H	D5
2N18	D5
2N20	D9
2N21	C9
2N22	E9
3N00	F5
3N03	G2
3N04	H2
3N05	E6
3N06	C2
3N07	G6
3N08	G3
3N09	G2
3N0B	F2
3N0C	F2
3N0D	F2
3N35	E2
3N36	E2
5N00	C5
5N01	B5
5N02	B5
5N03	A5
5N04	A5
7N00	D7
9N02	H8
CN00	C2
FN00	D6
IN00	D8
IN01	F6
IN03	B7
IN04	C7
IN05	C9
IN06	A7
IN07	B7
IN08	D6
IN09	C8
IN0A	E9
IN0B	D9
IN0C	G6
IN0D	E6
IN0E	F2
IN0H	C2

SSB: Ethernet

1N00 B11
1N02 C8
2N0K D8
2N0L D8
2N0M E3
2N0N H4
2N0P G10
2N0Q G10
2N0R B9
2N0S C9
2N0T B10
2N0U B10
2N0V H10
2N0W H10
2N0Y G12
2N0Z G13
2N10 G12
2N11 G12
2N12 G12
2N13 G11
2N14 G12
2N15 G11
2N16 G11
2N17 G11
2N1C H3
3N0F C7
3N0G D3
3N0H C7
3N0J F8
3N0K F8
3N0L-1 A8
3N0L-2 A9
3N0L-3 A8
3N0L-4 A8
3N0N-1 A9
3N0N-2 A9
3N0N-3 A9
3N0N-4 A9
3N0T-1 B9
3N0T-2 B9
3N0T-3 C9
3N0T-4 C9
3N0V C8
3N0W E8
3N0Y D1
5N06 G10
5N07 H10
6N00 F8
6N01 F8
7N04-1 B3
7N04-2 H7
9N05 D1
9N06 D1
FN05 A10
FN06 A10
FN07 B10
FN08 B11
FN09 C11
FN0A E9
FN0B F9
FN0C E3
FN15 B10
IN0K E8
IN0L G11
IN0M C7
IN0N H3
IN0P A9
IN0T C8
IN0U H10
IN0V C8
IN0W E8
IN0Y F8
IN0Z F8
IN10 F8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12
13
A
B
C
D
E
F
G
H
B09B
ETHERNET
B09B
+3V3-ET-DIG
+3V3-ET-ANA
7N04-1
DP83816AVNG
MacPhyter II
10/100 Mb/s
IAUXVDD
PCIVDD
AUXVDD
39
47
69
80
94
107
117
9
21
27
33
56
58
137
59 PMEM
CLKRUN
123 PWRGOOD
122 3VAUX
IRQ-PCI 61 INTA
PCI-CLK-USB20_ETH 60 PCICLK
PCI-PAR 99 PAR
PCI-IRDY 92 IRDY
PCI-TRDY 93 TRDY
PCI-PERR 97 PERR
PCI-SERR 98 SERR
PCI-FRAME 91 FRAME
9N05
PCI-GNT-ETHERNET
PCI-GNT-ETHERNET 63 GNT
PCI-GNT-PNX85XX
PCI-STOP 96 STOP
PCI-AD23 3N0G 100R 76 IDSEL
PCI-REQ-PNX85XX
PCI-DEVSEL 95 DEVSEL
9N06
PCI-REQ-ETHERNET
PCI-REQ-ETHERNET 64 REQ
+3V3-ET-DIG
3N0Y 10K
RESET-ETHERNET
RESET-ETHERNET 62 RST
+3V3-ET-ANA 2N0M 1u0 FN0C 48 REGE
PCI-CBE0 111 0
PCI-CBE1 100 1
PCI-CBE2 89 2
PCI-CBE3 75 3
CMD/ BE
PCI-AD0 121 0
PCI-AD1 120
PCI-AD2 119
PCI-AD3 118
PCI-AD4 116
PCI-AD5 115
PCI-AD6 113
PCI-AD7 112
PCI-AD8 110
PCI-AD9 109
PCI-AD10 108
PCI-AD11 106
PCI-AD12 105
PCI-AD13 104
PCI-AD14 102
PCI-AD15 101
PCI-AD16 88
PCI-AD17 87
PCI-AD18 86
PCI-AD19 83
PCI-AD20 82
PCI-AD21 81
PCI-AD22 79
PCI-AD23 78
PCI-AD24 74
PCI-AD25 73
PCI-AD26 72
PCI-AD27 71
PCI-AD28 70
PCI-AD29 68
PCI-AD30 67
PCI-AD31 66 31
AD<0:31>
DATA
TPTDP 54 ETH-TDP
TPTDM 53 ETH-TDM
TPRDP 46 ETH-RDP
TPRDM 45 ETH-RDM
X1 17 IN0V
X2 18 3N0F 470R IN0T
VREF 40 IN0M
10K 3N0H
3N0V 1M0
1N02
DSX840GA
25M
22p 2N0L
22p 2N0K
COL 28
CRS 29
MDC 5
MDIO 4
RXCLK 6
TXCLK 31
RXOE 13
TXE 30
MCS 129
MRD 130
MWR 131
EESEL 128
CFGDIS 0 132
133 IN0K 3N0W 1K0
134
135
138
EEDO 139
MD<0:7> 140
141 7
IN0W 3N0J 270R FN0A ETH-ACT
LEDACT 142
LED10LNK 143 IN0Y 6N00 BAS316
LED100LNK 144
EEDI 1
EECLK 2 IN0Z 6N01 BAS316 IN10 3N0K 220R FN0B ETH-LINK
MA5 3
7
RXD 0 10
1 11
2 12
3 14
RXER 15
RXDV 22
TXD 0 23
1 24
2 25
3
MA<0:15>
RESERVED 41
50
127
C1
VSS
IN0N 19
2N1C 10u 16V
2N0N 100n
8
16
20
26
32
35
38
44
49
51
52
55
57
65
77
90
103
114
136
7N04-2
DP83816AVNG
34 NC1
36 NC2
37 NC3
42 NC4
43 NC5
NC6 84
NC7 85
NC8 124
NC9 125
NC10 126
+3V3 5N06 220R IN0L +3V3-ET-DIG
2N0Q 100n
2N0P 2 4u7 6.3V 1
2N17 100n
2N16 100n
2N15 100n
2N13 100n
2N14 100n
2N12 100n
2N10 100n
2N11 100n
2N0Y 100n
2N0Z 100n
+3V3 5N07 220R IN0U +3V3-ET-ANA
2N0V 2 4u7 1
2N0W 100n

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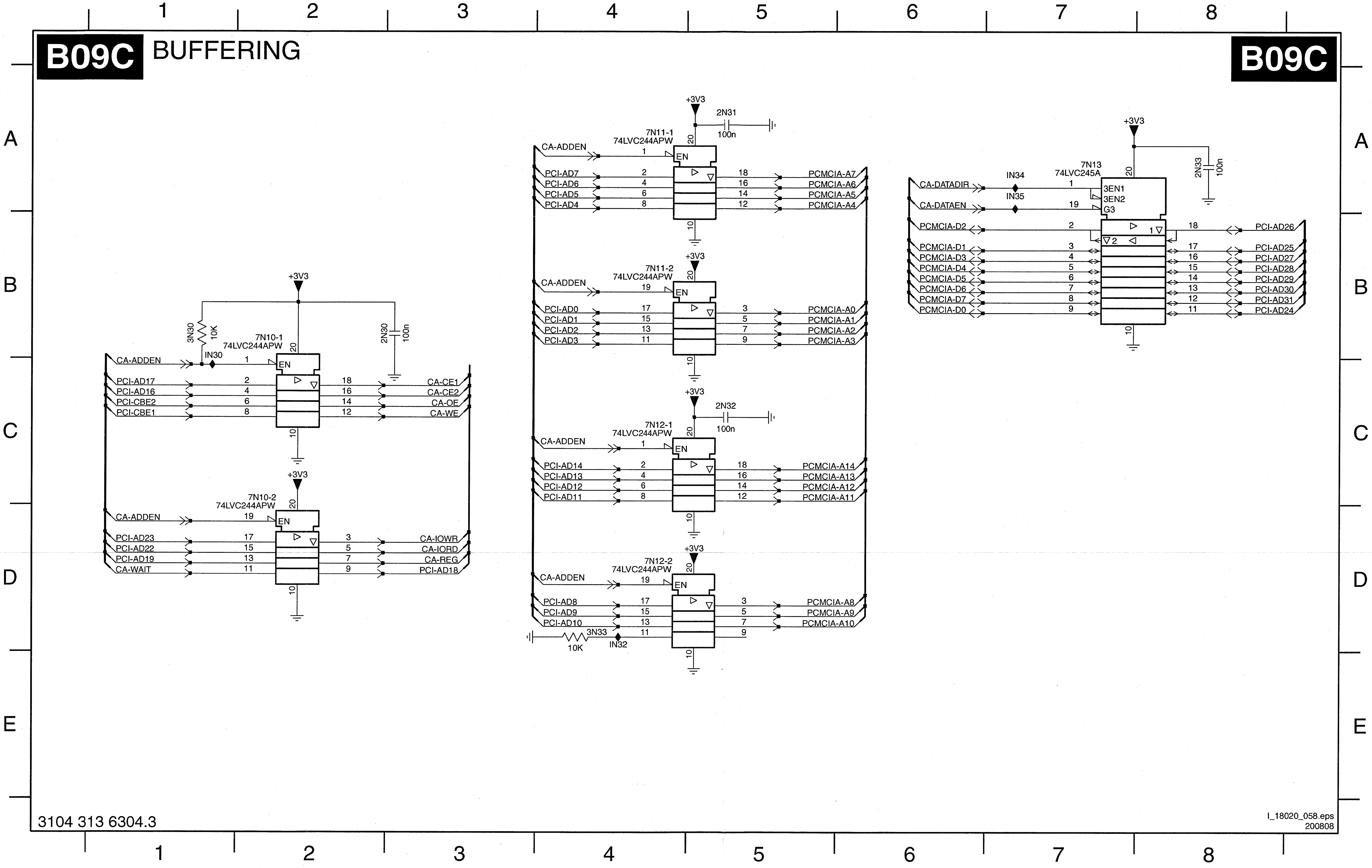
SSB: Buffering


B09C BUFFERING
B09C
7N10-1
74LVC244APW
7N10-2
74LVC244APW
7N11-1
74LVC244APW
7N11-2
74LVC244APW
7N12-1
74LVC244APW
7N12-2
74LVC244APW
7N13
74LVC245A
+3V3
2N30 100n
2N31 100n
2N32 100n
2N33 100n
3N30 10K
3N33 10K
IN30
IN32
IN34
IN35
EN
3EN1
3EN2
G3
CA-ADDEN
CA-DATADIR
CA-DATAEN
PCI-AD17
PCI-AD16
PCI-CBE2
PCI-CBE1
CA-CE1
CA-CE2
CA-OE
CA-WE
PCI-AD23
PCI-AD22
PCI-AD19
CA-WAIT
CA-IOWR
CA-IORD
CA-REG
PCI-AD18
PCI-AD7
PCI-AD6
PCI-AD5
PCI-AD4
PCMCIA-A7
PCMCIA-A6
PCMCIA-A5
PCMCIA-A4
PCI-AD0
PCI-AD1
PCI-AD2
PCI-AD3
PCMCIA-A0
PCMCIA-A1
PCMCIA-A2
PCMCIA-A3
PCI-AD14
PCI-AD13
PCI-AD12
PCI-AD11
PCMCIA-A14
PCMCIA-A13
PCMCIA-A12
PCMCIA-A11
PCI-AD8
PCI-AD9
PCI-AD10
PCMCIA-A8
PCMCIA-A9
PCMCIA-A10
PCMCIA-D2
PCMCIA-D1
PCMCIA-D3
PCMCIA-D4
PCMCIA-D5
PCMCIA-D6
PCMCIA-D7
PCMCIA-D0
PCI-AD26
PCI-AD25
PCI-AD27
PCI-AD28
PCI-AD29
PCI-AD30
PCI-AD31
PCI-AD24
A
B
C
D
E
1
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2N30	B3
2N31	A5
2N32	C5
2N33	A8
3N30	B1
3N33	D4
7N10-1	B2
7N10-2	C2
7N11-1	A4
7N11-2	B4
7N12-1	C4
7N12-2	D4
7N13	A7
IN30	B1
IN32	D4
IN34	A7
IN35	A7

SSB: SRP List Explanation

Example

Net Name	*Diagram*
+12-15V	AP1 (4x)
+12-15V	AP4 (4x)
+12-15V	AP5 (12x)
+12-15V	AP6 (4x)
+12-15V	AP7 (8x)
+12V	AP1 (4x)
+12V_NF	AP1 (2x)
+12VAL	AP1 (2x)
+25VLP	AP1 (4x)
+25VLP	AP2 (1x)
+3V3-STANDBY	AP5 (3x)
+400V-F	AP1 (2x)
+400V-F	AP2 (2x)
+400V-F	AP3 (2x)
+5V2	AP1 (6x)
+5V2	AP2 (1x)
+5V2-NF	AP1 (1x)
+5V2-NF	AP2 (1x)
+5V-SW	AP1 (6x)
+5V-SW	AP2 (1x)
+8V6	AP1 (3x)
+AUX	AP1 (2x)
+AUX	AP2 (1x)
+DC-F	AP1 (2x)
+DC-F	AP3 (2x)
+SUB-SPEAKER	AP5 (1x)
+SUB-SPEAKER	AP6 (2x)
-12-15V	AP1 (4x)
-12-15V	AP4 (6x)
-12-15V	AP5 (14x)
-12-15V	AP6 (6x)
-12-15V	AP7 (8x)
AL-OFF	AP1 (2x)
AUDIO-L	AP4 (1x)
AUDIO-L	AP5 (1x)
AUDIO-PROT	AP5 (3x)
AUDIO-R	AP4 (1x)
AUDIO-R	AP5 (1x)
AUDIO-SW	AP5 (1x)
AUDIO-SW	AP7 (1x)
BOOST	AP1 (2x)
CPROT	AP4 (2x)
CPROT	AP5 (1x)
CPROT-SW	AP5 (1x)
CPROT-SW	AP6 (2x)
-DC-F	AP1 (2x)
-DC-F	AP3 (2x)
DC-PROT	AP1 (1x)
DC-PROT	AP5 (2x)
DIM-CONTROL	AP1 (2x)
FEEDBACK+SW	AP6 (2x)
FEEDBACK-L	AP4 (2x)
FEEDBACK-R	AP4 (2x)
FEEDBACK-SW	AP6 (2x)
GND-AL	AP1 (2x)
GNDHA	AP1 (40x)
GNDHA	AP2 (20x)
GNDHA	AP3 (2x)
GNDHOT	AP3 (2x)
GND-L	AP1 (2x)
GND-L	AP4 (4x)
GND-L	AP5 (34x)
GND-LL	AP4 (7x)
GND-LL	AP5 (1x)
GND-LR	AP4 (7x)
GND-LR	AP5 (1x)
GND-LSW	AP5 (1x)
GND-LSW	AP6 (15x)
GND-S	AP1 (11x)
GND-SA	AP4 (8x)
GND-SA	AP5 (2x)
GND-SA	AP6 (8x)
GND-SA	AP7 (6x)
GNDscrew	AP3 (2x)
GNDscrew	AP5 (2x)
GND-SSB	AP5 (3x)
GND-SSP	AP1 (51x)
GND-SSP	AP2 (15x)
IN+SW	AP6 (2x)
IN-L	AP4 (2x)
IN-R	AP4 (2x)
IN-SW	AP6 (2x)
INV-MUTE	AP4 (1x)
INV-MUTE	AP5 (1x)
INV-MUTE	AP6 (1x)
LEFT-SPEAKER	AP4 (1x)
LEFT-SPEAKER	AP5 (1x)
MUTE	AP4 (2x)
MUTE	AP5 (1x)
MUTE	AP6 (2x)
ON-OFF	AP1 (3x)
OUT	AP6 (1x)
OUT	AP7 (2x)
OUTN	AP6 (1x)
OUTN	AP7 (1x)
POWER-GOOD	AP1 (2x)
POWER-OK-PLATFORM	AP1 (2x)
RIGHT-SPEAKER	AP4 (1x)
RIGHT-SPEAKER	AP5 (1x)
SOUND-ENABLE	AP5 (3x)
STANDBY	AP1 (5x)
STANDBY	AP2 (1x)
-SUB-SPEAKER	AP5 (1x)
-SUB-SPEAKER	AP6 (2x)
V-CLAMP	AP1 (1x)
V-CLAMP	AP3 (2x)

1.1. Introduction

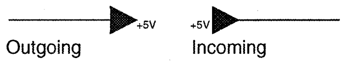
SRP (Service Reference Protocol) is a software tool that creates a list with all references to signal lines. The list contains references to the signals within all schematics of a PWB. It replaces the text references currently printed next to the signal names in the schematics. These printed references are created manually and are therefore not guaranteed to be 100% correct. In addition, in the current crowded schematics there is often none or very little place for these references.
Some of the PWB schematics will use SRP while others will still use the manual references. Either there will be an SRP reference list for a schematic, or there will be printed references in the schematic.

1.2. Non-SRP Schematics

There are several different signals available in a schematic:

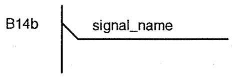
1.2.1. Power Supply Lines

All power supply lines are available in the supply line overview (see chapter 6). In the schematics (see chapter 7) is not indicated where supplies are coming from or going to.
It is however indicated if a supply is incoming (created elsewhere), or outgoing (created or adapted in the current schematic).



1.2.2. Normal Signals

For normal signals, a schematic reference (e.g. B14b) is placed next to the signals.

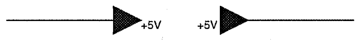


1.2.3. Grounds

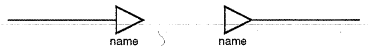
For normal and special grounds (e.g. GNDHOT or GND3V3 etc.), nothing is indicated.

1.3. SRP Schematics

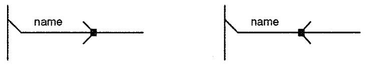
SRP is a tool, which automatically creates a list with signal references, indicating on which schematic the signals are used.
A reference is created for all signals indicated with an SRP symbol, these symbols are:



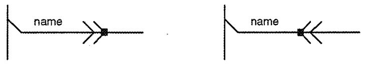
Power supply line.



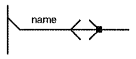
Stand alone signal or switching line (used as less as possible).



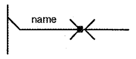
Signal line into a wire tree.



Switching line into a wire tree.



Bi-directional line (e.g. SDA) into a wire tree.



Signal line into a wire tree, its direction depends on the circuit (e.g. ingoing for PDP, outgoing for LCD sets).

Remarks:

- When there is a black dot on the "signal direction arrow" it is an SRP symbol, so there will be a reference to the signal name in the SRP list.
- All references to normal grounds (Ground symbols without additional text) are not listed in the reference list, this to keep it concise.
- Signals that are not used in multiple schematics, but only once or several times in the same schematic, are included in the SRP reference list, but only with one reference.

Additional Tip:

When using the PDF service manual file, you can very easily search for signal names and follow the signal over all the schematics. In Adobe PDF reader:

- Select the signal name you want to search for, with the "Select text" tool.
- Copy and paste the signal name in the "Search PDF" tool.
- Search for all occurrences of the signal name.
- Now you can quickly jump between the different occurrences and follow the signal over all schematics. It is advised to "zoom in" to e.g. 150% to see clearly, which text is selected. Then you can zoom out, to get an overview of the complete schematic.

PS. It is recommended to use at least Adobe PDF (reader) version 6.x, due to better search possibilities in this version.

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Personal Notes:

SSB: SRP List Part 1

Netname	Diagram
+12V	B01A
+12V	B01B
+12V	B04C
+12V	B04G
+12V	B04I
+12V	B04M
+12V	B05G
+12V	B05H
+12V	B08A
+12V	B08B
+12V	B08E
+12VF	B01A
+12VF	B01B
+12VF	B01C
+12VFF	B01C
+1V	B01B
+1V	B03E
+1V2DVB	B02A
+1V2-PNX5100	B01C
+1V2-PNX5100	B04A
+1V2-PNX5100	B05C
+1V2-PNX5100-CLOCK	B05C
+1V2-PNX5100-DDR-PLL1	B05C
+1V2-PNX5100-DLL	B05C
+1V2-PNX5100-LVDS-PLL	B05C
+1V2-PNX5100-TRI-PLL1	B05C
+1V2-PNX5100-TRI-PLL2	B05C
+1V2-PNX5100-TRI-PLL3	B05C
+1V2-PNX8541	B01A
+1V2-PNX8541	B01B
+1V2-PNX8541	B02A
+1V2-PNX8541	B04A
+1V2-PNX8541	B04E
+1V2-PNX8541	B04P
+1V2-STANDBY	B01A
+1V2-STANDBY	B01B
+1V2-STANDBY	B04P
+1V8DVBC	B02C
+1V8-PNX5100	B05A
+1V8-PNX5100	B05C
+1V8-PNX5100	B08D
+1V8-PNX8541	B04G
+1V8-PNX8541	B04P
+1V8-PNX8541	B08D
+1VTMDS	B03E
+2V5	B01B
+2V5	B03A
+2V5	B03C
+2V5	B03E
+2V5-CLKGENA	B03E
+2V5-REF	B01B
+33VTUN	B01B
+33VTUN	B02B
+3V3	B01A
+3V3	B01D
+3V3	B02A
+3V3	B02B
+3V3	B02C
+3V3	B03A
+3V3	B03B
+3V3	B03E
+3V3	B03G
+3V3	B03H
+3V3	B04A
+3V3	B04L
+3V3	B04M
+3V3	B04P
+3V3	B04Q
+3V3	B05C
+3V3	B05E
+3V3	B05F
+3V3	B05G
+3V3	B05H
+3V3	B05I
+3V3	B08A
+3V3	B08D
+3V3	B08G
+3V3	B09A
+3V3	B09B
+3V3	B09C
+3V3-ANA	B08G
+3V3-DIG	B08G
+3V3DVB	B02A
+3V3DVBC	B02C
+3V3-ET-ANA	B03F
+3V3-ET-ANA	B09B
+3V3-ET-DIG	B09B
+3V3-ET-LED	B03F
+3V3F	B01A
+3V3F	B01B
+3V3F	B04G
+3V3-NAND	B04Q
+3V3-PER	B04C
+3V3-PER	B04E
+3V3-PER	B04P
+3V3-PNX5100-CLOCK	B05C
+3V3-PNX5100-DDR-PLL0	B05C
+3V3-PNX5100-LVDS-IN	B05C
+3V3-PNX5100-LVDS-PLL	B05C
+3V3-STANDBY	B01B
+3V3-STANDBY	B01D
+3V3-STANDBY	B04A
+3V3-STANDBY	B04D
+3V3-STANDBY	B04P
+3V3-STANDBY	B08D
+3V3-STANDBY	B08F
+3V3TMDS	B03D
+3V3TMDS	B03E
+4V-STANDBY	B01B
+4V-STANDBY	B05E
+5V	B01C
+5V	B01D
+5V	B03F
+5V	B04A
+5V	B04L
+5V	B05E
+5V	B08A
+5V	B08B
+5V	B08F
+5V	B08G
+5V5-TUN	B01C
+5V5-TUN	B04C
+5V-CON	B08F
+5V-CON	B08G
+5V-EDID	B08F
+5V-MUX	B08G
+5V-TUN	B02A
+5V-TUN	B02B
+5V-TUN	B04C
+VCC-LM	B01B
+VDISP1	B05E
+VDISP1	B05H
+VDISP2	B05E
+VDISP2	B05H
+VTUN	B02B
27MHZ-3V3	B03A (2x)
2V5-LMI	B03C (6x)
2V5-LMI	B03E (2x)
3V3-ST	B01A (1x)
3V3-ST	B01B (1x)
4-MHz	B02A (1x)
4-MHz	B02B (2x)
ADAC(1)	B04L (1x)
ADAC(2)	B04L (1x)
ADAC(3)	B04L (1x)
ADAC(3)	B04M (1x)
ADAC(4)	B04L (1x)
ADAC(4)	B04M (1x)
ADAC(5)	B04I (1x)
ADAC(5)	B04L (1x)
ADAC(6)	B04I (1x)
ADAC(6)	B04L (1x)
ADAC(7)	B04I (1x)
ADAC(7)	B04L (3x)
ADAC(8)	B04I (1x)
ADAC(8)	B04L (3x)
AGC-COMP	B02A (2x)
AIN-5V	B08F (4x)
AIN-5V-EDID	B08F (2x)
ALE	B04A (2x)
A-PLOP	B04M (1x)
A-PLOP	B08A (3x)
AP-SCART-OUT-L	B08A (3x)
AP-SCART-OUT-R	B08A (3x)
ARX0-	B08F (1x)
ARX0-	B08G (1x)
ARX0+	B08F (1x)
ARX0+	B08G (1x)
ARX1-	B08F (1x)
ARX1-	B08G (1x)
ARX1+	B08F (1x)
ARX1+	B08G (1x)
ARX2-	B08F (1x)
ARX2-	B08G (1x)
ARX2+	B08F (1x)
ARX2+	B08G (1x)
ARXC-	B08F (1x)
ARXC-	B08G (1x)
ARXC+	B08F (1x)
ARXC+	B08G (1x)
ARX-DDC-SCL	B08F (2x)
ARX-DDC-SDA	B08F (2x)
ARX-HOTPLUG	B08F (2x)
ASEBRKn	B03A (1x)
ASEBRKn	B03G (1x)
AUDIO-CLK	B04L (1x)
AUDIO-CLK	B05E (1x)
AUDIO-CL-L	B04I (1x)
AUDIO-CL-L	B08A (1x)
AUDIO-CL-R	B04I (1x)
AUDIO-CL-R	B08A (1x)
AUDIO-HDPH-L-AP	B04M (1x)
AUDIO-HDPH-L-AP	B08B (1x)
AUDIO-HDPH-R-AP	B04M (1x)
AUDIO-HDPH-R-AP	B08B (1x)
AUDIO-IN1-L	B04L (1x)
AUDIO-IN1-L	B08A (1x)
AUDIO-IN1-R	B04L (1x)
AUDIO-IN1-R	B08A (1x)
AUDIO-IN2-L	B04L (1x)
AUDIO-IN2-L	B08A (1x)
AUDIO-IN2-R	B04L (1x)
AUDIO-IN2-R	B08A (1x)
AUDIO-IN3-L	B04L (1x)
AUDIO-IN3-L	B08A (1x)
AUDIO-IN3-R	B04L (1x)
AUDIO-IN3-R	B08A (1x)
AUDIO-IN4-L	B04L (1x)
AUDIO-IN4-L	B08E (1x)
AUDIO-IN4-R	B04L (1x)
AUDIO-IN4-R	B08E (1x)
AUDIO-IN5-L	B04L (1x)
AUDIO-IN5-L	B08B (1x)
AUDIO-IN5-R	B04L (1x)
AUDIO-IN5-R	B08B (1x)
AUDIO-MCK	B04L (1x)
AUDIO-MCK	B05E (1x)
AUDIO-OUT-L	B04I (1x)
AUDIO-OUT-L	B08A (1x)
AUDIO-OUT-R	B04I (1x)
AUDIO-OUT-R	B08A (1x)
AUDIO-SDO	B04L (1x)
AUDIO-SDO	B05E (1x)
AUDIO-VDD	B04I (5x)
AUDIO-WS	B04L (1x)
AUDIO-WS	B05E (1x)
AV1-BLK	B04A (1x)
AV1-BLK	B08A (1x)
AV1-PB	B04K (1x)
AV1-PB	B08A (1x)
AV1-PR	B04K (1x)
AV1-PR	B08A (1x)
AV1-STATUS	B04A (1x)
AV1-STATUS	B08A (1x)
AV1-Y	B04K (1x)
AV1-Y	B08A (1x)
AV1-Y_CVBS	B04K (1x)
AV1-Y_CVBS	B08A (1x)
AV2-BLK	B04A (1x)
AV2-BLK	B08A (1x)
AV2-C	B04K (1x)
AV2-STATUS	B04A (1x)
AV2-STATUS	B08A (1x)
AV2-Y_CVBS	B04K (1x)
AV2-Y_CVBS	B08A (1x)
AV3-PB	B04K (1x)
AV3-PB	B08A (1x)
AV3-PR	B04K (1x)
AV3-PR	B08A (1x)
AV3-Y	B04K (1x)
AV3-Y	B08A (1x)
BACKLIGHT-BOOST	B05H (1x)
BACKLIGHT-CTRL	B05H (2x)
BACKLIGHT-OUT	B05E (1x)
BACKLIGHT-OUT	B05H (1x)
BACKLIGHT-PWM-ANA-SSB	B05H (2x)
BIN-5V	B08F (4x)
BIN-5V-EDID	B08F (2x)
BOLT-ON-IO	B04A (2x)
BOOST-CTRL	B05H (3x)
BOOTMODE	B04E (2x)
BRX0-	B08F (1x)
BRX0-	B08G (1x)
BRX0+	B08F (1x)
BRX0+	B08G (1x)
BRX1-	B08F (1x)
BRX1-	B08G (1x)
BRX1+	B08F (1x)
BRX1+	B08G (1x)
BRX2-	B08F (1x)
BRX2-	B08G (1x)
BRX2+	B08F (1x)
BRX2+	B08G (1x)
BRXC-	B08F (1x)
BRXC-	B08G (1x)
BRXC+	B08F (1x)
BRXC+	B08G (1x)
BRX-DDC-SCL	B08F (2x)
BRX-DDC-SDA	B08F (2x)
BRX-HOTPLUG	B08F (2x)
BUF-RST-TARGETn	B03A (1x)
BUF-RST-TARGETn	B03G (1x)
B-VGA	B04K (1x)
B-VGA	B08A (1x)
B-VGA	B08B (1x)
CA-ADDEN	B04N (1x)
CA-ADDEN	B09C (6x)
CA-CD1	B03H (2x)
CA-CD1	B04N (1x)
CA-CD2	B03H (2x)
CA-CD2	B04N (1x)
CA-CE1	B03H (1x)
CA-CE1	B09C (1x)
CA-CE2	B03H (1x)
CA-CE2	B09C (1x)
CA-DATADIR	B04N (1x)
CA-DATADIR	B09C (1x)
CA-DATAEN	B04N (1x)
CA-DATAEN	B09C (1x)
CA-INPACK	B03H (2x)
CA-IORD	B03H (1x)
CA-IORD	B09C (1x)
CA-IOWR	B03H (1x)
CA-IOWR	B09C (1x)
CA-MDI0	B03A (1x)
CA-MDI0	B03H (1x)
CA-MDI0	B04N (1x)
CA-MDI1	B03A (1x)
CA-MDI1	B03H (1x)
CA-MDI1	B04N (1x)
CA-MDI2	B03A (1x)
CA-MDI2	B03H (1x)
CA-MDI2	B04N (1x)
CA-MDI3	B03A (1x)
CA-MDI3	B03H (1x)
CA-MDI3	B04N (1x)
CA-MDI4	B03A (1x)
CA-MDI4	B03H (1x)
CA-MDI4	B04N (1x)
CA-MDI5	B03A (1x)
CA-MDI5	B03H (1x)
CA-MDI5	B04N (1x)
CA-MDI6	B03A (1x)
CA-MDI6	B03H (1x)
CA-MDI6	B04N (1x)
CA-MDI7	B03A (1x)
CA-MDI7	B03H (1x)
CA-MDI7	B04N (1x)
CA-MDO0	B03A (1x)
CA-MDO0	B03H (2x)
CA-MDO0	B04N (1x)
CA-MDO1	B03A (1x)
CA-MDO1	B03H (2x)
CA-MDO1	B04N (1x)
CA-MDO2	B03A (1x)
CA-MDO2	B03H (2x)
CA-MDO2	B04N (1x)
CA-MDO3	B03A (1x)
CA-MDO3	B03H (2x)
CA-MDO3	B04N (1x)
CA-MDO4	B03A (1x)
CA-MDO4	B03H (2x)
CA-MDO4	B04N (1x)
CA-MDO5	B03A (1x)
CA-MDO5	B03H (2x)
CA-MDO5	B04N (1x)
CA-MDO6	B03A (1x)
CA-MDO6	B03H (2x)
CA-MDO6	B04N (1x)
CA-MDO7	B03A (1x)
CA-MDO7	B03H (2x)
CA-MDO7	B04N (1x)
CA-MICLK	B03A (1x)
CA-MICLK	B03H (1x)
CA-MICLK	B04N (1x)
CA-MISTRT	B03A (1x)
CA-MISTRT	B03H (1x)
CA-MISTRT	B04N (1x)
CA-MIVAL	B03A (1x)
CA-MIVAL	B03H (1x)
CA-MIVAL	B04N (1x)
CA-MOCLK_VS2	B03A (1x)
CA-MOCLK_VS2	B03H (2x)
CA-MOCLK_VS2	B04N (1x)
CA-MOSTRT	B03A (1x)
CA-MOSTRT	B03H (2x)
CA-MOSTRT	B04N (1x)
CA-MOVAL	B03A (1x)
CA-MOVAL	B03H (2x)
CA-MOVAL	B04N (1x)
CA-OE	B03H (1x)
CA-OE	B09C (1x)
CA-REG	B03H (1x)
CA-REG	B09C (1x)
CA-RST	B03H (1x)
CA-RST	B04N (1x)
CA-VS1	B03H (2x)
CA-VS1	B04N (1x)
CA-WAIT	B03H (2x)
CA-WAIT	B09C (1x)
CA-WE	B03H (1x)
CA-WE	B09C (1x)
CEC-HDMI	B04A (2x)
CEC-HDMI	B04H (1x)
CEC-HDMI	B08F (1x)
CIN-5V	B08F (4x)
CIN-5V-EDID	B08F (2x)
CONTRAST-GAIN	B05H (1x)
CPU-27MHZ	B03A (2x)
CRX0-	B08F (1x)
CRX0-	B08G (1x)
CRX0+	B08F (1x)
CRX0+	B08G (1x)
CRX1-	B08F (1x)
CRX1-	B08G (1x)
CRX1+	B08F (1x)
CRX1+	B08G (1x)
CRX2-	B08F (1x)
CRX2-	B08G (1x)
CRX2+	B08F (1x)
CRX2+	B08G (1x)
CRXC-	B08F (1x)
CRXC-	B08G (1x)
CRXC+	B08F (1x)
CRXC+	B08G (1x)
CRX-DDC-SCL	B08F (2x)
CRX-DDC-SDA	B08F (2x)
CRX-HOTPLUG	B08F (2x)
CTRL1-PNX5100	B05H (2x)
CTRL2-PNX5100	B05H (2x)
CTRL3-PNX5100	B05H (2x)
CTRL4-PNX5100	B05H (2x)
CTRL-DISP1	B05E (1x)
CTRL-DISP1	B05H (1x)
CTRL-DISP2	B05E (1x)
CTRL-DISP2	B05H (1x)
CTRL-DISP3	B05E (1x)
CTRL-DISP3	B05H (1x)
CTRL-DISP4	B05E (1x)
CTRL-DISP4	B05H (1x)
CVBS4	B02B (1x)
CVBS4	B04K (1x)
CVBS-OUT-SC1	B08A (2x)
CVBS-TER-OUT	B02B (1x)
CVBS-TER-OUT	B08A (1x)
DDC-SCL	B04H (1x)
DDC-SCL	B08G (1x)
DDC-SDA	B04H (1x)
DDC-SDA	B08G (1x)
DDR2-A0	B04G (4x)
DDR2-A1	B04G (4x)
DDR2-A10	B04G (4x)
DDR2-A11	B04G (4x)
DDR2-A12	B04G (4x)
DDR2-A2	B04G (4x)
DDR2-A3	B04G (4x)
DDR2-A4	B04G (4x)
DDR2-A5	B04G (4x)
DDR2-A6	B04G (4x)
DDR2-A7	B04G (4x)
DDR2-A8	B04G (4x)
DDR2-A9	B04G (4x)
DDR2-BA0	B04G (4x)
DDR2-BA1	B04G (4x)
DDR2-CAS	B04G (4x)
DDR2-CKE	B04G (4x)
DDR2-CLK_N	B04G (4x)
DDR2-CLK_P	B04G (4x)
DDR2-CS	B04G (4x)
DDR2-D0	B04G (2x)
DDR2-D1	B04G (2x)
DDR2-D10	B04G (2x)
DDR2-D11	B04G (2x)
DDR2-D12	B04G (2x)
DDR2-D13	B04G (2x)
DDR2-D14	B04G (2x)
DDR2-D15	B04G (2x)
DDR2-D16	B04G (2x)
DDR2-D17	B04G (2x)
DDR2-D18	B04G (2x)
DDR2-D19	B04G (2x)
DDR2-D2	B04G (2x)
DDR2-D20	B04G (2x)
DDR2-D21	B04G (2x)
DDR2-D22	B04G (2x)
DDR2-D23	B04G (2x)
DDR2-D24	B04G (2x)
DDR2-D25	B04G (2x)
DDR2-D26	B04G (2x)
DDR2-D27	B04G (2x)
DDR2-D28	B04G (2x)
DDR2-D29	B04G (2x)
DDR2-D3	B04G (2x)
DDR2-D30	B04G (2x)
DDR2-D31	B04G (2x)
DDR2-D4	B04G (2x)
DDR2-D5	B04G (2x)
DDR2-D6	B04G (2x)
DDR2-D7	B04G (2x)
DDR2-D8	B04G (2x)
DDR2-D9	B04G (2x)
DDR2-DQM0	B04G (2x)
DDR2-DQM1	B04G (2x)
DDR2-DQM2	B04G (2x)
DDR2-DQM3	B04G (2x)
DDR2-DQS0_N	B04G (2x)
DDR2-DQS0_P	B04G (2x)
DDR2-DQS1_N	B04G (2x)
DDR2-DQS1_P	B04G (2x)
DDR2-DQS2_N	B04G (2x)
DDR2-DQS2_P	B04G (2x)
DDR2-DQS3_N	B04G (2x)
DDR2-DQS3_P	B04G (2x)
DDR2-ODT	B04G (4x)
DDR2-RAS	B04G (4x)
DDR2-VREF-CTRL	B04G (2x)
DDR2-VREF-DDR	B04G (3x)
DDR2-WE	B04G (4x)
DETECT1	B04A (3x)
DETECT-12V	B01B (1x)
DETECT-12V	B04A (1x)
DETECT2	B04A (3x)
DIF-N	B02B (1x)
DIF-N	B02C (1x)
DIF-P	B02B (1x)
DIF-P	B02C (1x)
DV-B4_UV0	B04O (1x)
DV-B4_UV0	B05B (1x)
DV-B5_UV1	B04O (1x)
DV-B5_UV1	B05B (1x)
DV-B6_Y0	B04O (1x)
DV-B6_Y0	B05B (1x)
DV-B7_Y1	B04O (1x)
DV-B7_Y1	B05B (1x)
DV-CLK	B04O (1x)
DV-CLK	B05B (1x)
DV-FF_DE	B04O (1x)
DV-FF_DE	B05B (1x)
DV-G0_UV2	B04O (1x)
DV-G0_UV2	B05B (1x)
DV-G1_UV3	B04O (1x)
DV-G1_UV3	B05B (1x)
DV-G2_UV4	B04O (1x)
DV-G2_UV4	B05B (1x)
DV-G3_UV5	B04O (1x)
DV-G3_UV5	B05B (1x)
DV-G4_UV6	B04O (1x)
DV-G4_UV6	B05B (1x)
DV-G5_UV7	B04O (1x)
DV-G5_UV7	B05B (1x)
DV-G6_UV8	B04O (1x)
DV-G6_UV8	B05B (1x)
DV-G7_UV9	B04O (1x)
DV-G7_UV9	B05B (1x)
DV-HS	B04O (1x)
DV-HS	B05B (1x)
DV-R0_Y2	B04O (1x)
DV-R0_Y2	B05B (1x)
DV-R1_Y3	B04O (1x)
DV-R1_Y3	B05B (1x)
DV-R2_Y4	B04O (1x)
DV-R2_Y4	B05B (1x)
DV-R3_Y5	B04O (1x)
DV-R3_Y5	B05B (1x)
DV-R4_Y6	B04O (1x)
DV-R4_Y6	B05B (1x)
DV-R5_Y7	B04O (1x)
DV-R5_Y7	B05B (1x)
DV-R6_Y8	B04O (1x)
DV-R6_Y8	B05B (1x)
DV-R7_Y9	B04O (1x)
DV-R7_Y9	B05B (1x)
DV-VS	B04O (1x)
DV-VS	B05B (1x)
EA	B04A (2x)
EJTAG-DETECT	B04A (2x)
EJTAG-DETECT	B08D (1x)
EJTAG-PNX5100-TCK	B05F (1x)
EJTAG-PNX5100-TCK	B05I (1x)
EJTAG-PNX5100-TDI	B05F (1x)
EJTAG-PNX5100-TDI	B05I (1x)
EJTAG-PNX5100-TDO	B05F (1x)
EJTAG-PNX5100-TDO	B05I (1x)
EJTAG-PNX5100-TMS	B05F (1x)
EJTAG-PNX5100-TMS	B05I (1x)
EJTAG-PNX5100-TRSTn	B05F (1x)
EJTAG-PNX5100-TRSTn	B05I (1x)
EJTAG-TCK	B04E (1x)
EJTAG-TCK	B08D (1x)
EJTAG-TDI	B04E (1x)
EJTAG-TDI	B08D (3x)
EJTAG-TDO	B04E (1x)
EJTAG-TDO	B08D (1x)
EJTAG-TMS	B04E (1x)
EJTAG-TMS	B08D (2x)
EJTAG-TRSTN	B04E (1x)
EJTAG-TRSTN	B08D (2x)
EMI-A1	B03A (1x)
EMI-A1	B03B (2x)
EMI-A10	B03A (1x)
EMI-A10	B03B (2x)
EMI-A11	B03B (2x)
EMI-A12	B03A (1x)
EMI-A12	B03B (2x)
EMI-A13	B03A (1x)
EMI-A13	B03B (2x)
EMI-A14	B03A (2x)
EMI-A14	B03B (2x)
EMI-A15	B03A (1x)
EMI-A15	B03B (2x)
EMI-A16	B03B (2x)
EMI-A17	B03B (2x)
EMI-A18	B03B (2x)
EMI-A19	B03B (2x)
EMI-A2	B03A (1x)
EMI-A2	B03B (2x)
EMI-A20	B03B (2x)
EMI-A21	B03B (2x)
EMI-A22	B03B (2x)
EMI-A3	B03A (1x)
EMI-A3	B03B (2x)
EMI-A4	B03A (1x)
EMI-A4	B03B (2x)
EMI-A5	B03A (1x)
EMI-A5	B03B (2x)
EMI-A6	B03A (1x)
EMI-A6	B03B (2x)
EMI-A7	B03A (1x)
EMI-A7	B03B (2x)
EMI-A8	B03A (1x)
EMI-A8	B03B (2x)
EMI-A9	B03A (1x)
EMI-A9	B03B (2x)
EMI-D0	B03B (2x)
EMI-D1	B03B (2x)
EMI-D10	B03B (2x)
EMI-D11	B03B (2x)
EMI-D12	B03B (2x)
EMI-D13	B03B (2x)
EMI-D14	B03B (2x)
EMI-D15	B03B (2x)
EMI-D2	B03B (2x)
EMI-D3	B03B (2x)
EMI-D4	B03B (2x)
EMI-D5	B03B (2x)
EMI-D6	B03B (2x)
EMI-D7	B03B (2x)
EMI-D8	B03B (2x)
EMI-D9	B03B (2x)
EMI-FLASH-CSn	B03B (3x)
EMI-OEn	B03B (3x)
EMI-RB-WAIT	B03B (1x)
EMI-WRn	B03B (2x)
ENABLE-1V2	B01A (1x)
ENABLE-1V2	B01C (1x)
ENABLE-1V2	B04A (2x)
ENABLE-3V3	B01A (1x)
ENABLE-3V3	B01C (1x)
ENABLE-3V3	B04A (2x)
ETH-RDM	B03F (1x)
ETH-RDM	B09B (1x)
ETH-RDP	B03F (1x)
ETH-RDP	B09B (1x)
ETH-TDM	B03F (1x)
ETH-TDM	B09B (1x)
ETH-TDP	B03F (1x)
ETH-TDP	B09B (1x)
FAN1-DRV	B05G (2x)
FAN1-OUT	B05G (2x)
FE-CLK	B02A (1x)
FE-CLK	B02C (1x)
FE-CLK	B04N (1x)
FE-DATA0	B02A (1x)
FE-DATA0	B02C (2x)
FE-DATA0	B04N (1x)
FE-DATA1	B02A (1x)
FE-DATA1	B02C (2x)
FE-DATA1	B04N (1x)
FE-DATA2	B02A (1x)
FE-DATA2	B02C (2x)
FE-DATA2	B04N (1x)
FE-DATA3	B02A (1x)
FE-DATA3	B02C (2x)
FE-DATA3	B04N (1x)
FE-DATA4	B02A (1x)
FE-DATA4	B02C (2x)
FE-DATA4	B04N (1x)
FE-DATA5	B02A (1x)
FE-DATA5	B02C (2x)
FE-DATA5	B04N (1x)
FE-DATA6	B02A (1x)
FE-DATA6	B02C (2x)
FE-DATA6	B04N (1x)
FE-DATA7	B02A (1x)
FE-DATA7	B02C (2x)
FE-DATA7	B04N (1x)
FE-ERR	B02A (1x)
FE-ERR	B04N (2x)
FE-SOP	B02A (1x)
FE-SOP	B02C (1x)
FE-SOP	B04N (1x)
FE-VALID	B02A (1x)
FE-VALID	B02C (1x)
FE-VALID	B04N (1x)
FRONT-C	B04K (1x)
FRONT-Y_CVBS	B04K (1x)
FRONT-Y_CVBS	B08B (1x)
GND-SIG	B01A (14x)
GND-SIG1	B01C (14x)
G-VGA	B04K (1x)
G-VGA	B08A (1x)
G-VGA	B08B (1x)
HOT-PLUG	B04H (1x)
HOT-PLUG	B08F (3x)
H-SYNC-VGA	B04K (1x)
H-SYNC-VGA	B08B (1x)
IF-FILTN1	B02B (2x)
IF-FILTN2	B02B (2x)
IF-FILTN3	B02B (2x)
IF-FILTP1	B02B (2x)
IF-FILTP2	B02B (2x)
IF-FILTP3	B02B (2x)
IF-N	B02A (1x)
IF-N	B02B (1x)
IF-N	B02C (1x)
IF-N	B04K (1x)
IF-P	B02A (1x)
IF-P	B02B (1x)
IF-P	B02C (1x)
IF-P	B04K (1x)
IRQ-CA	B03H (2x)
IRQ-CA	B04E (2x)
IRQ-PCI	B04E (2x)
IRQ-PCI	B09A (2x)
IRQ-PCI	B09B (1x)
JTAG-TCK-ST	B03A (2x)
JTAG-TCK-ST	B03G (1x)
JTAG-TCK-TDA10023	B02C (1x)
JTAG-TCK-TDA10048	B02A (1x)
JTAG-TDI-ST	B03A (2x)
JTAG-TDI-ST	B03G (1x)
JTAG-TDI-TDA10023	B02C (1x)
JTAG-TDI-TDA10048	B02A (1x)
JTAG-TDO-ST	B03A (2x)
JTAG-TDO-ST	B03G (1x)
JTAG-TDO-TDA10023	B02C (1x)
JTAG-TDO-TDA10048	B02A (1x)
JTAG-TMS-ST	B03A (2x)
JTAG-TMS-ST	B03G (1x)
JTAG-TMS-TDA10023	B02C (1x)
JTAG-TMS-TDA10048	B02A (1x)
JTAG-TRSTn-ST	B03A (2x)
JTAG-TRSTn-ST	B03G (1x)
JTAG-TRST-TDA10023	B02C (1x)
JTAG-TRST-TDA10048	B02A (1x)
KEYBOARD	B01D (1x)
KEYBOARD	B04A (2x)
LCD-PWR-ON	B05H (2x)
LED1	B01D (1x)
LED1	B04A (2x)
LED2	B01D (1x)
LED2	B04A (2x)
LIGHT-SENSOR	B01D (1x)
LIGHT-SENSOR	B04A (1x)

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SSB: SRP List Part 2

Netname	Diagram
LMI-A(0)	B03C (3x)
LMI-A(1)	B03C (3x)
LMI-A(10)	B03C (3x)
LMI-A(11)	B03C (3x)
LMI-A(12)	B03C (3x)
LMI-A(2)	B03C (3x)
LMI-A(3)	B03C (3x)
LMI-A(4)	B03C (3x)
LMI-A(5)	B03C (3x)
LMI-A(6)	B03C (3x)
LMI-A(7)	B03C (3x)
LMI-A(8)	B03C (3x)
LMI-A(9)	B03C (3x)
LMI-BA0	B03C (3x)
LMI-BA1	B03C (3x)
LMI-CASnot	B03C (3x)
LMI-CLK	B03C (4x)
LMI-CLKEN	B03C (3x)
LMI-CLKnot	B03C (4x)
LMI-CSnot	B03C (3x)
LMI-D(0)	B03C (2x)
LMI-D(1)	B03C (2x)
LMI-D(10)	B03C (2x)
LMI-D(11)	B03C (2x)
LMI-D(12)	B03C (2x)
LMI-D(13)	B03C (2x)
LMI-D(14)	B03C (2x)
LMI-D(15)	B03C (2x)
LMI-D(16)	B03C (2x)
LMI-D(17)	B03C (2x)
LMI-D(18)	B03C (2x)
LMI-D(19)	B03C (2x)
LMI-D(2)	B03C (2x)
LMI-D(20)	B03C (2x)
LMI-D(21)	B03C (2x)
LMI-D(22)	B03C (2x)
LMI-D(23)	B03C (2x)
LMI-D(24)	B03C (2x)
LMI-D(25)	B03C (2x)
LMI-D(26)	B03C (2x)
LMI-D(27)	B03C (2x)
LMI-D(28)	B03C (2x)
LMI-D(29)	B03C (2x)
LMI-D(3)	B03C (2x)
LMI-D(30)	B03C (2x)
LMI-D(31)	B03C (2x)
LMI-D(4)	B03C (2x)
LMI-D(5)	B03C (2x)
LMI-D(6)	B03C (2x)
LMI-D(7)	B03C (2x)
LMI-D(8)	B03C (2x)
LMI-D(9)	B03C (2x)
LMI-DQM0	B03C (2x)
LMI-DQM1	B03C (2x)
LMI-DQM2	B03C (2x)
LMI-DQM3	B03C (2x)
LMI-DQS0	B03C (2x)
LMI-DQS1	B03C (2x)
LMI-DQS2	B03C (2x)
LMI-DQS3	B03C (2x)
LMI-RASnot	B03C (3x)
LMI-VREF	B03C (2x)
LMI-VREF2-ST	B03C (2x)
LMI-VREF-ST	B03C (2x)
LMI-WEnot	B03C (3x)
MDO0	B03H (4x)
MDO1	B03H (4x)
MDO2	B03H (4x)
MDO3	B03H (4x)
MDO4	B03H (4x)
MDO5	B03H (4x)
MDO6	B03H (4x)
MDO7	B03H (4x)
MOCLK_VS2	B03H (4x)
MOSTRT	B03H (4x)
MOVAL	B03H (4x)
MPEG-DDC-SCLD	B08G (1x)
MPEG-DDC-SDAD	B08G (1x)
MPEG-TX0-	B03D (1x)
MPEG-TX0-	B08G (1x)
MPEG-TX0+	B03D (1x)
MPEG-TX0+	B08G (1x)
MPEG-TX1-	B03D (1x)
MPEG-TX1-	B08G (1x)
MPEG-TX1+	B03D (1x)
MPEG-TX1+	B08G (1x)
MPEG-TX2-	B03D (1x)
MPEG-TX2-	B08G (1x)
MPEG-TX2+	B03D (1x)
MPEG-TX2+	B08G (1x)
MPEG-TXC-	B03D (1x)
MPEG-TXC-	B08G (1x)
MPEG-TXC+	B03D (1x)
MPEG-TXC+	B08G (1x)
NAND-AD(0)	B04Q (2x)
NAND-AD(1)	B04Q (2x)
NAND-AD(2)	B04Q (2x)
NAND-AD(3)	B04Q (2x)
NAND-AD(4)	B04Q (2x)
NAND-AD(5)	B04Q (2x)
NAND-AD(6)	B04Q (2x)
NAND-AD(7)	B04Q (2x)
NAND-ALE	B04Q (2x)
NAND-CLE	B04Q (2x)
NAND-REn	B04Q (2x)
NAND-WEn	B04Q (2x)
P0.4	B04A (2x)
P0.7	B04A (2x)
P2.0	B04A (2x)
P2.2	B04A (2x)
PARX-DDC-SCL	B08F (1x)
PARX-DDC-SCL	B08G (1x)
PARX-DDC-SDA	B08F (1x)
PARX-DDC-SDA	B08G (1x)
PBRX-DDC-SCL	B08F (1x)
PBRX-DDC-SCL	B08G (1x)
PBRX-DDC-SDA	B08F (1x)
PBRX-DDC-SDA	B08G (1x)
PCEC-HDMI	B08F (4x)
PCI-AD0	B04F (1x)
PCI-AD0	B04Q (1x)
PCI-AD0	B05G (1x)
PCI-AD0	B09A (1x)
PCI-AD0	B09B (1x)
PCI-AD0	B09C (1x)
PCI-AD1	B04F (1x)
PCI-AD1	B04Q (1x)
PCI-AD1	B05G (1x)
PCI-AD1	B09A (1x)
PCI-AD1	B09B (1x)
PCI-AD1	B09C (1x)
PCI-AD10	B04F (1x)
PCI-AD10	B05G (1x)
PCI-AD10	B09A (1x)
PCI-AD10	B09B (1x)
PCI-AD10	B09C (1x)
PCI-AD11	B04F (1x)
PCI-AD11	B05G (1x)
PCI-AD11	B09A (1x)
PCI-AD11	B09B (1x)
PCI-AD11	B09C (1x)
PCI-AD12	B04F (1x)
PCI-AD12	B05G (1x)
PCI-AD12	B09A (1x)
PCI-AD12	B09B (1x)
PCI-AD12	B09C (1x)
PCI-AD13	B04F (1x)
PCI-AD13	B05G (1x)
PCI-AD13	B09A (1x)
PCI-AD13	B09B (1x)
PCI-AD13	B09C (1x)
PCI-AD14	B04F (1x)
PCI-AD14	B05G (1x)
PCI-AD14	B09A (1x)
PCI-AD14	B09B (1x)
PCI-AD14	B09C (1x)
PCI-AD15	B04F (1x)
PCI-AD15	B05G (1x)
PCI-AD15	B09A (1x)
PCI-AD15	B09B (1x)
PCI-AD16	B04F (1x)
PCI-AD16	B05G (1x)
PCI-AD16	B09A (1x)
PCI-AD16	B09B (1x)
PCI-AD16	B09C (1x)
PCI-AD17	B04F (1x)
PCI-AD17	B05G (1x)
PCI-AD17	B09A (1x)
PCI-AD17	B09B (1x)
PCI-AD17	B09C (1x)
PCI-AD18	B04F (1x)
PCI-AD18	B05G (1x)
PCI-AD18	B09A (1x)
PCI-AD18	B09B (1x)
PCI-AD18	B09C (1x)
PCI-AD19	B04F (1x)
PCI-AD19	B05G (1x)
PCI-AD19	B09A (1x)
PCI-AD19	B09B (1x)
PCI-AD19	B09C (1x)
PCI-AD2	B04F (1x)
PCI-AD2	B05G (1x)
PCI-AD2	B09A (1x)
PCI-AD2	B09B (1x)
PCI-AD2	B09C (1x)
PCI-AD20	B04F (1x)
PCI-AD20	B05G (1x)
PCI-AD20	B09A (1x)
PCI-AD20	B09B (1x)
PCI-AD21	B04F (1x)
PCI-AD21	B05G (1x)
PCI-AD21	B09A (1x)
PCI-AD21	B09B (1x)
PCI-AD22	B04F (1x)
PCI-AD22	B05G (1x)
PCI-AD22	B09A (2x)
PCI-AD22	B09B (1x)
PCI-AD22	B09C (1x)
PCI-AD23	B04F (1x)
PCI-AD23	B05G (1x)
PCI-AD23	B09A (1x)
PCI-AD23	B09B (2x)
PCI-AD23	B09C (1x)
PCI-AD24	B04F (2x)
PCI-AD24	B04Q (1x)
PCI-AD24	B05G (1x)
PCI-AD24	B09A (1x)
PCI-AD24	B09B (1x)
PCI-AD24	B09C (1x)
PCI-AD25	B04F (1x)
PCI-AD25	B04Q (1x)
PCI-AD25	B05G (2x)
PCI-AD25	B09A (1x)
PCI-AD25	B09B (1x)
PCI-AD25	B09C (1x)
PCI-AD26	B04F (1x)
PCI-AD26	B04Q (1x)
PCI-AD26	B05G (1x)
PCI-AD26	B09A (1x)
PCI-AD26	B09B (1x)
PCI-AD26	B09C (1x)
PCI-AD27	B04F (1x)
PCI-AD27	B04Q (1x)
PCI-AD27	B05G (1x)
PCI-AD27	B09A (1x)
PCI-AD27	B09B (1x)
PCI-AD27	B09C (1x)
PCI-AD28	B04F (1x)
PCI-AD28	B04Q (1x)
PCI-AD28	B05G (1x)
PCI-AD28	B09A (1x)
PCI-AD28	B09B (1x)
PCI-AD28	B09C (1x)
PCI-AD29	B04F (1x)
PCI-AD29	B04Q (1x)
PCI-AD29	B05G (1x)
PCI-AD29	B09A (1x)
PCI-AD29	B09B (1x)
PCI-AD29	B09C (1x)
PCI-AD3	B04F (1x)
PCI-AD3	B05G (1x)
PCI-AD3	B09A (1x)
PCI-AD3	B09B (1x)
PCI-AD3	B09C (1x)
PCI-AD30	B04F (1x)
PCI-AD30	B04Q (1x)
PCI-AD30	B05G (1x)
PCI-AD30	B09A (1x)
PCI-AD30	B09B (1x)
PCI-AD30	B09C (1x)
PCI-AD31	B04F (1x)
PCI-AD31	B04Q (1x)
PCI-AD31	B05G (1x)
PCI-AD31	B09A (1x)
PCI-AD31	B09B (1x)
PCI-AD31	B09C (1x)
PCI-AD4	B04F (1x)
PCI-AD4	B05G (1x)
PCI-AD4	B09A (1x)
PCI-AD4	B09B (1x)
PCI-AD4	B09C (1x)
PCI-AD5	B04F (1x)
PCI-AD5	B05G (1x)
PCI-AD5	B09A (1x)
PCI-AD5	B09B (1x)
PCI-AD5	B09C (1x)
PCI-AD6	B04F (1x)
PCI-AD6	B05G (1x)
PCI-AD6	B09A (1x)
PCI-AD6	B09B (1x)
PCI-AD6	B09C (1x)
PCI-AD7	B04F (1x)
PCI-AD7	B05G (1x)
PCI-AD7	B09A (1x)
PCI-AD7	B09B (1x)
PCI-AD7	B09C (1x)
PCI-AD8	B04F (1x)
PCI-AD8	B05G (1x)
PCI-AD8	B09A (1x)
PCI-AD8	B09B (1x)
PCI-AD8	B09C (1x)
PCI-AD9	B04F (1x)
PCI-AD9	B05G (1x)
PCI-AD9	B09A (1x)
PCI-AD9	B09B (1x)
PCI-AD9	B09C (1x)
PCI-CBE0	B04F (1x)
PCI-CBE0	B05G (1x)
PCI-CBE0	B09A (1x)
PCI-CBE0	B09B (1x)
PCI-CBE1	B04F (1x)
PCI-CBE1	B04Q (1x)
PCI-CBE1	B05G (1x)
PCI-CBE1	B09A (1x)
PCI-CBE1	B09B (1x)
PCI-CBE1	B09C (1x)
PCI-CBE2	B04F (1x)
PCI-CBE2	B04Q (1x)
PCI-CBE2	B05G (1x)
PCI-CBE2	B09A (1x)
PCI-CBE2	B09B (1x)
PCI-CBE2	B09C (1x)
PCI-CBE3	B04F (1x)
PCI-CBE3	B05G (1x)
PCI-CBE3	B09A (1x)
PCI-CBE3	B09B (1x)
PCI-CLK-ETHERNET	B04E (2x)
PCI-CLK-OUT	B04E (3x)
PCI-CLK-PNX5100	B04E (2x)
PCI-CLK-PNX5100	B05G (1x)
PCI-CLK-PNX8535	B04E (2x)
PCI-CLK-PNX8535	B04F (1x)
PCI-CLK-USB20_ETH	B04E (2x)
PCI-CLK-USB20_ETH	B09A (1x)
PCI-CLK-USB20_ETH	B09B (1x)
PCI-DEVSEL	B04F (2x)
PCI-DEVSEL	B05G (1x)
PCI-DEVSEL	B09A (1x)
PCI-DEVSEL	B09B (1x)
PCI-FRAME	B04F (2x)
PCI-FRAME	B05G (1x)
PCI-FRAME	B09A (1x)
PCI-FRAME	B09B (1x)
PCI-GNT	B04F (2x)
PCI-GNT-B	B04F (2x)
PCI-GNT-ETHERNET	B05G (1x)
PCI-GNT-ETHERNET	B09B (2x)
PCI-GNT-PNX85XX	B04F (1x)
PCI-GNT-PNX85XX	B05G (1x)
PCI-GNT-PNX85XX	B09B (1x)
PCI-GNT-USB20	B04F (1x)
PCI-GNT-USB20	B05G (1x)
PCI-GNT-USB20	B09A (2x)
PCI-IRDY	B04F (2x)
PCI-IRDY	B05G (1x)
PCI-IRDY	B09A (1x)
PCI-IRDY	B09B (1x)
PCI-PAR	B04F (1x)
PCI-PAR	B05G (1x)
PCI-PAR	B09A (1x)
PCI-PAR	B09B (1x)
PCI-PERR	B04F (2x)
PCI-PERR	B05G (1x)
PCI-PERR	B09A (1x)
PCI-PERR	B09B (1x)
PCI-REQ	B04F (2x)
PCI-REQ-B	B04F (2x)
PCI-REQ-ETHERNET	B05G (1x)
PCI-REQ-ETHERNET	B09B (2x)
PCI-REQ-PNX85XX	B04F (1x)
PCI-REQ-PNX85XX	B05G (1x)
PCI-REQ-PNX85XX	B09B (1x)
PCI-REQ-USB20	B04F (1x)
PCI-REQ-USB20	B05G (1x)
PCI-REQ-USB20	B09A (2x)
PCI-SERR	B04F (2x)
PCI-SERR	B05G (1x)
PCI-SERR	B09A (1x)
PCI-SERR	B09B (1x)
PCI-STOP	B04F (2x)
PCI-STOP	B05G (1x)
PCI-STOP	B09A (1x)
PCI-STOP	B09B (1x)
PCI-TRDY	B04F (2x)
PCI-TRDY	B05G (1x)
PCI-TRDY	B09A (1x)
PCI-TRDY	B09B (1x)
PCMCIA-A0	B03H (1x)
PCMCIA-A0	B09C (1x)
PCMCIA-A1	B03H (1x)
PCMCIA-A1	B09C (1x)
PCMCIA-A10	B03H (1x)
PCMCIA-A10	B09C (1x)
PCMCIA-A11	B03H (1x)
PCMCIA-A11	B09C (1x)
PCMCIA-A12	B03H (1x)
PCMCIA-A12	B09C (1x)
PCMCIA-A13	B03H (1x)
PCMCIA-A13	B09C (1x)
PCMCIA-A14	B03H (1x)
PCMCIA-A14	B09C (1x)
PCMCIA-A2	B03H (1x)
PCMCIA-A2	B09C (1x)
PCMCIA-A3	B03H (1x)
PCMCIA-A3	B09C (1x)
PCMCIA-A4	B03H (1x)
PCMCIA-A4	B09C (1x)
PCMCIA-A5	B03H (1x)
PCMCIA-A5	B09C (1x)
PCMCIA-A6	B03H (1x)
PCMCIA-A6	B09C (1x)
PCMCIA-A7	B03H (1x)
PCMCIA-A7	B09C (1x)
PCMCIA-A8	B03H (1x)
PCMCIA-A8	B09C (1x)
PCMCIA-A9	B03H (1x)
PCMCIA-A9	B09C (1x)
PCMCIA-D0	B03H (1x)
PCMCIA-D0	B09C (1x)
PCMCIA-D1	B03H (1x)
PCMCIA-D1	B09C (1x)
PCMCIA-D2	B03H (1x)
PCMCIA-D2	B09C (1x)
PCMCIA-D3	B03H (1x)
PCMCIA-D3	B09C (1x)
PCMCIA-D4	B03H (1x)
PCMCIA-D4	B09C (1x)
PCMCIA-D5	B03H (1x)
PCMCIA-D5	B09C (1x)
PCMCIA-D6	B03H (1x)
PCMCIA-D6	B09C (1x)
PCMCIA-D7	B03H (1x)
PCMCIA-D7	B09C (1x)
PCMCIA-VCC-VPP	B03H (4x)
PCMOUT2	B03A (1x)
PCMOUT2	B03D (1x)
PCMOUT3	B03A (1x)
PCMOUT3	B03D (1x)
PCMOUT4	B03A (1x)
PCMOUT4	B03D (1x)
PCRX-DDC-SCL	B08F (1x)
PCRX-DDC-SCL	B08G (1x)
PCRX-DDC-SDA	B08F (1x)
PCRX-DDC-SDA	B08G (1x)
PNX5100-DDR2-A0	B05A (3x)
PNX5100-DDR2-A1	B05A (3x)
PNX5100-DDR2-A10	B05A (3x)
PNX5100-DDR2-A11	B05A (3x)
PNX5100-DDR2-A12	B05A (3x)
PNX5100-DDR2-A2	B05A (3x)
PNX5100-DDR2-A3	B05A (3x)
PNX5100-DDR2-A4	B05A (3x)
PNX5100-DDR2-A5	B05A (3x)
PNX5100-DDR2-A6	B05A (3x)
PNX5100-DDR2-A7	B05A (3x)
PNX5100-DDR2-A8	B05A (3x)
PNX5100-DDR2-A9	B05A (3x)
PNX5100-DDR2-BA0	B05A (3x)
PNX5100-DDR2-BA1	B05A (3x)
PNX5100-DDR2-CAS	B05A (3x)
PNX5100-DDR2-CKE	B05A (3x)
PNX5100-DDR2-CLK_N	B05A (3x)
PNX5100-DDR2-CLK_P	B05A (3x)
PNX5100-DDR2-CS	B05A (3x)
PNX5100-DDR2-D0	B05A (2x)
PNX5100-DDR2-D1	B05A (2x)
PNX5100-DDR2-D10	B05A (2x)
PNX5100-DDR2-D11	B05A (2x)
PNX5100-DDR2-D12	B05A (2x)
PNX5100-DDR2-D13	B05A (2x)
PNX5100-DDR2-D14	B05A (2x)
PNX5100-DDR2-D15	B05A (2x)
PNX5100-DDR2-D16	B05A (2x)
PNX5100-DDR2-D17	B05A (2x)
PNX5100-DDR2-D18	B05A (2x)
PNX5100-DDR2-D19	B05A (2x)
PNX5100-DDR2-D2	B05A (2x)
PNX5100-DDR2-D20	B05A (2x)
PNX5100-DDR2-D21	B05A (2x)
PNX5100-DDR2-D22	B05A (2x)
PNX5100-DDR2-D23	B05A (2x)
PNX5100-DDR2-D24	B05A (2x)
PNX5100-DDR2-D25	B05A (2x)
PNX5100-DDR2-D26	B05A (2x)
PNX5100-DDR2-D27	B05A (2x)
PNX5100-DDR2-D28	B05A (2x)
PNX5100-DDR2-D29	B05A (2x)
PNX5100-DDR2-D3	B05A (2x)
PNX5100-DDR2-D30	B05A (2x)
PNX5100-DDR2-D31	B05A (2x)
PNX5100-DDR2-D4	B05A (2x)
PNX5100-DDR2-D5	B05A (2x)
PNX5100-DDR2-D6	B05A (2x)
PNX5100-DDR2-D7	B05A (2x)
PNX5100-DDR2-D8	B05A (2x)
PNX5100-DDR2-D9	B05A (2x)
PNX5100-DDR2-DQM0	B05A (2x)
PNX5100-DDR2-DQM1	B05A (2x)
PNX5100-DDR2-DQM2	B05A (2x)
PNX5100-DDR2-DQM3	B05A (2x)
PNX5100-DDR2-DQS0_N	B05A (2x)
PNX5100-DDR2-DQS0_P	B05A (2x)
PNX5100-DDR2-DQS1_N	B05A (2x)
PNX5100-DDR2-DQS1_P	B05A (2x)
PNX5100-DDR2-DQS2_N	B05A (2x)
PNX5100-DDR2-DQS2_P	B05A (2x)
PNX5100-DDR2-DQS3_N	B05A (2x)
PNX5100-DDR2-DQS3_P	B05A (2x)
PNX5100-DDR2-ODT	B05A (3x)
PNX5100-DDR2-RAS	B05A (3x)
PNX5100-DDR2-VREF-CTRL	B05A (2x)
PNX5100-DDR2-VREF-DDR	B05A (3x)
PNX5100-DDR2-WE	B05A (3x)
PNX5100-RST-OUT	B05F (1x)
PNX5100-RST-OUT	B05I (1x)
PROT-DC	B01A (1x)
PROT-DC	B01C (1x)
PSEN	B04A (2x)
RC	B01D (1x)
RC	B04A (2x)
RC	B05H (1x)
REGIMBEAU_CVBS-SWITCH	B04A (2x)
REGIMBEAU_CVBS-SWITCH	B08A (1x)
RESET-AUDIO	B04A (2x)
RESET-AUDIO	B04M (2x)
RESET-ETHERNET	B04A (2x)
RESET-ETHERNET	B09A (1x)
RESET-ETHERNET	B09B (2x)
RESET-FLASH-STn	B03B (3x)
RESET-NVM	B04A (2x)
RESET-NVM	B04C (1x)
RESET-PNX5100	B04A (2x)
RESET-PNX5100	B05F (1x)
RESET-ST7100	B03A (1x)
RESET-ST7100	B03B (1x)
RESET-ST7100	B04A (1x)
RESET-STBY	B04A (1x)
RESET-STBY	B04D (1x)
RESET-SYSTEM	B02A (1x)
RESET-SYSTEM	B02C (1x)
RESET-SYSTEM	B04A (2x)
RESET-SYSTEM	B04E (2x)
RESET-SYSTEM	B05H (1x)
RESET-SYSTEM	B08G (1x)
RESET-USB20	B09A (2x)
RREF-PNX8541	B04H (1x)
RREF-PNX8541	B04P (1x)
RSETIN-ST7100	B03A (2x)
RST-TARGETn	B03G (2x)
R-VGA	B04K (1x)
R-VGA	B08A (1x)
R-VGA	B08B (1x)
RX0-	B04H (1x)
RX0-	B08G (1x)
RX0+	B04H (1x)
RX0+	B08G (1x)
RX1-	B04H (1x)
RX1-	B08G (1x)
RX1+	B04H (1x)
RX1+	B08G (1x)
RX2-	B04H (1x)
RX2-	B08G (1x)
RX2+	B04H (1x)
RX2+	B08G (1x)
RXC-	B04H (1x)
RXC-	B08G (1x)
RXC+	B04H (1x)
RXC+	B08G (1x)
RXD-ASC2	B03A (1x)
RXD-ASC2	B03G (1x)
RXD-MIPS	B04E (1x)
RXD-MIPS	B08D (1x)
RXD-UP	B04A (2x)
RXD-UP	B08D (1x)
SCL1	B04E (2x)
SCL2	B04E (2x)
SCL3	B04E (2x)
SCL-DISP	B01B (1x)
SCL-DISP	B05E (2x)
SCL-DISP	B05F (1x)
SCL-DISP	B05G (3x)
SCL-SSB	B02A (1x)
SCL-SSB	B02B (2x)
SCL-SSB	B02C (1x)
SCL-SSB	B04E (2x)
SCL-SSB	B05E (1x)
SCL-SSB	B05F (2x)
SCL-SSB	B08D (1x)
SCL-SSB	B08G (1x)
SCL-ST	B03A (1x)
SCL-ST	B05E (1x)
SCL-TUNER	B02A (1x)
SCL-TUNER	B02B (2x)
SCL-TUNER	B02C (1x)
SCL-UP-MIPS	B04A (2x)
SCL-UP-MIPS	B04C (1x)
SCL-UP-MIPS	B04E (2x)
SDA1	B04E (2x)
SDA2	B04E (2x)
SDA3	B04E (2x)
SDA-DISP	B01B (1x)
SDA-DISP	B05E (2x)
SDA-DISP	B05F (1x)
SDA-DISP	B05G (3x)
SDA-SSB	B02A (1x)
SDA-SSB	B02B (2x)
SDA-SSB	B02C (1x)
SDA-SSB	B04E (2x)
SDA-SSB	B05E (1x)
SDA-SSB	B05F (2x)
SDA-SSB	B08D (1x)
SDA-SSB	B08G (1x)
SDA-ST	B03A (1x)
SDA-ST	B05E (1x)
SDA-TUNER	B02A (1x)
SDA-TUNER	B02B (2x)
SDA-TUNER	B02C (1x)
SDA-UP-MIPS	B04A (2x)
SDA-UP-MIPS	B04C (1x)
SDA-UP-MIPS	B04E (2x)
SDM	B04A (3x)
SENSE+1V	B01B (4x)
SENSE+1V	B03E (2x)
SENSE+1V2-PNX5100	B01C (6x)
SENSE+1V2-PNX5100	B05C (2x)
SENSE+1V2-PNX8541	B01A (1x)
SENSE+1V2-PNX8541	B04P (1x)
SPDIF-OUT	B04L (1x)
SPDIF-OUT	B08A (1x)
SPI-CLK	B04A (2x)
SPI-CSB	B04A (2x)
SPI-PROG	B04A (3x)
SPI-SDI	B04A (3x)
SPI-SDO	B04A (2x)
SPI-WP	B04A (3x)
STANDBY	B01B (1x)
STANDBY	B04A (2x)
ST-DL-APP	B03A (1x)
ST-DL-APP	B04A (2x)
SUPPLY-FAULT	B01A (1x)
SUPPLY-FAULT	B04A (2x)
TACHO1	B05G (2x)
TACHO1-INV	B05G (2x)
TDA-IF-AGC	B02A (1x)
TDA-IF-AGC	B02B (1x)
TDA-IF-AGC	B02C (1x)
TMUCLK	B03A (2x)
TRIG-IN	B03A (2x)
TRIG-IN	B03G (1x)
TRIG-OUT	B03A (1x)
TRIG-OUT	B03G (1x)
TSI0-ST-CLK	B03A (2x)
TSI0-ST-D0	B03A (2x)
TSI0-ST-D1	B03A (2x)
TSI0-ST-D2	B03A (2x)
TSI0-ST-D3	B03A (2x)
TSI0-ST-D4	B03A (2x)
TSI0-ST-D5	B03A (2x)
TSI0-ST-D6	B03A (2x)
TSI0-ST-D7	B03A (2x)
TSI0-ST-STRT	B03A (1x)
TSI0-ST-VAL	B03A (2x)
TSI1-ST-CLK	B03A (2x)
TSI1-ST-D0	B03A (2x)
TSI1-ST-D1	B03A (2x)
TSI1-ST-D2	B03A (2x)
TSI1-ST-D3	B03A (2x)
TSI1-ST-D4	B03A (2x)
TSI1-ST-D5	B03A (2x)
TSI1-ST-D6	B03A (2x)
TSI1-ST-D7	B03A (2x)
TSI1-ST-VAL	B03A (2x)
TUN-AGC	B02A (1x)
TUN-AGC	B02B (3x)
TUN-AGC-MON	B02A (1x)
TUN-AGC-MON	B02B (1x)
TX1A-	B05E (3x)
TX1A+	B05E (3x)
TX1B-	B05E (3x)
TX1B+	B05E (3x)
TX1C-	B05E (3x)
TX1C+	B05E (3x)
TX1CLK-	B05E (3x)
TX1CLK+	B05E (3x)
TX1D-	B05E (3x)
TX1D+	B05E (3x)
TX1E-	B05E (3x)
TX1E+	B05E (3x)
TX2A-	B05E (3x)
TX2A+	B05E (3x)
TX2B-	B05E (3x)
TX2B+	B05E (3x)
TX2C-	B05E (3x)
TX2C+	B05E (3x)
TX2CLK-	B05E (3x)
TX2CLK+	B05E (3x)
TX2D-	B05E (3x)
TX2D+	B05E (3x)
TX2E-	B05E (3x)
TX2E+	B05E (3x)
TX3A-	B05E (3x)
TX3A+	B05E (3x)
TX3B-	B05E (3x)
TX3B+	B05E (3x)
TX3C-	B05E (3x)
TX3C+	B05E (3x)
TX3CLK-	B05E (3x)
TX3CLK+	B05E (3x)
TX3D-	B05E (3x)
TX3D+	B05E (3x)
TX3E-	B05E (3x)
TX3E+	B05E (3x)
TX4A-	B05E (3x)
TX4A+	B05E (3x)
TX4B-	B05E (3x)
TX4B+	B05E (3x)
TX4C-	B05E (3x)
TX4C+	B05E (3x)
TX4CLK-	B05E (3x)
TX4CLK+	B05E (3x)
TX4D-	B05E (3x)
TX4D+	B05E (3x)
TX4E-	B05E (3x)
TX4E+	B05E (3x)
TXD-ASC2	B03A (1x)
TXD-ASC2	B03G (1x)
TXD-MIPS	B04E (1x)
TXD-MIPS	B08D (1x)
TXD-UP	B04A (2x)
TXD-UP	B08D (1x)
USB20-2-DM	B03F (1x)
USB20-2-DM	B09A (2x)
USB20-2-DP	B03F (1x)
USB20-2-DP	B09A (2x)
USB20-OC1	B09A (3x)
USB20-OC2	B09A (3x)
USB-OC	B03F (1x)
USB-OC	B09A (1x)
V_LVC04	B03A (5x)
V1	B02B (3x)
VDDA-ADC	B04P (2x)
VDDA-AUDIO	B04L (2x)
VDDA-AUDIO	B04P (2x)
VDDA-DAC	B04P (2x)
VDDA-LVDS	B04O (1x)
VDDA-LVDS	B04P (2x)
VDDE-2V5	B03E (7x)
VDDE-3V3	B03E (3x)
VSW	B01A (1x)
VSW	B01B (1x)
V-SYNC-VGA	B04K (1x)
V-SYNC-VGA	B08B (1x)
VTT-TERM-DDR	B04G (2x)
WC-EEPROM-PNX5100	B04E (1x)
WC-EEPROM-PNX5100	B05F (2x)
WC-EEPROM-PNX5100	B08F (1x)
WP-FLASH-ST	B03A (1x)
WP-FLASH-ST	B03B (1x)
WP-NANDFLASH	B04A (2x)
WP-NANDFLASH	B04Q (2x)
WRITE-PROT	B08F (4x)
XIO-ACK	B04F (1x)
XIO-ACK	B04Q (2x)
XIO-SEL-NAND	B04F (1x)
XIO-SEL-NAND	B04Q (2x)
Y_CVBS-MON-OUT	B04K (1x)
Y_CVBS-MON-OUT	B08A (1x)
Y_CVBS-MON-OUT-SC	B08A (2x)

Layout Small Signal Board (Overview Top Side)

1AM0	G5
1AM2	F5
1C00	C1
1C51	D1
1CJ0	A1
1E01	A4
1E05	A5
1E06	A3
1E11	D8
1E15	C8
1E50	B3
1E51	A3
1E99	B6
1F01	D1
1F29	A3
1G50	A1
1G51	B1
1H11	D6
1HE0	B4
1HP0	A3
1M20	G1
1M71	C1
1M95	F1
1N00	E8
1N01	E3
1P00	E7
1P02	A7
1P03	A8
1P05	A8
1P07	D8
1P0A	B8
1P0B	B8
1T04	D8
1T55	E7
1T65	E8
1T70	E7
1T71	D8
1T99	A7
1U01	G1
2A57	E8
2A58	E8
2A59	E8
2A60	E8
2A61	E8
2A63	E8
2A64	E8
2A70	G6
2A71	G6
2AEA	G4
2AEM	G4
2AEU	G4
2C03	C1
2C05	C2
2C06	C1
2C07	C1
2C08	A3
2C09	C1
2C10	C1
2C11	C1
2C12	D2
2C45	C1
2C46	C1
2C47	C1
2CBK	C1
2CBM	C1
2CBN	C1
2CBP	C1
2CBR	C1
2CBS	C1
2CBY	A1
2CG2	C1
2CH0	C1
2CH1	C1
2E06	A6
2E09	A7
2E10	A8
2E11	A6
2E12	B8
2E13	A5
2E14	B8
2E15	B8
2E16	A4
2E17	A4
2E18	B8
2E19	A4
2E20	B8
2E21	B8
2E22	A8
2E23	A8
2E24	A7
2E25	A7
2E26	A6
2E27	A8
2E28	A8
2E29	A3
2E30	A4
2E31	A4
2E32	A4
2E33	A4
2E34	A8
2E35	D8
2E36	A6
2E37	C8
2E39	C8
2E40	C8
2E41	A5
2E42	D8
2E43	D8
2E45	B8
2E46	A6
2E48	A3
2E50	A3
2E51	A4
2E57	B6
2E59	A4
2E64	A6
2E65	A6
2E70	A4
2E73	A5
2E74	A5
2E75	A5
2E76	A5
2E77	A5
2E78	A5
2E79	A5
2E80	B8
2E81	B5
2E82	A4
2E83	A4
2E84	A4
2E85	A4
2E94	A7
2E95	A5
2E97	C8
2E98	C8
2E99	A6
2EA4	A4
2EA5	A3
2EA6	A5
2EB4	A6
2H02	B4
2H10	C4
2H11	B5
2H12	B5
2H14	D6
2H80	B3
2H81	B3
2H82	B3
2H83	B3
2H84	B4
2H85	B4
2H86	B4
2HA0	D4
2HA1	D3
2HHB	D2
2HKA	D2
2HKC	D2
2HMG	C3
2HR0	C5
2HR1	C5
2HR2	C5
2HR3	C5
2HR4	C5
2HR5	C5
2HR6	C5
2HR7	C5
2HR8	C5
2HR9	C5
2HRA	C5
2HRB	C5
2HRC	C5
2HRD	C5
2HRE	C5
2HRF	C5
2HRG	C5
2HRH	C5
2HRJ	C5
2HRK	C5
2HRZ	C5
2HS0	C5
2HS1	C5
2HS2	C5
2HS3	C5
2HS4	D5
2HS7	D5
2HS8	D5
2HS9	D5
2HSA	D5
2HSB	C5
2HSC	C5
2HSD	C5
2HSE	C5
2HSF	D5
2HSJ	D5
2HSK	D5
2HSM	D5
2HSP	C5
2HT8	D5
2HTL	D5
2HTP	D5
2HTR	D5
2HTU	D5
2HTV	D5
2HU5	D5
2HU8	D5
2HVC	B4
2N0K	F4
2N0L	F4
2N0M	E5
2N0N	F5
2N0Z	E4
2N13	E5
2N1C	E5
2N21	E3
2T48	D6
2T49	D6
2T53	D6
2T59	D6
2T61	C6
2T62	D6
2T64	D6
2T67	C6
2T68	D6
2T69	D6
2T71	C6
2T72	C6
2T91	D6
2U05	F2
2U06	F3
2U08	E2
2U09	E2
2U0F	E2
2U0J	E2
2U0K	E2
2U0R	E2
2U0W	E2
2U0Y	F2
2U0Z	F3
2U10	F2
2U11	F2
2U14	F2
2U15	G3
2U19	G2
2U1A	E2
2U1B	E3
2U20	F2
2U21	F1
2U24	E2
2U25	E2
2U26	E2
2U32	G1
2U33	F1
2U34	G1
2U35	G1
2U36	G1
2U40	E2
2U50	E1
2U60	E2
2U62	E2
2U63	E2
2U64	F2
2U65	F2
2U66	E2
2U67	E2
2U68	F2
2U69	F2
2U72	G1
2U73	G1
2U74	G1
2U86	G2
2U8A	G2
2U8C	G2
2U8D	G2
2U8E	G1
2U8F	F2
2U8G	G2
2U8H	G2
2U8K	F2
2U8M	F2
2U8Q	G1
2U8R	G1
2U8U	G2
2U8V	G2
2U90	G1
2U91	G1
2U92	G1
2U93	G1
2U94	G1
2U95	G1
3A18	G5
3A22	G6
3A33	G5
3A34	G5
3A40	G5
3A41	G5
3A42	G5
3A51	G5
3A53	G5
3A55	G5
3A60	E8
3A61	E8
3A62	E8
3A63	E8
3A79	G6
3A80	G6
3A81	G6
3A82	G6
3A83	G6
3A84	G6
3A85	G6
3A86	G6
3A87	G6
3AA1	G3
3AA2	G3
3AA3	F3
3AA4	F3
3AA5	G3
3AA6	G3
3AA7	F3
3AA8	F3
3AA9	G4
3AAB	G3
3AAC	F3
3AAK	F4
3AAL	G4
3AAM	F4
3AM7	F5
3AM8	F5
3C03	A2
3C05	A2
3C06	A2
3C07	A2
3C08	A2
3C09	A2
3C11	A2
3C12	A2
3C13	A2
3C14	C1
3C15	C1
3C16	C2
3C17	C1
3C18	C1
3C19	C1
3C24	C1
3C25	A1
3C26	A2
3C27	A1
3C28	A2
3C29	C1
3C30	A1
3C31	A1
3C32	A1
3C33	C1
3C34	C1
3C35	C1
3C36	C1
3C37	A2
3C38	A3
3C39	A3
3C40	A3
3C41	A2
3C42	A2
3C43	C2
3C44	C1
3C45	C1
3C46	C1
3CA2	A1
3CA3	A1
3CAA	C1
3CAB	C1
3CAC	C1
3CAD	C1
3CAE	C1
3CD0	B3
3CD1	A1
3CD2	A1
3CFK	C2
3CFL	C2
3CH8	C1
3CH9	C1
3CHA	C1
3CHB	C1
3CHC	C1
3CHD	C1
3CHE	C1
3CHF	C1
3CHG	C1
3E01	A6
3E02	A4
3E03	A6
3E05	A6
3E06	A5
3E07	B6
3E08	A6
3E09	B7
3E10	A6
3E11	A4
3E12	B8
3E14	A4
3E15	B8
3E16	A4
3E17	A4
3E18	A4
3E21	A4
3E22	B8
3E23	B8
3E24	A3
3E26	B8
3E34	A4
3E35	A6
3E36	A8
3E37	A8
3E40	A8
3E42	A6
3E44	A8
3E45	A8
3E46	A6
3E47	A6
3E48	A8
3E49	A6
3E50	A8
3E51	A4
3E52	A5
3E53	B8
3E54	A8
3E55	A4
3E56	A7
3E57	A7
3E58	A7
3E59	A7
3E60	A7
3E61	A5
3E62	A5
3E63	A3
3E64	A4
3E65	A6
3E66	A6
3E67	A7
3E68	A7
3E69	A5
3E70	A6
3E71	A6
3E72	A6
3E73	A5
3E74	D8
3E75	A8
3E76	C8
3E77	C8
3E78	C8
3E79	B8
3E80	C8
3E81	D8
3E82	A6
3E83	A5
3E84	A7
3E85	B3
3E89	A6
3E90	A6
3E93	B3
3E94	A8
3E95	A8
3E96	A8
3E97	A8
3E99	A5
3EA1	A5
3EA2	A5
3EA3	B5
3EA5	A5
3EA6	A5
3EA7	A4
3EA8	A3
3EA9	A4
3EB0	A4
3EB1	A5
3EB2	A5
3EB4	A8
3EB5	A8
3EB6	A5
3EB7	A5
3EB8	A5
3EB9	A5
3EC1	A7
3EC2	B8
3EC3	A5
3EC4	A8
3EC5	A8
3EC6	A5
3EC7	A5
3EC8	A5
3ED1	B4
3ED2	B4
3ED3	B4
3ED4	B4
3ED5	B4
3ED8	A7
3H01	B4
3H06	B4
3H07	B4
3H08	B4
3H38	C3
3H41	B5
3H43	B5
3H53	C3
3H54	B4
3H55	C3
3H56	B4
3H61	D4
3H69	B5
3H72	B5
3H73	B5
3H85	B4
3HA0	D3
3HA3	D3
3HA4	D4
3HA8	D4
3HAC	D3
3HG0	B3
3HJ0	C3
3HKM	C3
3HP0	C4
3HP1	C4
3HP5	C4
3HR0	C5
3HR3	C5
3HR6	C4
3HR8	C5
3HR9	C4
3HRC	C5
3HRJ	C5
3HRP	C5
3HRR	C5
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3HRT	D5
3HRU	D5
3HRV	D5
3HRW	C5
3HRY	C5
3HRZ	D5
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3HS9	D5
3HSF	D5
3HSH	D5
3HSJ	D5
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3N0F	F4
3N0H	E5
3N0J	E4
3N0K	E4
3N0V	F4
3N0W	E4
3N0Y	E5
3N36	E3
3T35	D6
3T36	D6
3T37	D6
3T38	C6
3T65	D7
3T66	D7
3T67	E6
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3U08	E2
3U09	E2
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3U1J	E2
3U1W	G2
3U1Y	G2
3U2G	G2
3U2H	G1
3U33	G2
3U34	G2
3U3J	G2
3U3N	G1
3U3T	G2
3U3V	E2
3U3W	E2
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3U52	E2
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3U61	E2
3U62	E2
3U63	E2
3U64	E2
3U65	F2
3U66	F2
3U67	F2
3U68	E2
3U69	E2
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3U70	F3
3U74	E2
3U75	E2
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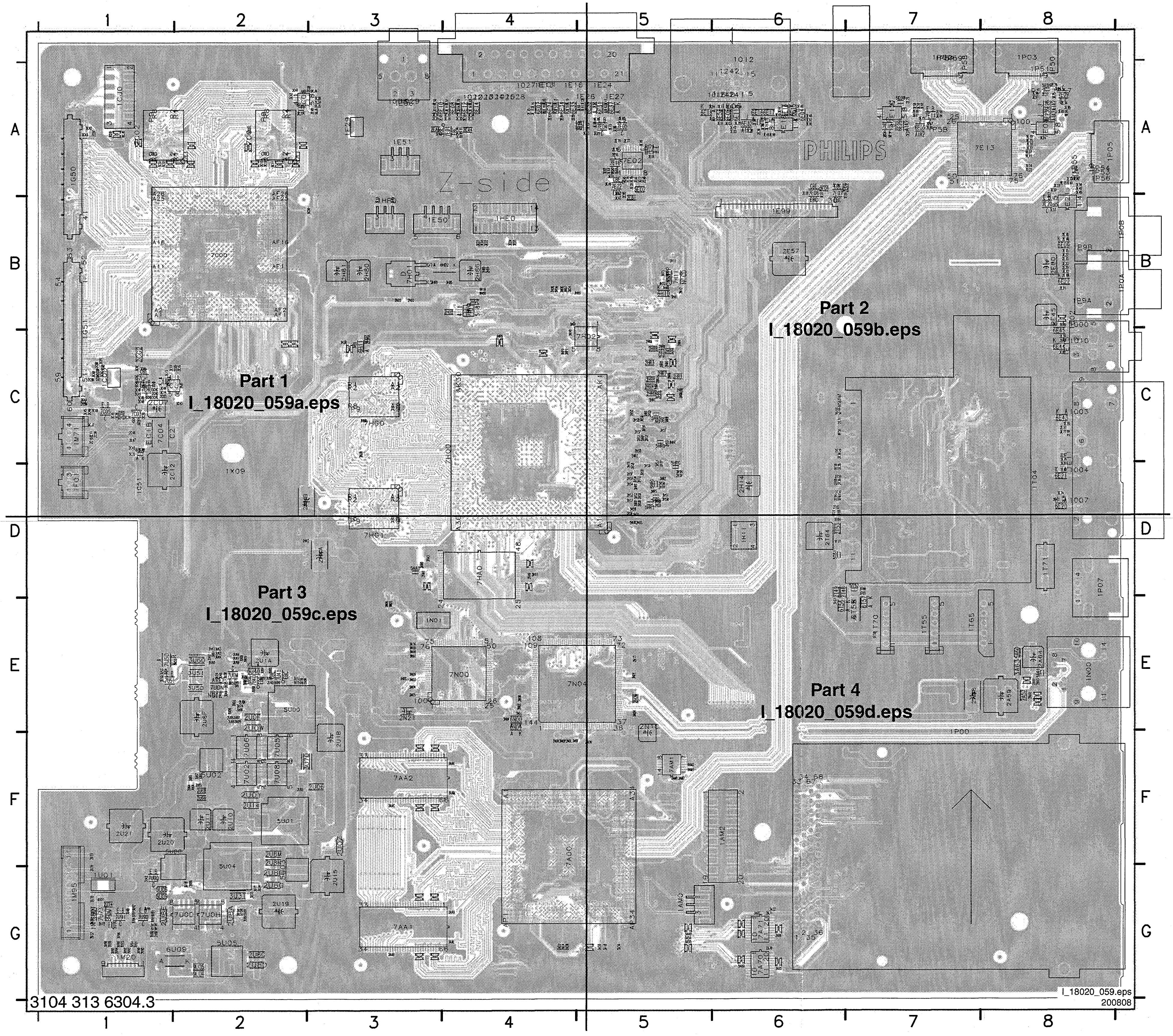
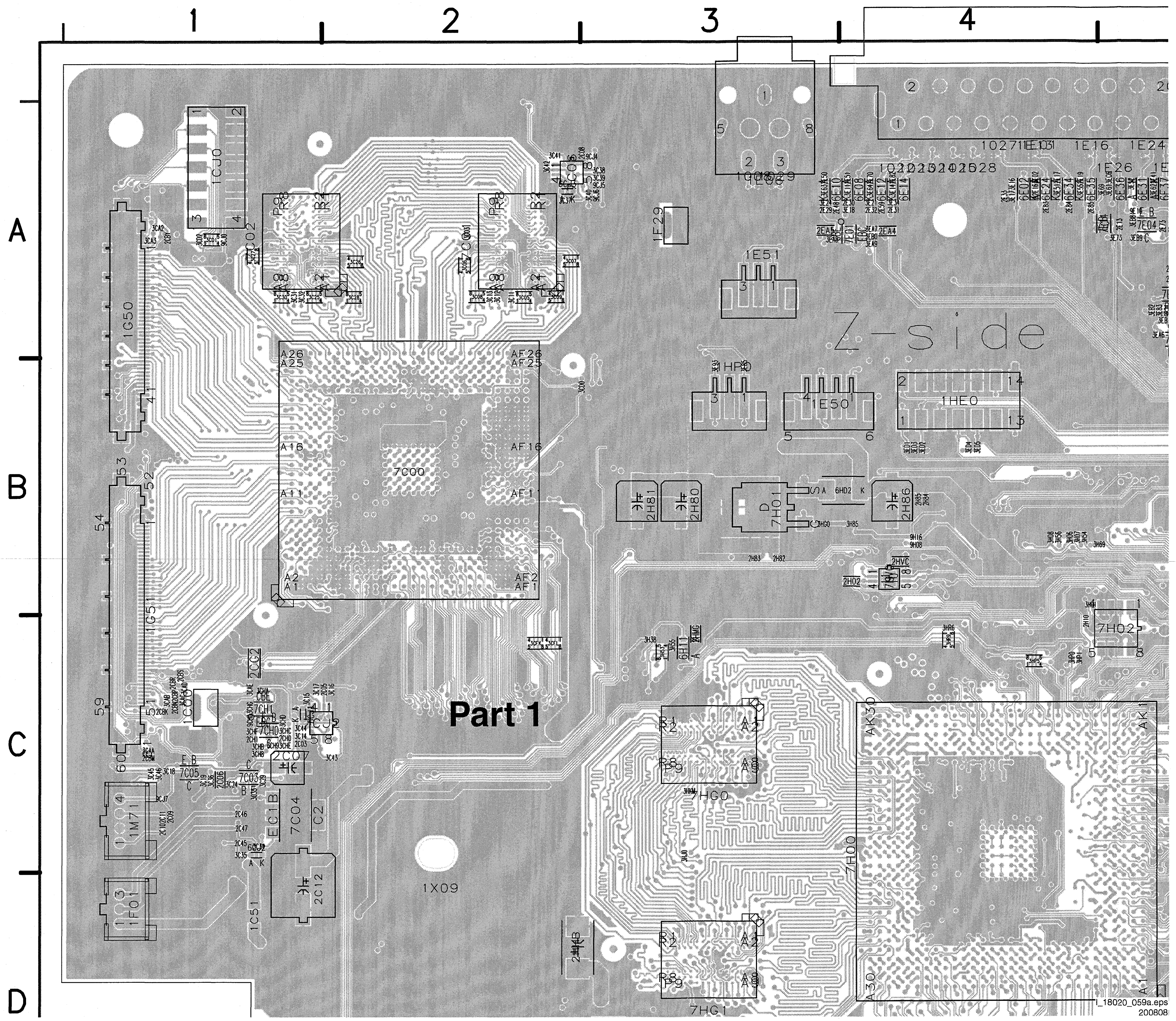
3U93	G1
3U94	G1
3U95	G1
3U96	G1
3U97	G1
3U98	G1
3U99	G1
5A60	E8
5A61	E8
5E02	A5
5E04	A6
5E07	A8
5E08	A7
5E09	A8
5HA0	D3
5HR0	C5
5HR2	D5
5HR3	C5
5HR5	D5
5HRC	D5
5HRG	D5
5T52	D7
5T61	D6
5U00	E3
5U01	F3
5U02	F2
5U03	G2
5U04	F2
5U05	G2
5U06	G1
5U08	F1
5U09	G1
5U90	G1
6CJ1	C1
6CJ2	C1
6CJ3	A2
6E02	A4
6E03	A7
6E04	A6
6E05	A6
6E08	A4
6E09	B8
6E10	A4
6E11	A6
6E12	A4
6E13	A6
6E14	A4
6E15	A6
6E16	A6
6E17	A6
6E18	A5
6E20	D8
6E21	D8
6E22	B8
6E23	A8
6E24	A4
6E26	A8
6E29	A7
6E31	A5
6E32	A6
6E34	A4
6E35	A4
6E36	A5
6E37	A5
6E43	C8
6E44	C8
6E45	C8
6E53	A6
6H10	B5
6H11	C3
6HD2	B4
6N00	E4
6N01	E4
6T55	E7
6T56	E6
6T57	E7
6U09	G1
6U40	E2
7A00	F5
7A70	G6
7A71	G6
7AA1	G3
7AA2	F3
7AM1	F5
7C00	A2
7C01	A2
7C02	A2
7C03	C1
7C04	C2
7C05	C1
7C06	A2
7CH0	C1
7CH1	C1
7CJ2	C2
7E01	A4
7E02	A5
7E04	A5
7E05	A5
7E06	A6
7E07	B6
7E08	A8
7E09	A8
7E11	A7
7E12	A7
7E13	A8
7E14	A4
7E15	A5
7E16	A5
7E18	A6
7E19	A7
7E20	B8
7E21	B8
7E22	A5
7H00	D4
7H01	B3
7H02	B5
7H11	B5
7HA0	D4
7HG0	C3
7HG1	D3
7HV0	B4
7N00	E4
7N04	E5
7U02	F2
7U05	F2
7U06	F2
7U08	F2
7U0D	G2
7U0H	G2
7U0M	E2
7U0N	E2
7U0Q	G1
7U40	E2
7U41	E2
7U50	E1
7U51	E2
7U73	G1
7U90	G1
7U91	G1
9AM1	F5
9AM2	F5
9CH0	C1
9CJ0	A1
9CJ4	A3
9CJ5	A3
9CJ6	A3
9CJ7	C1
9E04	A8
9E07	A8
9E10	A5
9E11	A8
9E13	A8
9E14	A7
9E15	A7
9E19	A8
9E20	A8
9E21	A5
9H06	C5
9H08	B4
9H13	B5
9H16	B4
9N05	E3
9N06	E3
9T21	D6
9T53	C6
9T54	C6
9T55	E7
9T56	C6
9T58	D6
9T61	D6
9T64	D6
9T77	D6
9U01	G1
9U04	G2
9U05	G2
9U90	G1
9U91	G1
9U92	G1



Layout Small Signal Board (Part 1 Top Side)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2
3
4
A
B
C
D
1CJ0
1G50
1G51
1C01
1M71
1F01
1C51
2C12
7C04
7C05
7C03
7CH0
7CH1
2C07
2CG2
7C00
A26
A25
A16
A11
A2
A1
AF26
AF25
AF16
AF11
AF2
AF1
Part 1
1X09
1F29
1E51
1E50
1HP0
1HE0
Z-side
2H81
2H80
7H01
2H86
2H02
2HVC
7H02
7HG0
7HG1
7H00
AK30
AK1
A30
1E16
1E24
1E26
6E02
6E36
6E31
6E34
6E35
7E01
7E04
6E08
6E10
6E12
6E14
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2EA5
I_18020_059a.eps
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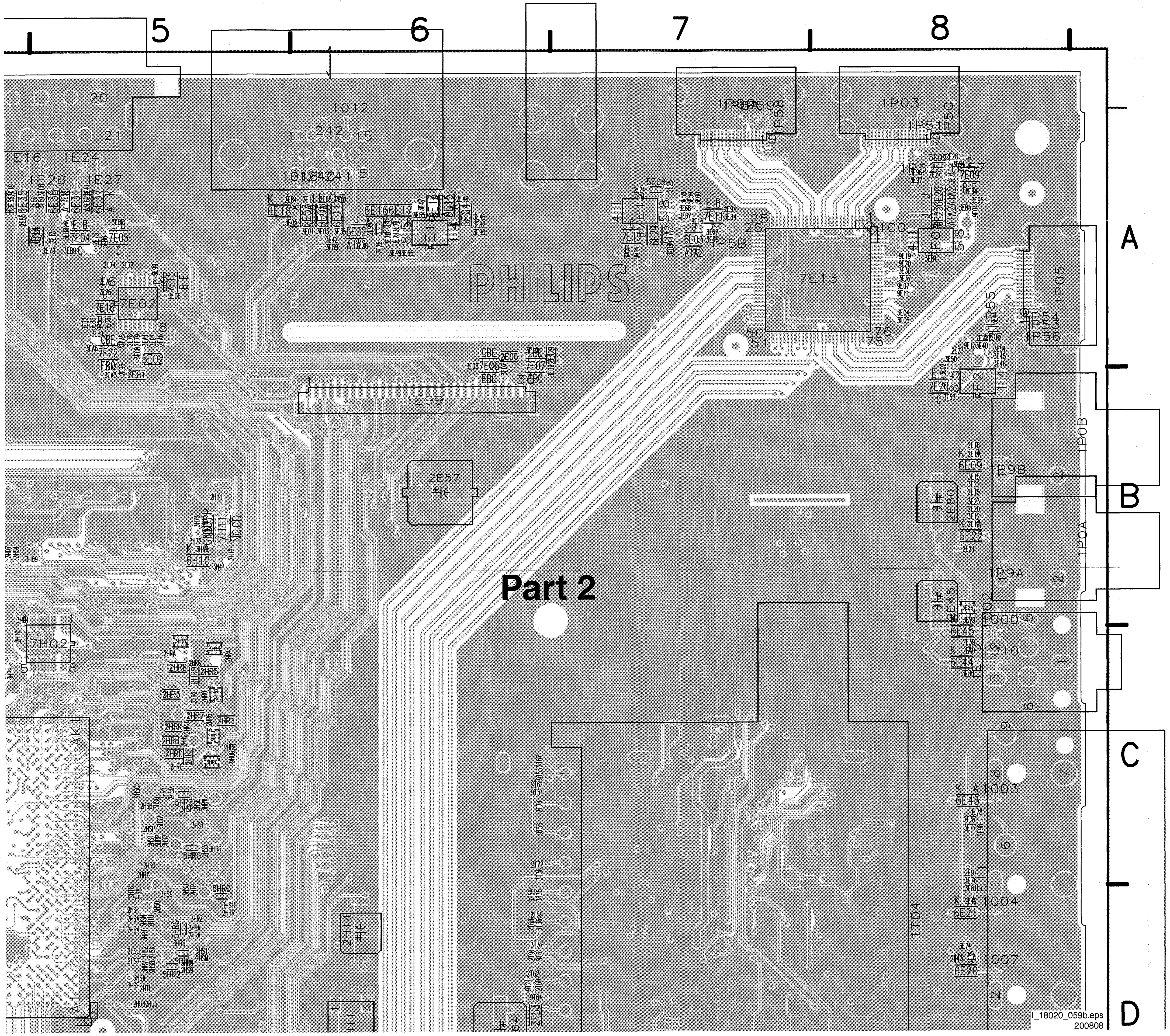
Layout Small Signal Board (Part 2 Top Side)


5
6
7
8
A
B
C
D
Part 2
PHILIPS
1012
1242
1E16
1E24
1E26
1E27
7E02
7E04
7E05
7E22
2EB1
6E18
6E16
6E17
6E04
6E32
6E29
6E03
7E19
7E11
7E13
1P02
1P03
1P50
1P51
1P52
1P5B
1P05
1P54
1P53
1P56
1P55
7E20
7E06
7E07
1E99
2E57
2E80
2E45
1P0B
1P9B
1P0A
1P9A
6E09
6E22
6E45
6E44
1000
1010
1003
6E43
1004
6E21
1007
6E20
1T04
7H11
6H10
7H02
2H14
2HR1
2HR3
2HR5
2HR7
5HRC
5HRG
5HR0
5HR2
I_18020_059b.eps
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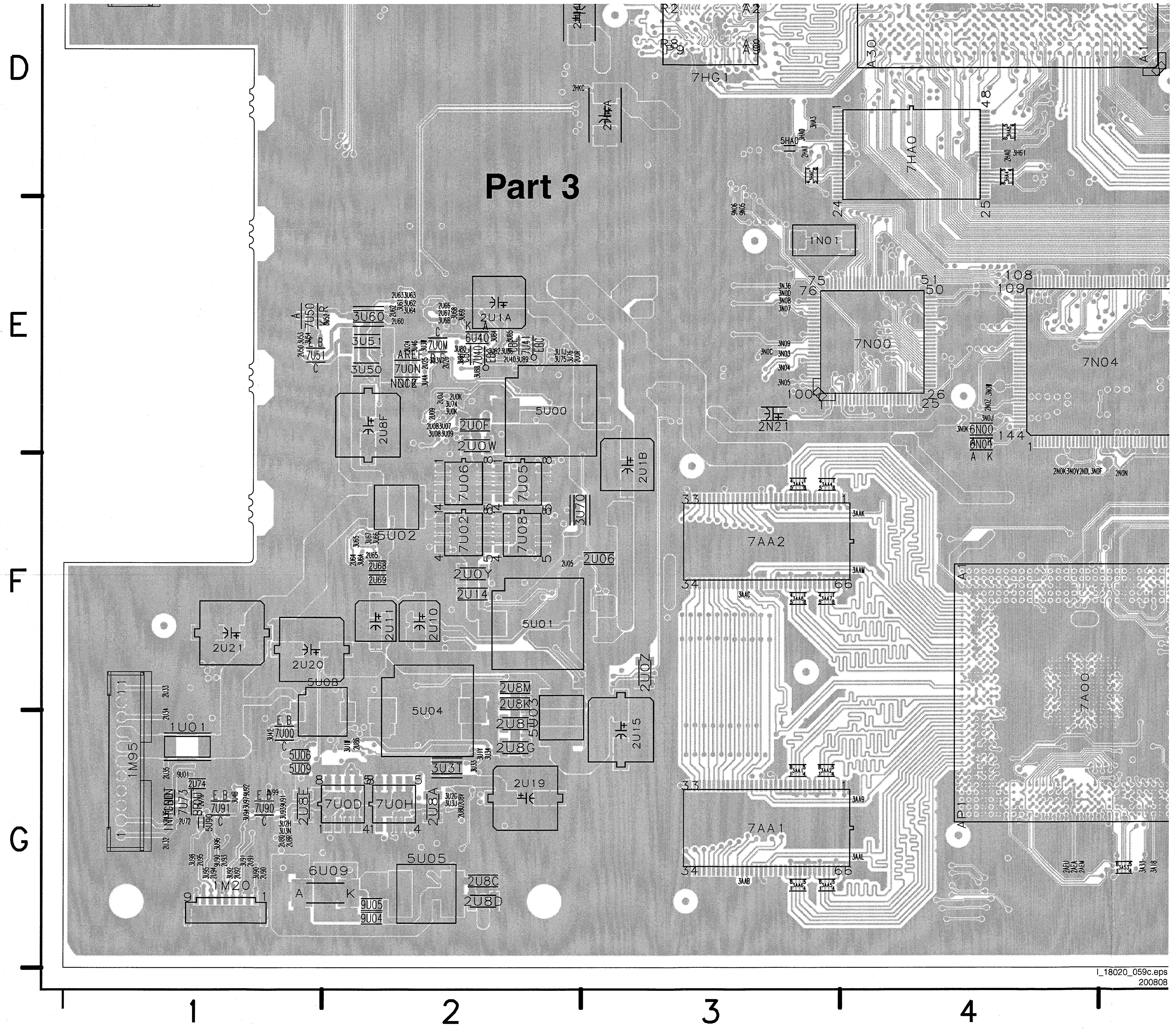
Layout Small Signal Board (Part 3 Top Side)


D
E
F
G
1
2
3
4
Part 3
7HA0
7N00
7N04
7AA2
7AA1
7A00
7HG1
1N01
2N21
5U00
5U01
5U02
5U04
5U05
5U08
7U06
7U05
7U02
7U08
7U0D
7U0H
2U1A
2U1B
2U8F
2U21
2U20
2U11
2U10
2U15
2U19
1U01
1M95
1M20
6U09
6N00
3U60
3U51
3U50
2U06
2U0F
2U0W
2U0Y
2U14
2U0Z
2U8M
2U8K
2U8G
2U8E
2U8A
2U8C
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3U31
3U70
9U05
9U04

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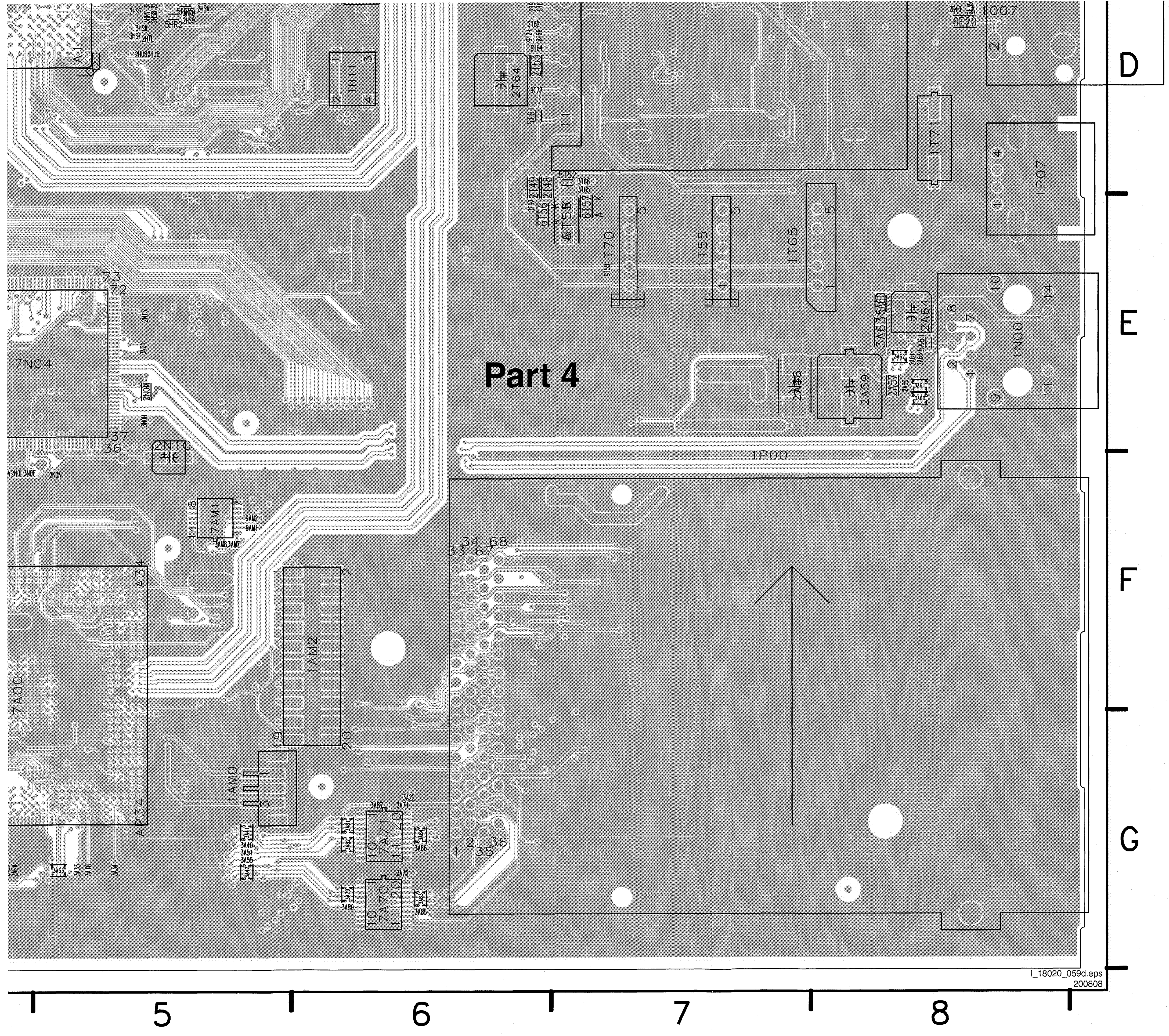
Layout Small Signal Board (Part 4 Top Side)


Part 4
1007
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6T58
6T57
5T52
3T66
3T65
3A63
5A60
2A64
1N00
2A59
2A57
2A58
1P00
7N04
73
72
37
36
2N10
7AM1
1AM2
1AM0
7A00
A34
AP34
7A71
7A70
34
68
33
67
1
2
35
36
D
E
F
G
5
6
7
8
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Layout Small Signal Board (Overview Bottom Side)

1A10 F5
1C50 B8
1C55 B8
1CD0 B6
1HF0 C4
1N02 F4
1T85 D2
1TA1 D2
2A18 F5
2A19 E5
2A20 F5
2A21 F5
2A22 F5
2A23 F5
2A24 G4
2A25 G4
2A26 F4
2A50 G5
2A55 F2
2A56 F2
2A62 E1
2AA0 G5
2AA1 G6
2AA2 F5
2AA3 F6
2AA6 G6
2AA7 G6
2AA8 G6
2AA9 F6
2AAA F6
2AAB F6
2AAE F6
2AAF F6
2AAG F6
2AAH F5
2AAJ F6
2AAK F6
2AAL G6
2AAM G6
2AAN G6
2AAP G6
2AAR G6
2AAS G5
2AAT G6
2AAU G6
2AAZ F5
2AB0 F5
2AB1 F5
2AB2 F5
2AB3 F5
2AB4 F5
2AB5 G5
2AB6 G5
2AB8 F5
2AB9 F5
2ABA F5
2ABB F5
2AC0 F4
2AE2 G4
2AE5 G5
2AE7 G4
2AE8 G4
2AEB G4
2AEC G5
2AED F5
2AEE F4
2AEH F5
2AEJ F4
2AEN G4
2AER G4
2AET F4
2AEZ F4
2AF0 G4
2AF4 F4
2AF5 F4
2AF8 G4
2AFB G5
2AFC G5
2AFD G5
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2AFF G4
2AFG F4
2AFH F4
2AFJ G4
2AFK G4
2AFL G4
2AFN F5
2AFR F5
2AFS F5
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2AG5 F4
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2AGN G5
2AGP G4
2AGT F5
2AM0 G4
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2AM2 F4
2AM3 F4
2AM4 F4
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2C01 A7
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2C43 A8
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2C56 A6
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2C61 B7
2C62 B7
2C63 B7
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2C96 B7
2C97 B7
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2CA9 A8
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2CAC A8
2CAD A8
2CAE A8
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2CAG A8
2CAH A8
2CAJ A8
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2CAM A8
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2CAR A8
2CAS C8
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2CAV C8
2CAW C8
2CAY C8
2CAZ C8
2CB0 C8
2CB1 C8
2CB2 C8
2CB3 C8
2CB4 C8
2CB5 B8
2CB6 B8
2CB7 B8
2CB8 B8
2CB9 B8
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2CBB B8
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2CGD A8
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2E61 B6
2E62 B6
2E63 B6
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2H06 C4
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2H09 D3
2H13 D3
2H15 D4
2H16 D4
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2H88 B6
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2HA4 D4
2HA5 C4
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2HG5 C6
2HG6 C6
2HG7 C6
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2HGZ D6
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2HH5 C6
2HH6 D5
2HH7 D5
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2HH9 C5
2HHA C6
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2HHF D6
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2HHJ C6
2HHK C6
2HHM C5
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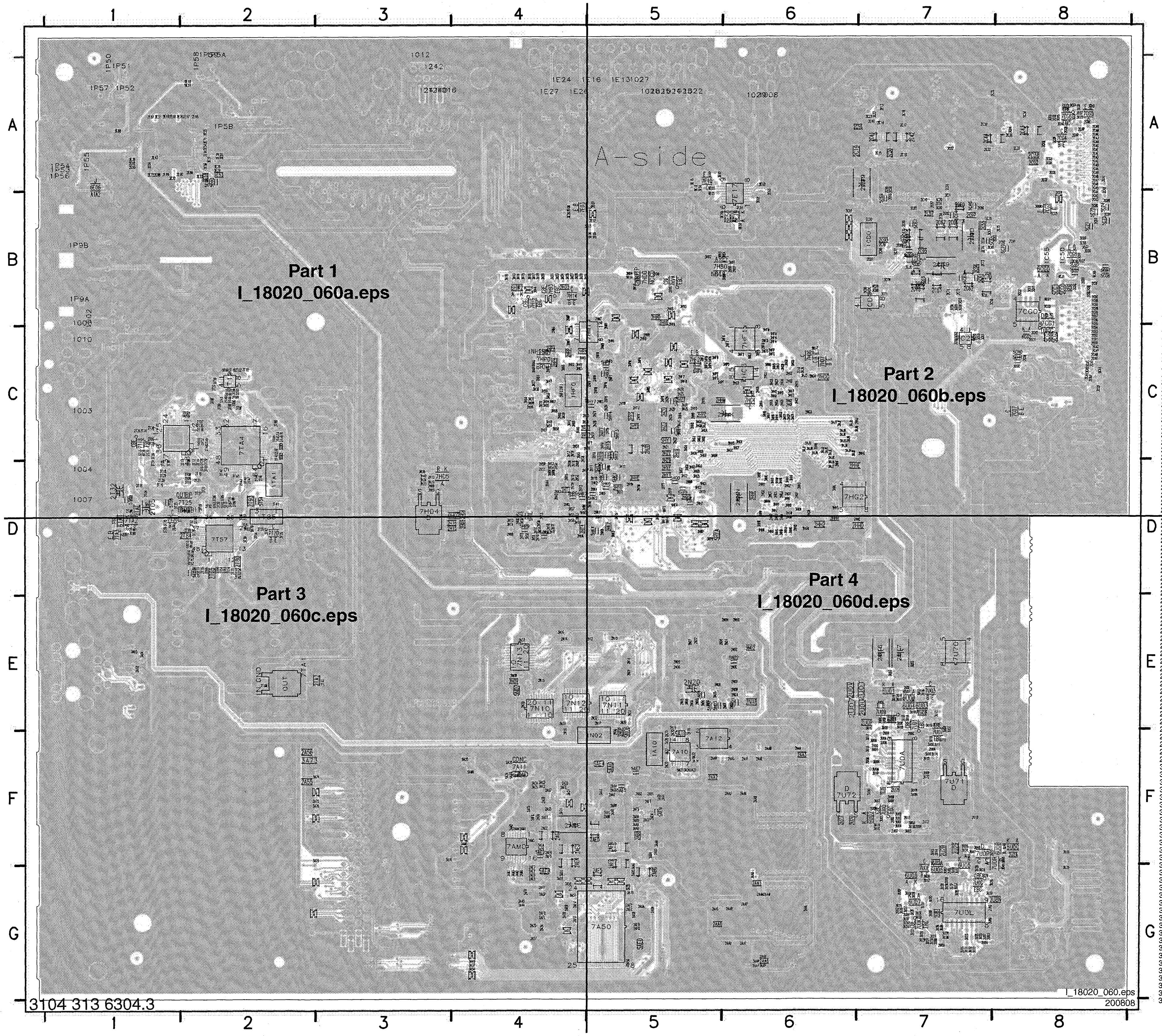
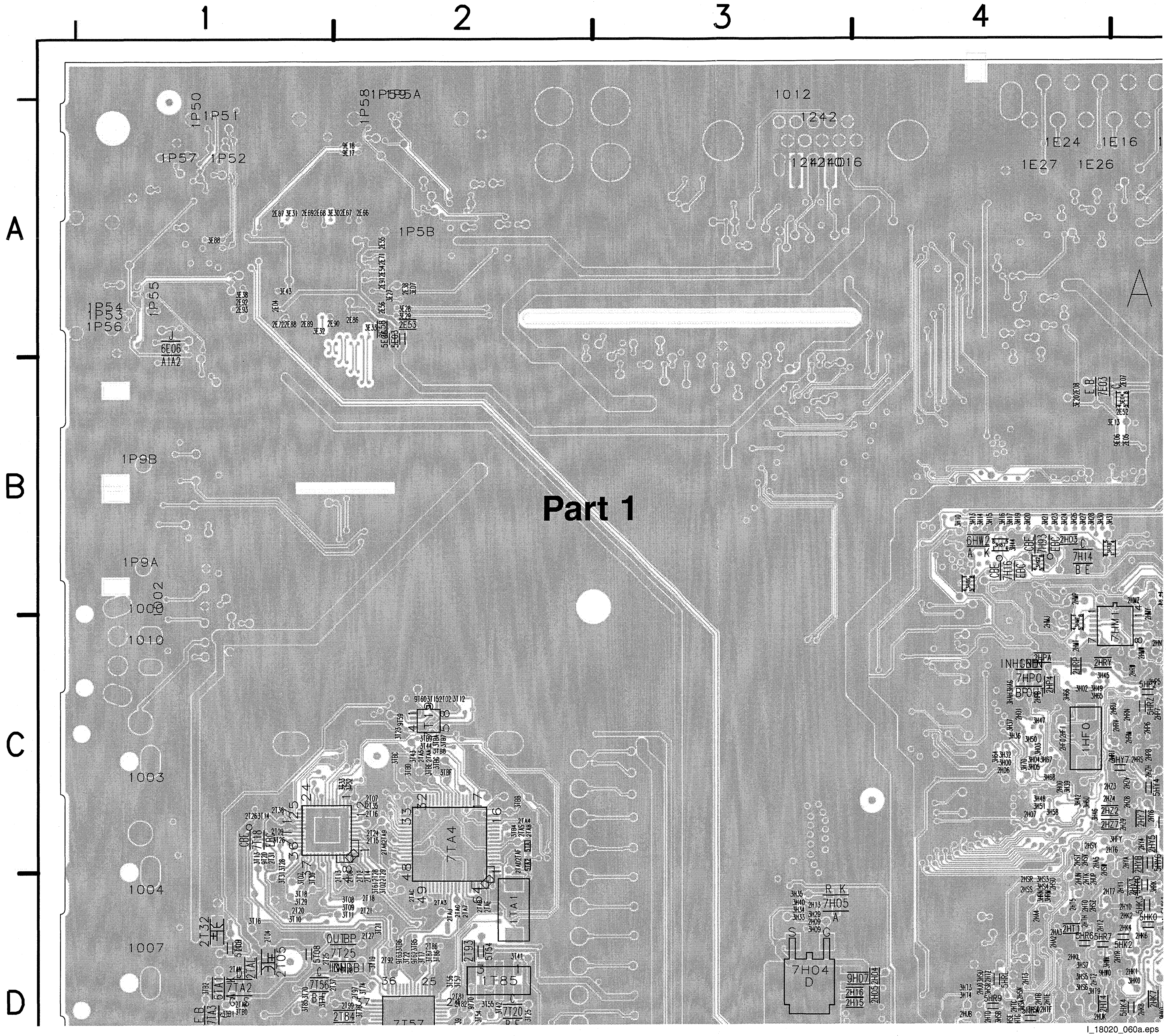


Layout Small Signal Board (Part 1 Bottom Side)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A
B
C
D
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1P5B
1P54
1P53
1P56
1P55
6E06
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1P9A
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1004
1007
1012
1242
1E24
1E16
1E27
1E26
7E03
7TA4
1TA1
1T85
7T25
7T20
7T57
7TA2
7TA3
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7HM1
7H14
6HW2
2H03

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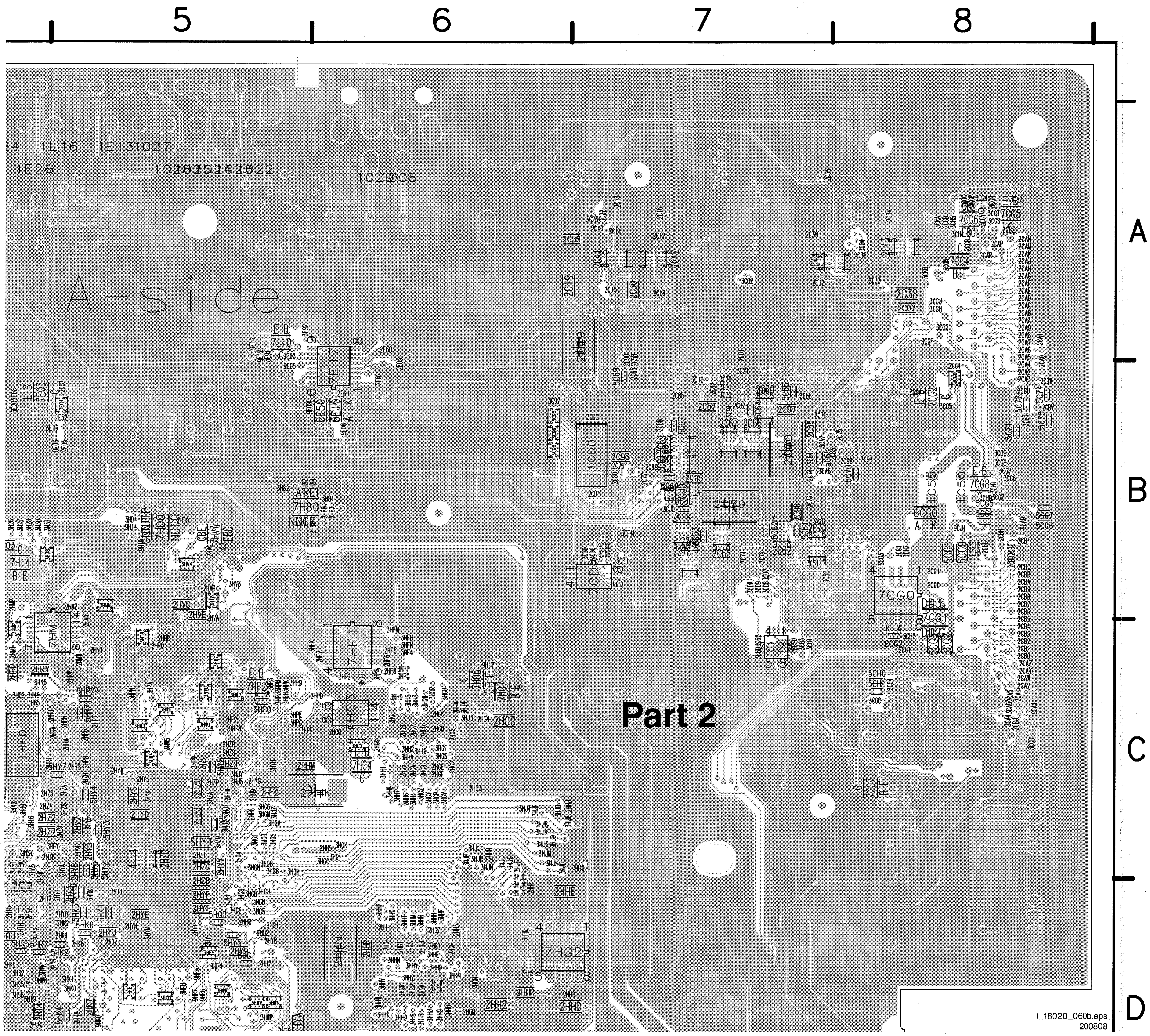
Layout Small Signal Board (Part 2 Bottom Side)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6
7
8
A
B
C
D
A-side
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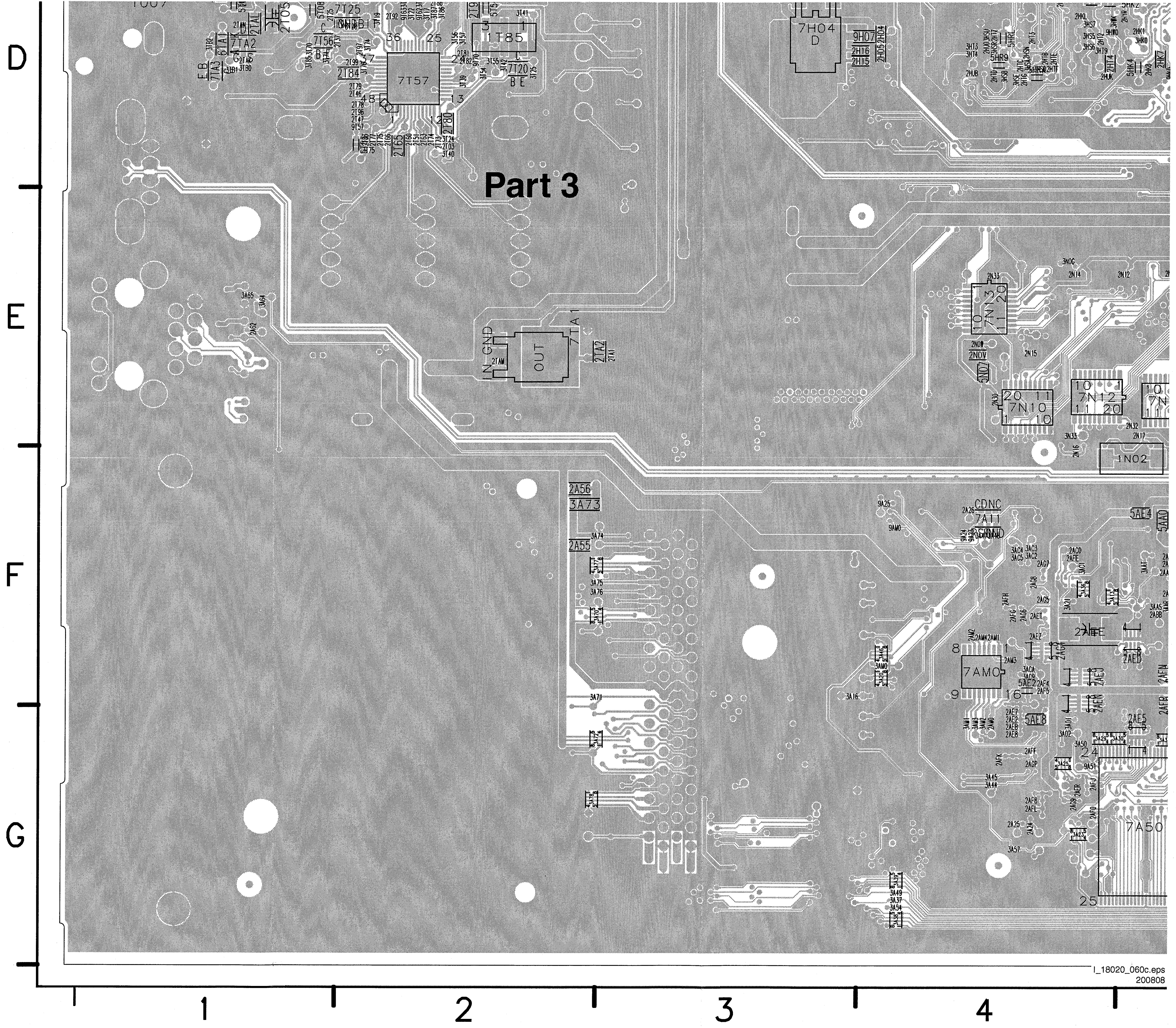
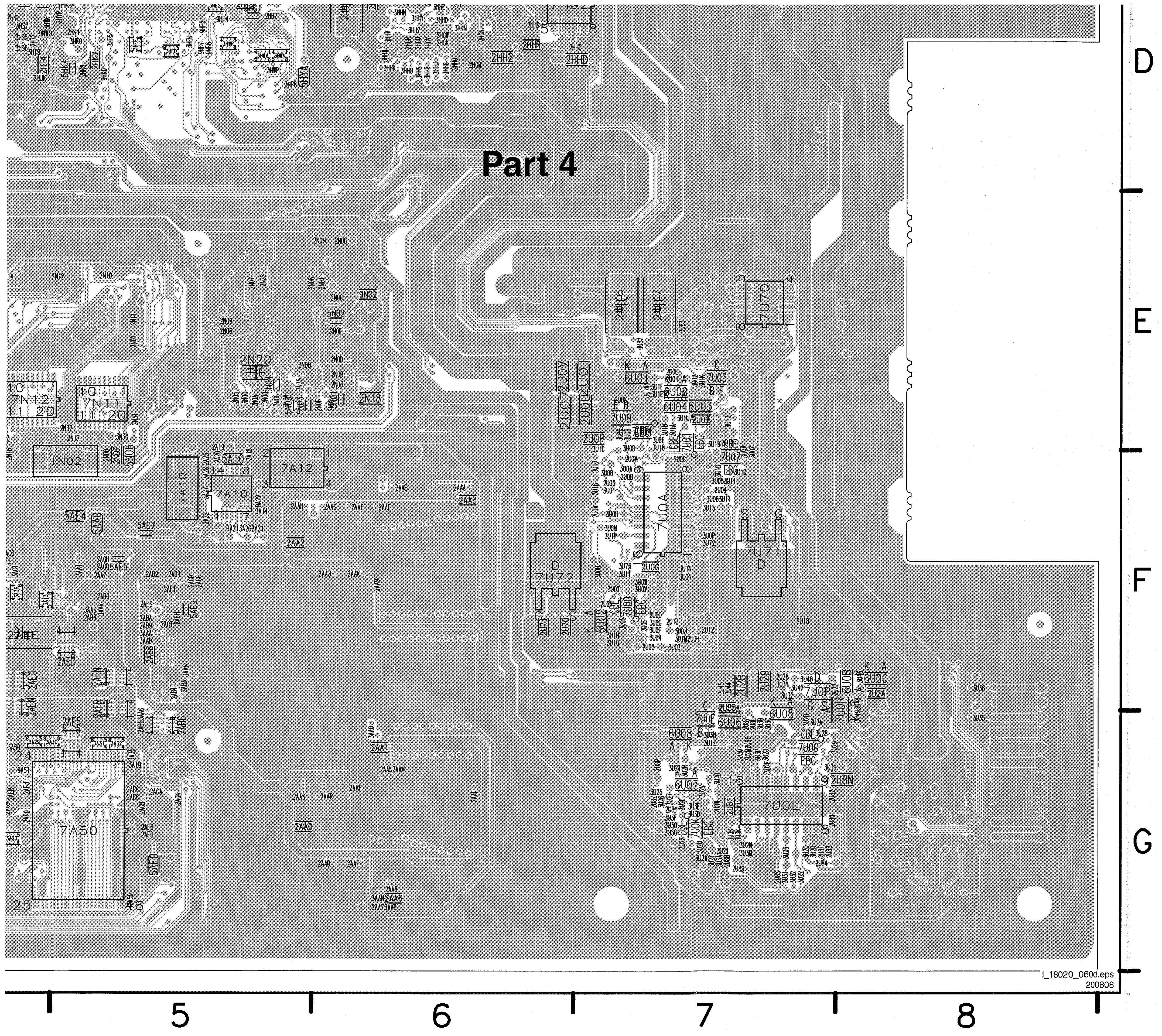
Layout Small Signal Board (Part 3 Bottom Side)

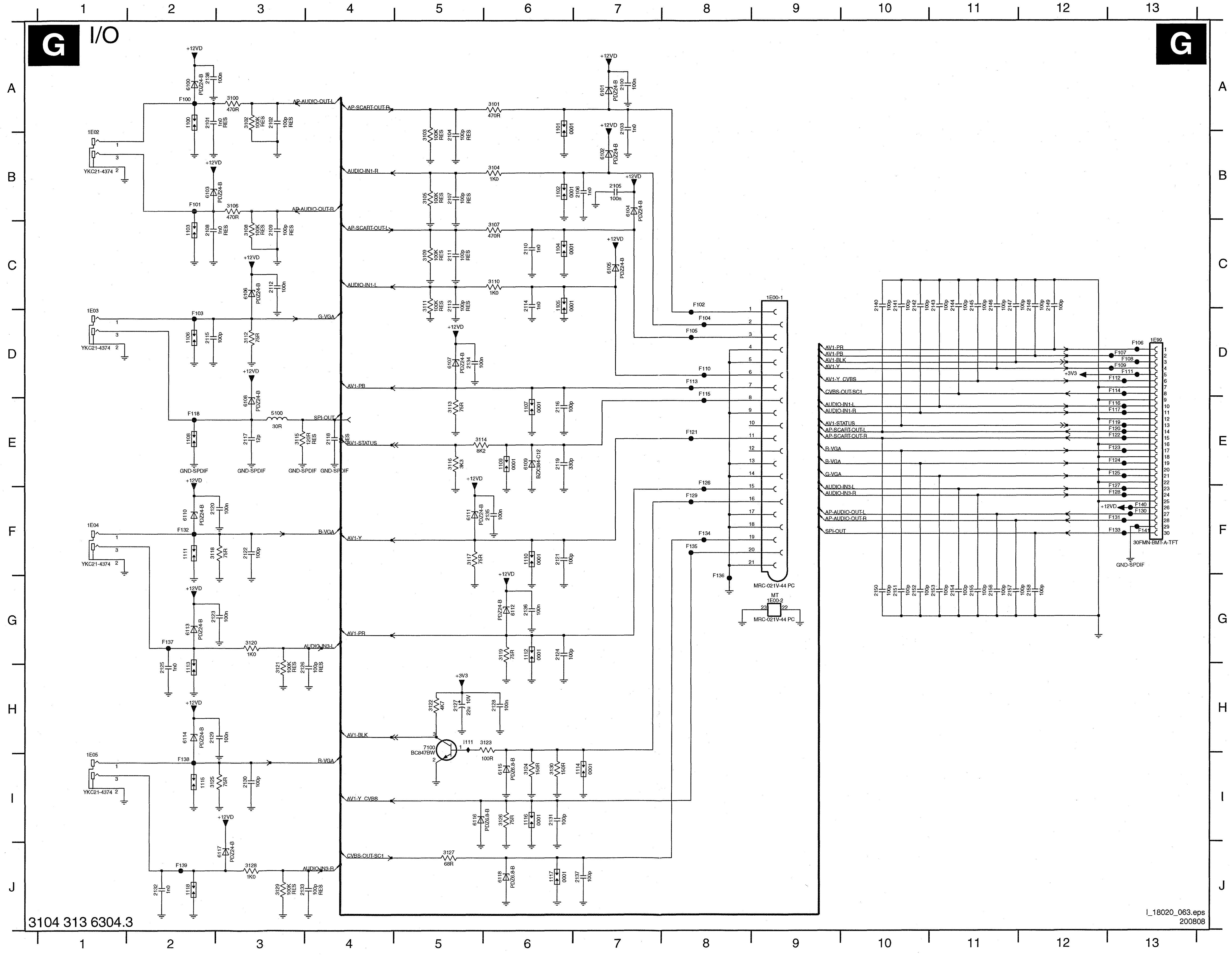

D
E
F
G
1
2
3
4
Part 3
7T57
1T85
7H04
7N13
7N10
7N12
1N02
7A11
7AM0
7A50
7TA1
OUT
IN GND
2A56
3A73
2A55
I_18020_060c.eps
200808

Layout Small Signal Board (Part 4 Bottom Side)


Part 4
D
E
F
G
5
6
7
8
7U0A
7U0L
7U70
7U71
7U72
7A50
7A10
7A12
1A10
7N12
7N11
1N02
2N20
2N18
9N02
5N02
2HH2
2HHR
2HHD
2AA3
2AA2
2AA1
2AA0
2AA6
2U0P
2U0G
2U8N
2U2A
6U0C
6U0B
6U05
6U06
6U07
6U08
6U01
6U02
6U03
6U04
7U0P
7U0E
7U0G
7U07
7U09
7U00
5AE4
5AE7
5AE9
5AE0
2AED

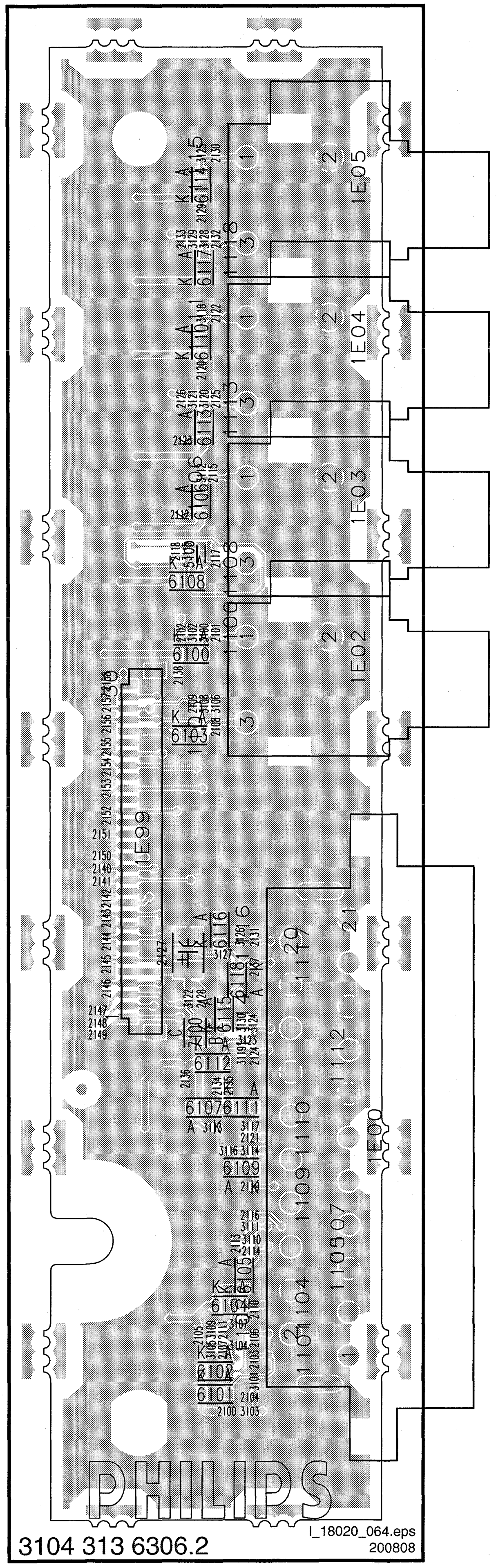
I_18020_060d.eps
200808

I/O Panel


G
I/O
1E02
YKC21-4374
1E03
1E04
1E05
1E99
30FMN-BMT-A-TFT
1E00-1
1E00-2
MRC-021V-44 PC
MT
7100
BC847BW
+12VD
+3V3
GND-SPDIF
AP-AUDIO-OUT-L
AP-AUDIO-OUT-R
AP-SCART-OUT-R
AP-SCART-OUT-L
AUDIO-IN1-R
AUDIO-IN1-L
AUDIO-IN3-L
AUDIO-IN3-R
G-VGA
B-VGA
R-VGA
SPI-OUT
AV1-STATUS
AV1-PR
AV1-PB
AV1-Y
AV1-BLK
AV1-Y_CVBS
CVBS-OUT-SC1
PDZ24-B
PDZ6.8-B
BZX384-C12
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H I J
3104 313 6304.3
I_18020_063.eps
200808

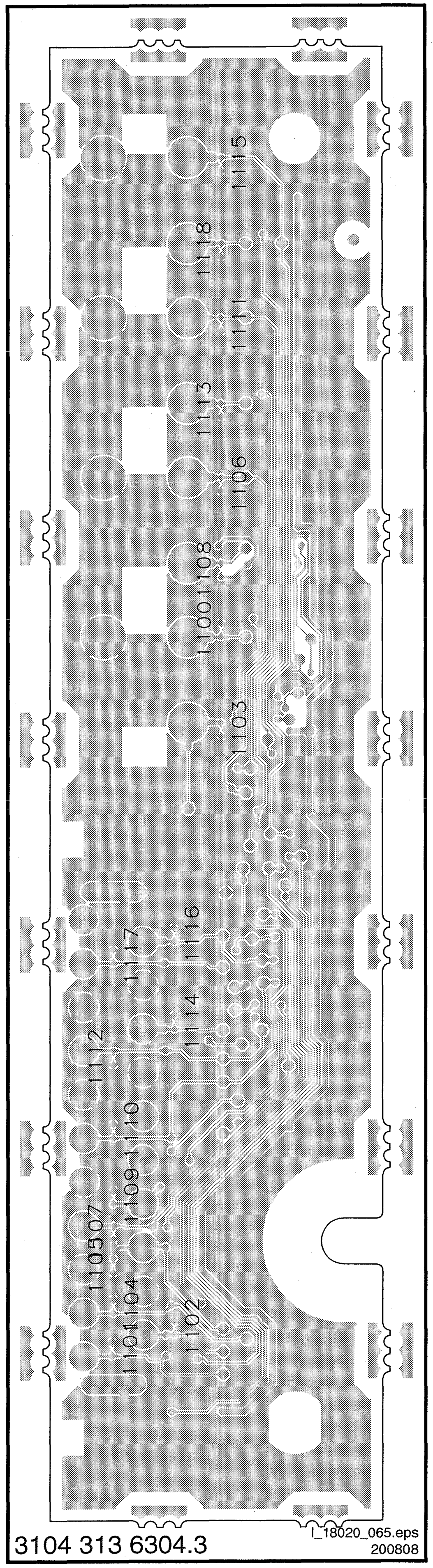
1100	A2
1101	A6
1102	B6
1103	C2
1104	C6
1105	C6
1106	D2
1107	E6
1108	E2
1109	E6
1110	F6
1111	F2
1112	G6
1113	H2
1114	I7
1115	I2
1116	I6
1117	J6
1118	J2
1E00-1	C9
1E00-2	G9
1E02	A1
1E03	C1
1E04	F1
1E05	H1
1E99	D13
2100	A7
2101	A2
2102	A3
2103	A7
2104	B5
2105	B7
2106	B7
2107	B5
2108	C2
2109	C3
2110	C6
2111	C5
2112	C3
2113	C5
2114	C6
2115	D2
2116	E6
2117	E3
2118	E4
2119	E6
2120	F2
2121	F6
2122	F3
2123	G2
2124	G6
2125	H2
2126	H3
2127	H5
2128	H6
2129	H2
2130	I3
2131	I6
2132	J2
2133	J3
2134	D5
2135	F6
2136	G6
2137	J7
2138	A2
2140	C10
2141	C10
2142	C10
2143	C11
2144	C11
2145	C11
2146	C11
2147	C11
2148	C12
2149	C12
2150	G10
2151	G10
2152	G10
2153	G11
2154	G11
2155	G11
2156	G11
2157	G11
2158	G12
3100	A3
3101	A6
3102	A3
3103	B5
3104	B6
3105	B5
3106	B3
3107	C6
3108	C3
3109	C5
3110	C6
3111	C5
3112	D3
3113	E5
3114	E5
3115	E3
3116	E5
3117	F5
3118	F2
3119	G6
3120	G3
3121	H3
3122	H5
3123	H6
3124	I6
3125	I2
3126	I6
3127	J5
3128	J3
3129	J3
3130	I6
5100	E3
6100	A2
6101	A7
6102	B7
6103	B2
6104	B7
6105	C7
6106	C3
6107	D5
6108	E3
6109	E6
6110	F2
6111	F5
6112	G6
6113	G2
6114	H2
6115	I6
6116	I5
6117	J3
6118	J6
7100	H5
F100	A2
F101	B2
F102	C8
F103	D2
F104	D8
F105	D8
F106	D13
F107	D13
F108	D13
F109	D13
F110	D8
F111	D13
F112	D13
F113	D8
F114	D13
F115	D8
F116	E13
F117	E13
F118	E2
F119	E13
F120	E13
F121	E8
F122	E13
F123	E13
F124	E13
F125	E13
F126	E8
F127	F13
F128	F13
F129	F8
F130	F13
F131	F13
F132	F2
F133	F13
F134	F8
F135	F8
F136	G8
F137	G2
F138	I2
F139	J2
F140	F13
F141	F13
I111	H5

Layout I/O Panel (Top Side)

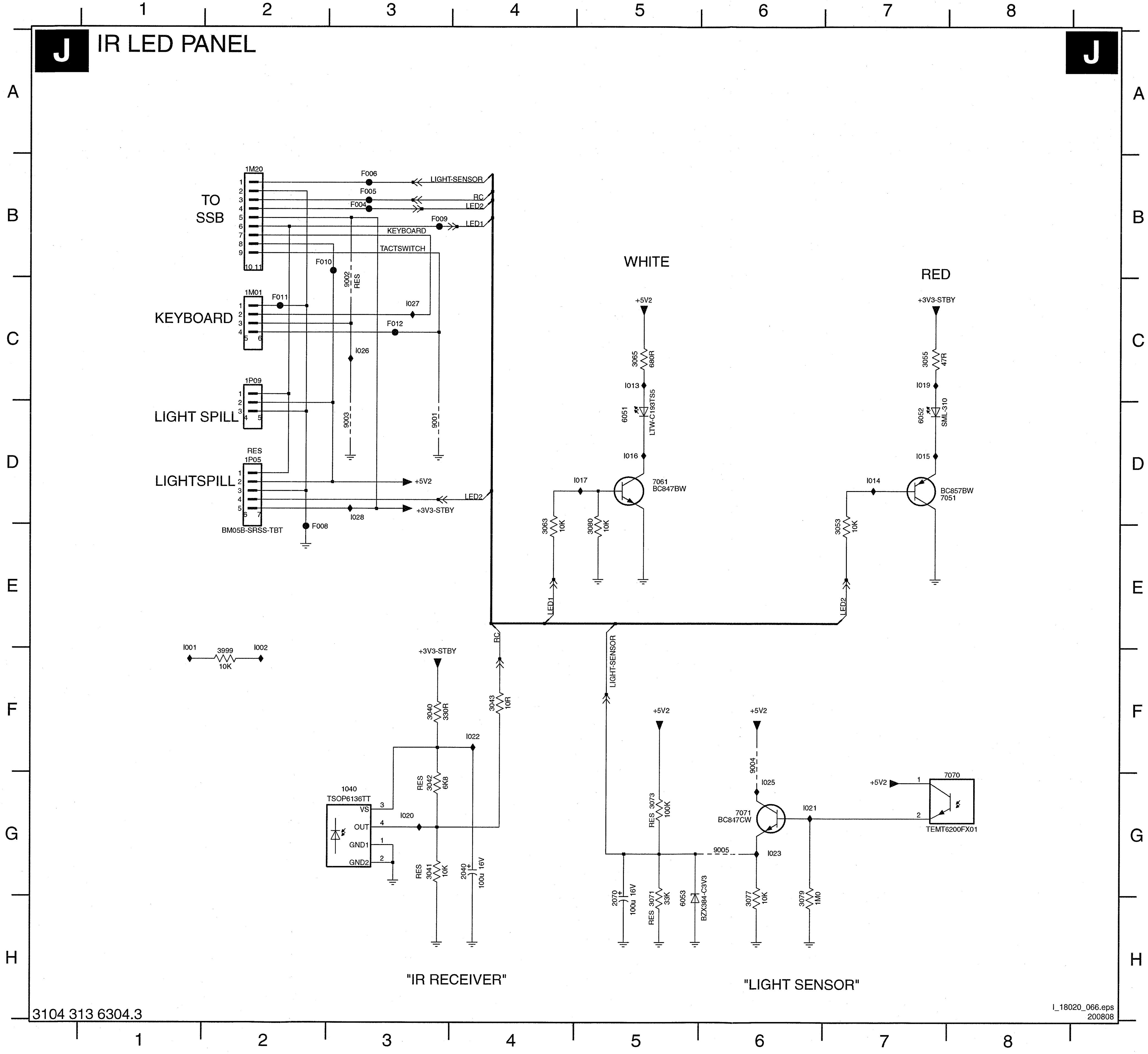

1E05
1E04
1E03
1E02
1E00
1E99
1118
1113
1108
1100
1129
1119
1121
1112
1110
1109
1107
1105
1104
1101
6100
6101
6102
6103
6105
6106
6107
6108
6109
6111
6112
6115
6116
6117
PHILIPS
3104 313 6306.2
I_18020_064.eps
200808

1E00	--
1E02	--
1E03	--
1E04	--
1E05	--
1E99	--
2100	--
2101	--
2102	--
2103	--
2104	--
2105	--
2106	--
2107	--
2108	--
2109	--
2110	--
2111	--
2112	--
2113	--
2114	--
2115	--
2116	--
2117	--
2118	--
2119	--
2120	--
2121	--
2122	--
2123	--
2124	--
2125	--
2126	--
2127	--
2128	--
2129	--
2130	--
2131	--
2132	--
2133	--
2134	--
2135	--
2136	--
2137	--
2138	--
2140	--
2141	--
2142	--
2143	--
2144	--
2145	--
2146	--
2147	--
2148	--
2149	--
2150	--
2151	--
2152	--
2153	--
2154	--
2155	--
2156	--
2157	--
2158	--
3100	--
3101	--
3102	--
3103	--
3104	--
3105	--
3106	--
3107	--
3108	--
3109	--
3110	--
3111	--
3112	--
3113	--
3114	--
3115	--
3116	--
3117	--
3118	--
3119	--
3120	--
3121	--
3122	--
3123	--
3124	--
3125	--
3126	--
3127	--
3128	--
3129	--
3130	--
5100	--
6100	--
6101	--
6102	--
6103	--
6104	--
6105	--
6106	--
6107	--
6108	--
6109	--
6110	--
6111	--

Layout I/O Panel (Bottom Side)


1115
1118
1111
1113
1106
1108
1100
1103
1116
1117
1114
1112
1110
1109
1105
1107
1104
1101
1102
3104 313 6304.3
I_18020_065.eps
200808

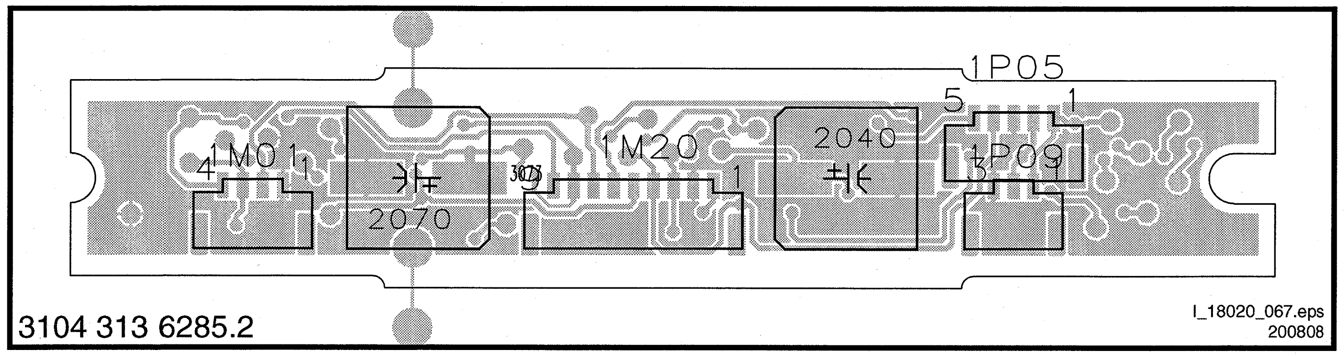
IR & LED Panel (ME TOP)


J
IR LED PANEL
J
TO SSB
1M20
F006
LIGHT-SENSOR
F005
RC
F004
LED2
F009
LED1
KEYBOARD
TACTSWITCH
F010
9002
RES
KEYBOARD
1M01
F011
I027
F012
I026
LIGHT SPILL
1P09
9003
9001
LIGHTSPILL
RES
1P05
+5V2
LED2
+3V3-STBY
I028
F008
BM05B-SRSS-TBT
WHITE
+5V2
3065
680R
I013
6051
LTW-C193TS5
I016
I017
7061
BC847BW
3063
10K
3080
10K
LED1
RED
+3V3-STBY
3055
47R
I019
6052
SML-310
I015
I014
BC857BW
7051
3053
10K
LED2
RC
LIGHT-SENSOR
I001
3999
10K
I002
+3V3-STBY
3040
330R
3043
10R
I022
1040
TSOP6136TT
VS
OUT
GND1
GND2
I020
RES
3042
6K8
RES
3041
10K
2040
100u 16V
+5V2
+5V2
9004
I025
RES 3073
100K
7071
BC847CW
I021
+5V2
7070
TEMT6200FX01
9005
I023
2070
100u 16V
RES 3071
33K
6053
BZX384-C3V3
3077
10K
3079
1M0
"IR RECEIVER"
"LIGHT SENSOR"
3104 313 6304.3
I_18020_066.eps
200808
1 2 3 4 5 6 7 8
A B C D E F G H

1040	G3
1M01	C2
1M20	B2
1P05	D2
1P09	C2
2040	G4
2070	H5
3040	F3
3041	G3
3042	G3
3043	F4
3053	E7
3055	C7
3063	E4
3065	C5
3071	H5
3073	G5
3077	H6
3079	H6
3080	E5
3999	F2
6051	D5
6052	D7
6053	H5
7051	D7
7061	D5
7070	G8
7071	G6
9001	D3
9002	C3
9003	D3
9004	F6
9005	G6
F004	B3
F005	B3
F006	B3
F008	E2
F009	B3
F010	B2
F011	C2
F012	C3
I001	E1
I002	E2
I013	C5
I014	D7
I015	D7
I016	D5
I017	D5
I019	C7
I020	G3
I021	G6
I022	F4
I023	G6
I025	G6
I026	C3
I027	C3
I028	D3

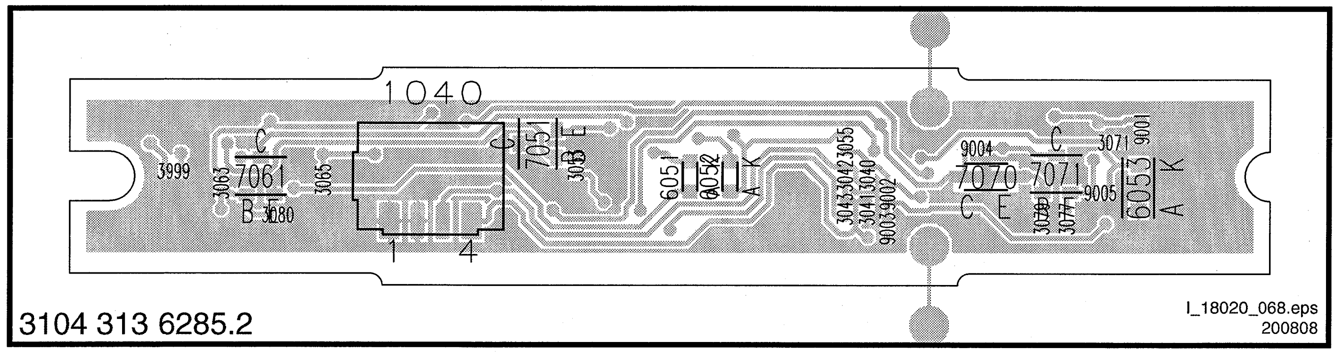
Layout IR & LED Panel (ME TOP) (Top Side)

1M01 --	1M20 --	1P05 --	1P09 --	2040 --	2070 --	3073 --


1P05
5
1
1M01
4
1
2070
3073
1M20
1
2040
1P09
3
3104 313 6285.2
I_18020_067.eps
200808

Layout IR & LED Panel (ME TOP) (Bottom Side)

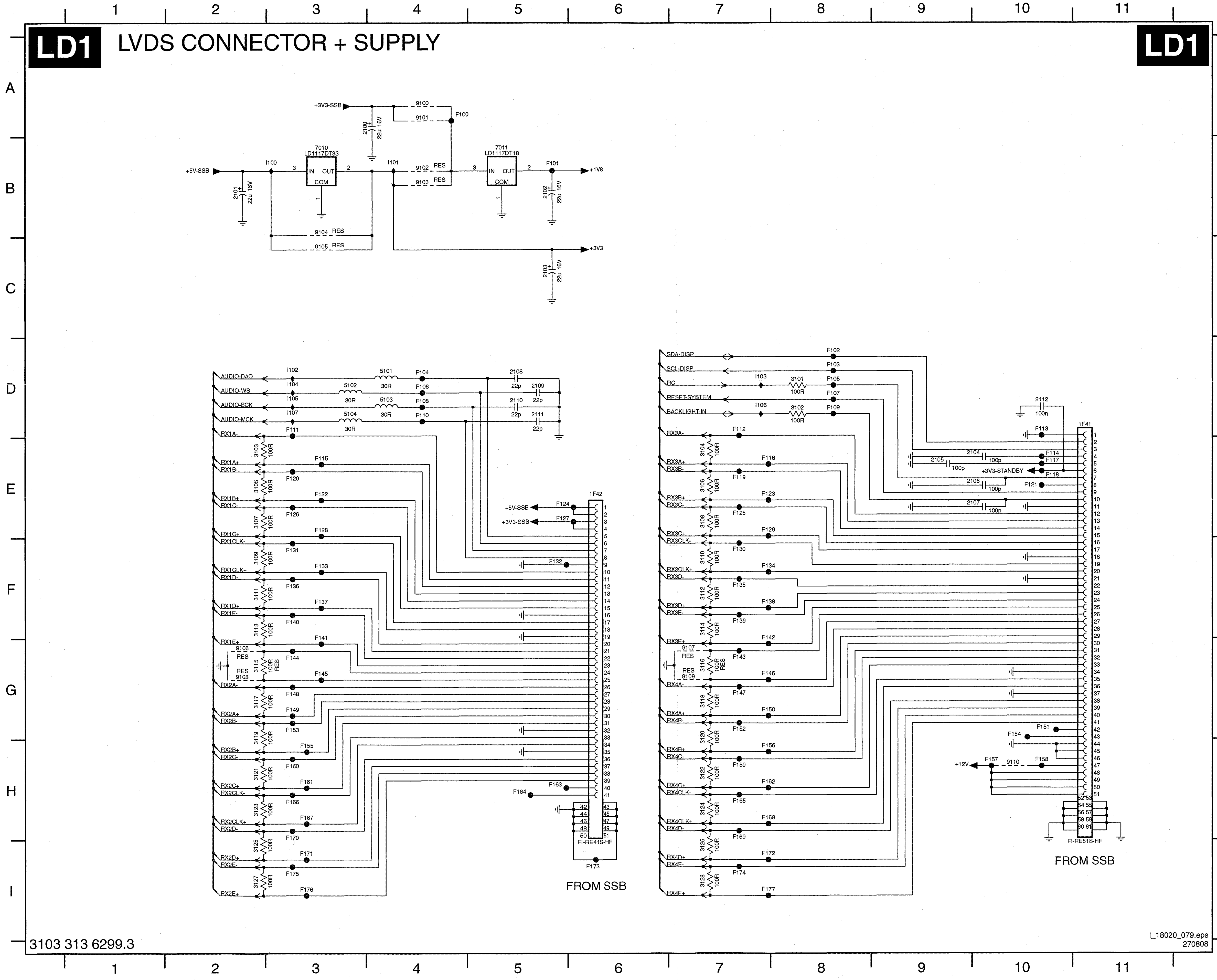
1040 --	3042 --	3055 --	3071 --	3080 --	6052 --	7061 --	9001 --	9004 --
3040 --	3043 --	3063 --	3077 --	3999 --	6053 --	7070 --	9002 --	9005 --
3041 --	3053 --	3065 --	3079 --	6051 --	7051 --	7071 --	9003 --	


1040
3999
3063
C
7061
B
E
3080
3065
1
4
C
7051
B
E
3053
6051
6052
A
K
3043 3042 3055
3041 3040
9003 9002
9004
7070
C
E
C
7071
3071
9001
9005
3079
3077
6053
A
K
3104 313 6285.2
I_18020_068.eps
200808

Personal Notes:

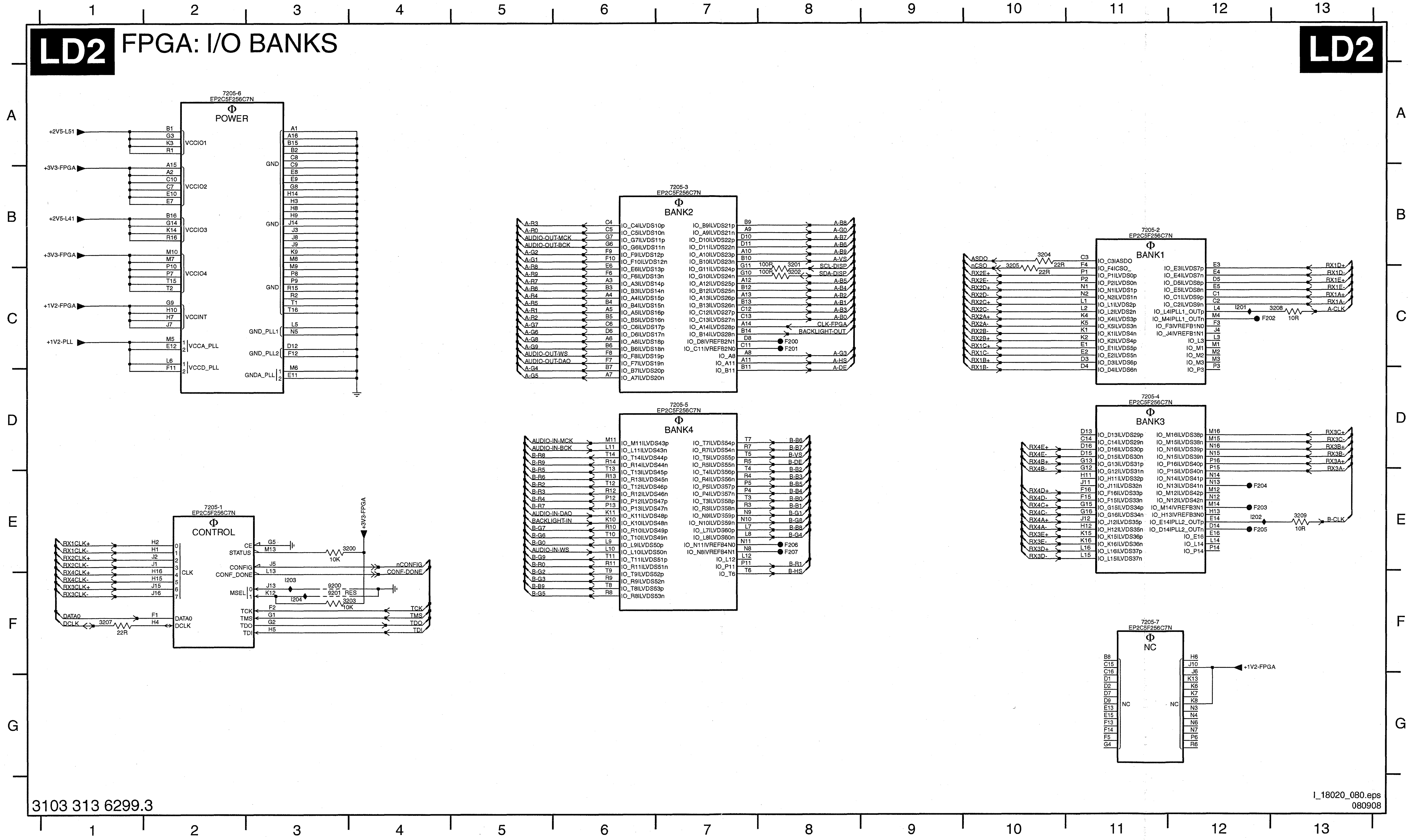
E_06532_012.eps
131004

LVDS2DP Panel: Connector & Supply


LD1
LVDS CONNECTOR + SUPPLY
1
2
3
4
5
6
7
8
9
10
11
A
B
C
D
E
F
G
H
I
+3V3-SSB
+5V-SSB
7010
LD1117DT33
7011
LD1117DT18
IN
OUT
COM
2100
2101
2102
2103
22u 16V
9100
9101
9102 RES
9103 RES
9104 RES
9105 RES
I100
I101
F100
F101
+1V8
+3V3
AUDIO-DAO
AUDIO-WS
AUDIO-BCK
AUDIO-MCK
5101
5102
5103
5104
30R
2108
2109
2110
2111
22p
RX1A-
RX1A+
RX1B-
RX1B+
RX1C-
RX1C+
RX1CLK-
RX1CLK+
RX1D-
RX1D+
RX1E-
RX1E+
RX2A-
RX2A+
RX2B-
RX2B+
RX2C-
RX2C+
RX2CLK-
RX2CLK+
RX2D-
RX2D+
RX2E-
RX2E+
100R
1F42
FI-RE41S-HF
FROM SSB
SDA-DISP
SCL-DISP
RC
RESET-SYSTEM
BACKLIGHT-IN
3101
3102
2104
2105
2106
2107
100p
2112
100n
+3V3-STANDBY
+12V
9110
RX3A-
RX3A+
RX3B-
RX3B+
RX3C-
RX3C+
RX3CLK-
RX3CLK+
RX3D-
RX3D+
RX3E-
RX3E+
RX4A-
RX4A+
RX4B-
RX4B+
RX4C-
RX4C+
RX4CLK-
RX4CLK+
RX4D-
RX4D+
RX4E-
RX4E+
1F41
FI-RE51S-HF
FROM SSB
3103 313 6299.3
I_18020_079.eps
270808

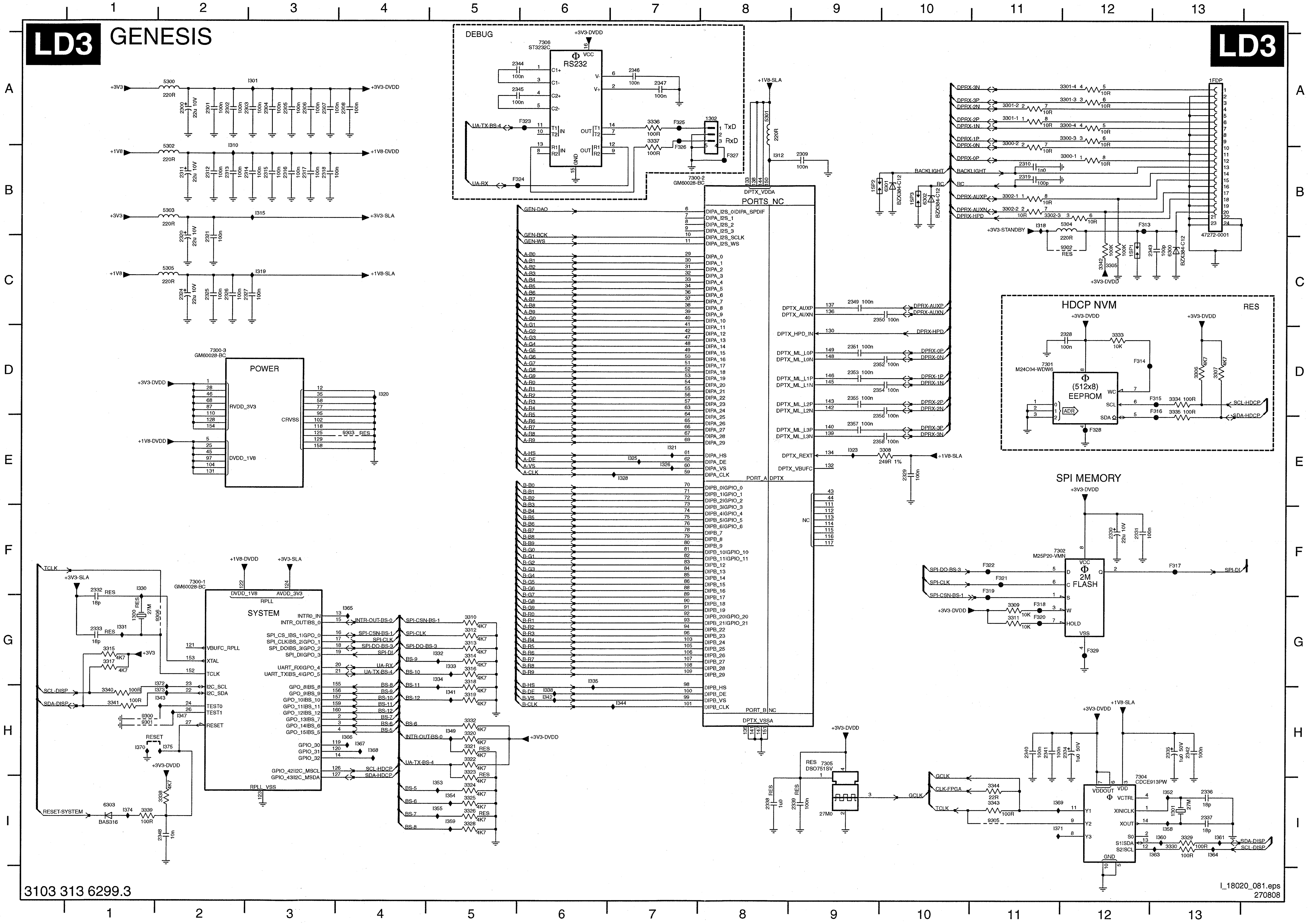
1F41	D11
1F42	E6
2100	A3
2101	B2
2102	B5
2103	C5
2104	E10
2105	E9
2106	E10
2107	E10
2108	D5
2109	D5
2110	D5
2111	D5
2112	D10
3101	D8
3102	D8
3103	E2
3104	E7
3105	E2
3106	E7
3107	E2
3108	E7
3109	F2
3110	F7
3111	F2
3112	F7
3113	F2
3114	F7
3115	G2
3116	G7
3117	G2
3118	G7
3119	G2
3120	G7
3121	H2
3122	H7
3123	H2
3124	H7
3125	I2
3126	I7
3127	I2
3128	I7
5101	D4
5102	D3
5103	D4
5104	D3
7010	B3
7011	B5
9100	A4
9101	A4
9102	B4
9103	B4
9104	B3
9105	C3
9106	G2
9107	G7
9108	G2
9109	G7
9110	H10
F100	A4
F101	B5
F102	D8
F103	D8
F104	D4
F105	D8
F106	D4
F107	D8
F108	D4
F109	D8
F110	D4
F111	D3
F112	D7
F113	D10
F114	E10
F115	E3
F116	E7
F117	E10
F118	E10
F119	E7
F120	E3
F121	E10
F122	E3
F123	E7
F124	E5
F125	E7
F126	E3
F127	E5
F128	E3
F129	E7
F130	F7
F131	F3
F132	F5
F133	F3
F134	F7
F135	F7
F136	F3
F137	F3
F138	F7
F139	F7
F140	F3
F141	G3
F142	G7
F143	G7
F144	G3
F145	G3
F146	G7
F147	G7
F148	G3
F149	G3
F150	G7
F151	G10
F152	G7
F153	G3
F154	G10
F155	H3
F156	H7
F157	H10
F158	H10
F159	H7
F160	H3
F161	H3
F162	H7
F163	H5
F164	H5
F165	H7
F166	H3
F167	H3
F168	H7
F169	H7
F170	H3
F171	I3
F172	I7
F173	I6
F174	I7
F175	I3
F176	I3
F177	I7
I100	B3
I101	B4
I102	D3
I103	D7
I104	D3
I105	D3
I106	D7
I107	D3

LVDS2DP Panel: FPGA: I/O Banks


LD2
FPGA: I/O BANKS
LD2
7205-6
EP2C5F256C7N
POWER
7205-3
EP2C5F256C7N
BANK2
7205-2
EP2C5F256C7N
BANK1
7205-5
EP2C5F256C7N
BANK4
7205-4
EP2C5F256C7N
BANK3
7205-1
EP2C5F256C7N
CONTROL
7205-7
EP2C5F256C7N
NC
+2V5-L51
+3V3-FPGA
+2V5-L41
+1V2-FPGA
+1V2-PLL
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCINT
VCCA_PLL
VCCD_PLL
GND
GND_PLL1
GND_PLL2
GNDA_PLL
3103 313 6299.3
I_18020_080.eps
080908

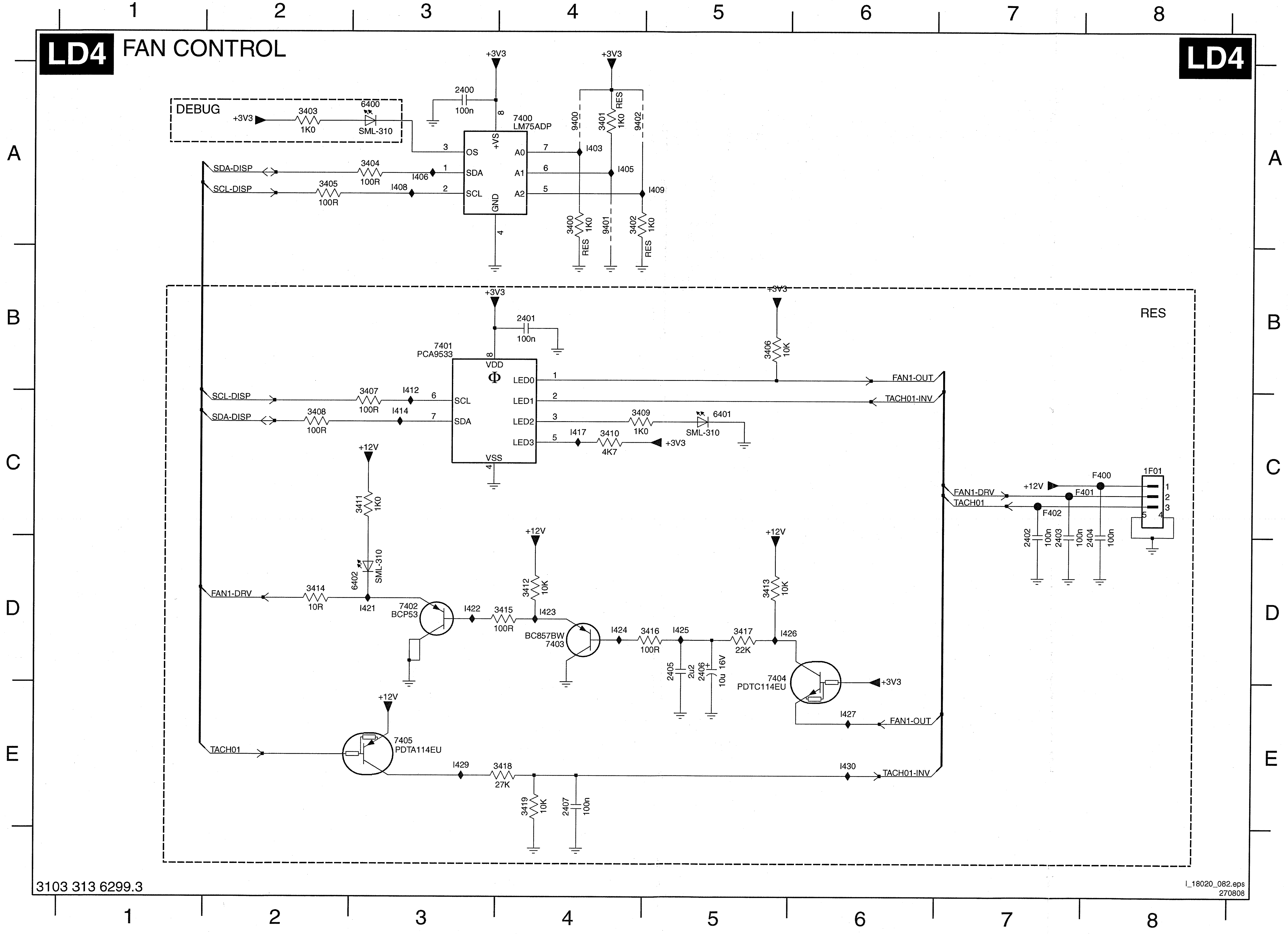
3200	E4
3201	C8
3202	C8
3203	F4
3204	B10
3205	C10
3207	F1
3208	C13
3209	E13
7205-1	E2
7205-2	B11
7205-3	B7
7205-4	D11
7205-5	D7
7205-6	A2
7205-7	F11
9200	F3
9201	F3
F200	C8
F201	C8
F202	C12
F203	E12
F204	E12
F205	E12
F206	E8
F207	E8
I201	C12
I202	E12
I203	F3
I204	F3

LVDS2DP Panel: Genesis



1301	I13
1302	A8
1FDP	A13
1SP1	C12
1SP2	B9
1SP3	B10
2300	A2
2301	A2
2302	A2
2303	A3
2304	A3
2305	A3
2306	A3
2307	A3
2308	A4
2309	B9
2310	B11
2311	B2
2312	B2
2313	B2
2314	B3
2315	B3
2316	B3
2317	B3
2318	B3
2319	B11
2320	C2
2321	C2
2324	C2
2325	C2
2326	C2
2327	C3
2328	D12
2329	E10
2330	F12
2331	F12
2332	F1
2333	G1
2334	H12
2335	H13
2336	I13
2337	I13
2338	I8
2339	I9
2340	H11
2341	H11
2342	H13
2343	C13
2344	A5
2345	A5
2346	A7
2347	A7
2348	I2
2349	C9
2350	C9
2351	D9
2352	D9
2353	D9
2354	D9
2355	D9
2356	D9
2357	E9
2358	E9
3300-1	B12
3300-2	A11
3300-3	A12
3300-4	A12
3301-1	A11
3301-2	A11
3301-3	A12
3301-4	A12
3302-1	B11
3302-2	B11
3302-3	B11
3305	C12
3306	D13
3307	D13
3308	E10
3309	G11
3310	G5
3311	G11
3312	G5
3313	G5
3314	G5
3315	G1
3316	G5
3317	G1
3318	G5
3319	H5
3320	H5
3321	H5
3322	H5
3323	H5
3324	I5
3325	I5
3326	I5
3328	I5
3329	I13
3330	I13
3332	H5
3333	D12
3334	D13
3335	D13
3336	A7
3337	A7
3338	I2
3339	I1
3340	H1
3341	H1
3342	C12
3343	I11
3344	I11
5300	A2
5301	A8
5302	B2
5304	B12
5305	C2
6300	C13
6301	B10
6302	B10
6303	I1
7300-1	F2
7300-2	B8
7300-3	D2
7301	D11
7302	F12
7304	I12
7305	H9
7306	A6
9300	H1
9301	H1
9302	C12
9303	E4
9305	I11
9306	G2
F313	B12
F314	D12
F315	D13
F316	D13
F317	F13
F318	G11
F319	F11
F320	G11
F321	F11
F322	F11
F323	A6
F324	B5
F325	A7
F326	B7
F327	B8
F328	E12
F329	G12
I301	A3
I310	A2
I312	B8
I315	B3
I318	B11
I319	C3
I320	D4
I321	E7
I323	E9
I325	E7
I326	E7
I328	E7
I330	F1
I331	G1
I332	G5
I333	G5
I334	G5
I335	G6
I338	H6
I341	H5
I342	H6
I343	H2
I344	H7
I347	H2
I349	H5
I352	I13
I353	I5
I354	I5
I355	I5
I358	I13
I359	I5
I360	I13
I361	I13
I363	I13
I364	I13
I365	G4
I366	H4
I367	H4
I368	H4
I369	I11
I370	H1
I371	I11
I372	G2
I373	H2
I374	I1
I375	H2

LVDS2DP Panel: Fan Control


LD4
FAN CONTROL
LD4
1 2 3 4 5 6 7 8
A B C D E
DEBUG
+3V3
3403
1K0
6400
SML-310
2400
100n
+3V3
8
7400
LM75ADP
OS
SDA
SCL
+VS
GND
A0
A1
A2
3
1
2
7
6
5
4
SDA-DISP
SCL-DISP
3404
100R
3405
100R
I406
I408
I403
I405
I409
9400
3401
1K0
RES
9402
3400
1K0
RES
9401
3402
1K0
RES
RES
+3V3
2401
100n
7401
PCA9533
VDD
VSS
SCL
SDA
LED0
LED1
LED2
LED3
3406
10K
FAN1-OUT
TACH01-INV
SCL-DISP
SDA-DISP
3407
100R
I412
3408
100R
I414
3409
1K0
6401
SML-310
I417
3410
4K7
+3V3
+12V
3411
1K0
6402
SML-310
FAN1-DRV
3414
10R
I421
7402
BCP53
I422
3415
100R
+12V
3412
10K
I423
BC857BW
7403
I424
3416
100R
I425
3417
22K
+12V
3413
10K
I426
2405
2u2
2406
10u 16V
7404
PDTC114EU
+3V3
I427
FAN1-OUT
+12V
7405
PDTA114EU
TACH01
I429
3418
27K
3419
10K
2407
100n
I430
TACH01-INV
FAN1-DRV
TACH01
+12V
F400
F401
F402
1F01
1 2 3 4 5
2402
100n
2403
100n
2404
100n
3103 313 6299.3
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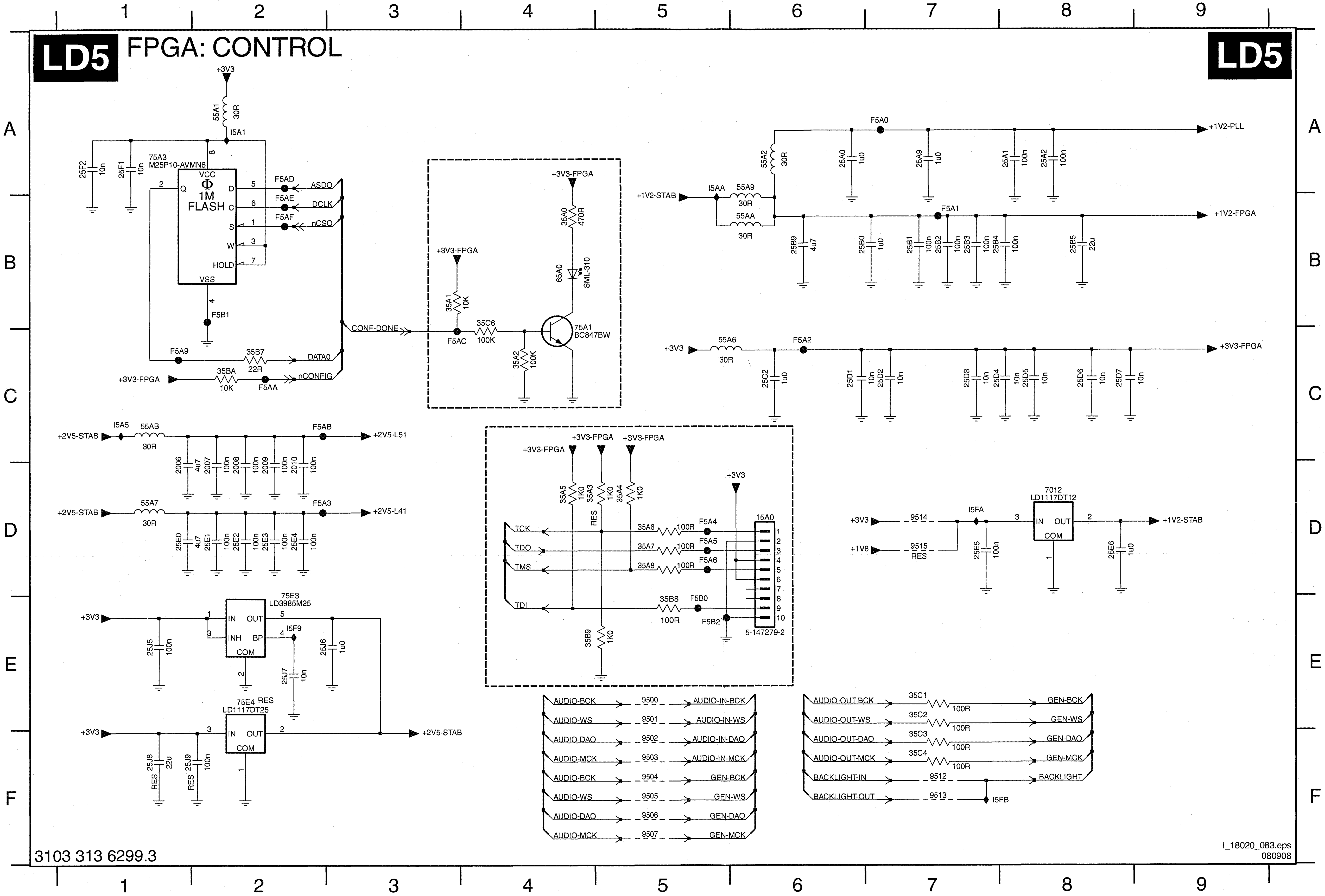
270808

1F01	C8
2400	A3
2401	B4
2402	C7
2403	C7
2404	C8
2405	D5
2406	D5
2407	E4
3400	A4
3401	A4
3402	A4
3403	A2
3404	A3
3405	A2
3406	B5
3407	C3
3408	C2
3409	C4
3410	C4
3411	C3
3412	D4
3413	D5
3414	D2
3415	D4
3416	D5
3417	D5
3418	E4
3419	E4
6400	A3
6401	C5
6402	D3
7400	A4
7401	B3
7402	D3
7403	D4
7404	D5
7405	E3
9400	A4
9401	A4
9402	A4
F400	C8
F401	C8
F402	C7
I403	A4
I405	A4
I406	A3
I408	A3
I409	A5
I412	B3
I414	C3
I417	C4
I421	D3
I422	D3
I423	D4
I424	D4
I425	D5
I426	D5
I427	E6
I429	E3
I430	E6

LVDS2DP Panel: FPGA: Control


LD5
FPGA: CONTROL
LD5
1 2 3 4 5 6 7 8 9
A B C D E F
+3V3
55A1 30R
I5A1
25F2 10n
25F1 10n
75A3 M25P10-AVMN6
VCC
Φ
1M
FLASH
VSS
Q D C S W HOLD
F5AD ASDO
F5AE DCLK
F5AF nCSO
F5B1
CONF-DONE
F5A9 35B7 22R DATA0
+3V3-FPGA 35BA 10K F5AA nCONFIG
+3V3-FPGA
35A0 470R
65A0 SML-310
35A1 10K
35C6 100K
F5AC
35A2 100K
75A1 BC847BW
+1V2-STAB
I5AA
55A9 30R
55AA 30R
55A2 30R
F5A0
25A0 1u0
25A9 1u0
25A1 100n
25A2 100n
+1V2-PLL
F5A1
+1V2-FPGA
25B9 4u7
25B0 1u0
25B1 100n
25B2 100n
25B3 100n
25B4 100n
25B5 22u
+3V3
55A6 30R
F5A2
+3V3-FPGA
25C2 1u0
25D1 10n
25D2 10n
25D3 10n
25D4 10n
25D5 10n
25D6 10n
25D7 10n
+2V5-STAB I5A5 55AB 30R F5AB +2V5-L51
2006 4u7
2007 100n
2008 100n
2009 100n
2010 100n
+2V5-STAB 55A7 30R F5A3 +2V5-L41
25E0 4u7
25E1 100n
25E2 100n
25E3 100n
25E4 100n
+3V3
75E3 LD3985M25
IN OUT INH BP COM
I5F9
25J5 100n
25J6 1u0
25J7 10n
+3V3
75E4 RES LD1117DT25
IN OUT COM
+2V5-STAB
25J8 22u RES
25J9 100n RES
+3V3-FPGA
35A5 1K0
35A3 1K0 RES
35A4 1K0
+3V3
TCK TDO TMS TDI
35A6 100R F5A4
35A7 100R F5A5
35A8 100R F5A6
35B8 100R F5B0
F5B2
15A0
5-147279-2
35B9 1K0
7012 LD1117DT12
+3V3 9514
+1V8 9515 RES
I5FA
25E5 100n
IN OUT COM
25E6 1u0
+1V2-STAB
AUDIO-BCK 9500 AUDIO-IN-BCK
AUDIO-WS 9501 AUDIO-IN-WS
AUDIO-DAO 9502 AUDIO-IN-DAO
AUDIO-MCK 9503 AUDIO-IN-MCK
AUDIO-BCK 9504 GEN-BCK
AUDIO-WS 9505 GEN-WS
AUDIO-DAO 9506 GEN-DAO
AUDIO-MCK 9507 GEN-MCK
AUDIO-OUT-BCK 35C1 100R GEN-BCK
AUDIO-OUT-WS 35C2 100R GEN-WS
AUDIO-OUT-DAO 35C3 100R GEN-DAO
AUDIO-OUT-MCK 35C4 100R GEN-MCK
BACKLIGHT-IN 9512 BACKLIGHT
BACKLIGHT-OUT 9513 I5FB
3103 313 6299.3
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080908

15A0	D6
2006	D1
2007	D2
2008	D2
2009	D2
2010	D2
25A0	A6
25A1	A8
25A2	A8
25A9	A7
25B0	B6
25B1	B7
25B2	B7
25B3	B7
25B4	B7
25B5	B8
25B9	B6
25C2	C6
25D1	C6
25D2	C7
25D3	C7
25D4	C7
25D5	C8
25D6	C8
25D7	C8
25E0	D1
25E1	D2
25E2	D2
25E3	D2
25E4	D2
25E5	D7
25E6	D8
25F1	A1
25F2	A1
25J5	E1
25J6	E2
25J7	E2
25J8	F1
25J9	F1
35A0	B4
35A1	B3
35A2	C4
35A3	D4
35A4	D5
35A5	D4
35A6	D5
35A7	D5
35A8	D5
35B7	C2
35B8	E5
35B9	E4
35BA	C2
35C1	E7
35C2	E7
35C3	F7
35C4	F7
35C6	B4
55A1	A2
55A2	A6
55A6	C5
55A7	D1
55A9	A6
55AA	B6
55AB	C1
65A0	B4
7012	D8
75A1	C4
75A3	A1
75E3	E2
75E4	E2
9500	E5
9501	E5
9502	F5
9503	F5
9504	F5
9505	F5
9506	F5
9507	F5
9512	F7
9513	F7
9514	D7
9515	D7
F5A0	A7
F5A1	B7
F5A2	C6
F5A3	D2
F5A4	D5
F5A5	D5
F5A6	D5
F5A9	C1
F5AA	C2
F5AB	C2
F5AC	C3
F5AD	A2
F5AE	B2
F5AF	B2
F5B0	E5
F5B1	B2
F5B2	E5
I5A1	A2
I5A5	C1
I5AA	A5
I5F9	E2
I5FA	D7
I5FB	F8

LVDS2DP: SRP List

Netname	Diagram
+12V	LD1
+12V	LD4
+1V2-FPGA	LD2
+1V2-FPGA	LD5
+1V2-PLL	LD2
+1V2-PLL	LD5
+1V2-STAB	LD5
+1V8	LD1
+1V8	LD3
+1V8	LD5
+1V8-DVDD	LD3
+1V8-SLA	LD3
+2V5-L41	LD2
+2V5-L41	LD5
+2V5-L51	LD2
+2V5-L51	LD5
+2V5-STAB	LD5
+3V3	LD1
+3V3	LD3
+3V3	LD4
+3V3	LD5
+3V3-DVDD	LD3
+3V3-FPGA	LD2
+3V3-FPGA	LD5
+3V3-SLA	LD3
+3V3-SSB	LD1
+3V3-STANDBY	LD1
+3V3-STANDBY	LD3
+5V-SSB	LD1
A-B0	LD2 (1x)
A-B0	LD3 (1x)
A-B1	LD2 (1x)
A-B1	LD3 (1x)
A-B2	LD2 (1x)
A-B2	LD3 (1x)
A-B3	LD2 (1x)
A-B3	LD3 (1x)
A-B4	LD2 (1x)
A-B4	LD3 (1x)
A-B5	LD2 (1x)
A-B5	LD3 (1x)
A-B6	LD2 (1x)
A-B6	LD3 (1x)
A-B7	LD2 (1x)
A-B7	LD3 (1x)
A-B8	LD2 (1x)
A-B8	LD3 (1x)
A-B9	LD2 (1x)
A-B9	LD3 (1x)
A-CLK	LD2 (1x)
A-CLK	LD3 (1x)
A-DE	LD2 (1x)
A-DE	LD3 (1x)
A-G0	LD2 (1x)
A-G0	LD3 (1x)
A-G1	LD2 (1x)
A-G1	LD3 (1x)
A-G2	LD2 (1x)
A-G2	LD3 (1x)
A-G3	LD2 (1x)
A-G3	LD3 (1x)
A-G4	LD2 (1x)
A-G4	LD3 (1x)
A-G5	LD2 (1x)
A-G5	LD3 (1x)
A-G6	LD2 (1x)
A-G6	LD3 (1x)
A-G7	LD2 (1x)
A-G7	LD3 (1x)
A-G8	LD2 (1x)
A-G8	LD3 (1x)
A-G9	LD2 (1x)
A-G9	LD3 (1x)
A-HS	LD2 (1x)
A-HS	LD3 (1x)
A-R0	LD2 (1x)
A-R0	LD3 (1x)
A-R1	LD2 (1x)
A-R1	LD3 (1x)
A-R2	LD2 (1x)
A-R2	LD3 (1x)
A-R3	LD2 (1x)
A-R3	LD3 (1x)
A-R4	LD2 (1x)
A-R4	LD3 (1x)
A-R5	LD2 (1x)
A-R5	LD3 (1x)
A-R6	LD2 (1x)
A-R6	LD3 (1x)
A-R7	LD2 (1x)
A-R7	LD3 (1x)
A-R8	LD2 (1x)
A-R8	LD3 (1x)
A-R9	LD2 (1x)
A-R9	LD3 (1x)
ASDO	LD2 (1x)
ASDO	LD5 (1x)
AUDIO-BCK	LD1 (1x)
AUDIO-BCK	LD5 (2x)
AUDIO-DAO	LD1 (1x)
AUDIO-DAO	LD5 (2x)
AUDIO-IN-BCK	LD2 (1x)
AUDIO-IN-BCK	LD5 (1x)
AUDIO-IN-DAO	LD2 (1x)
AUDIO-IN-DAO	LD5 (1x)
AUDIO-IN-MCK	LD2 (1x)
AUDIO-IN-MCK	LD5 (1x)
AUDIO-IN-WS	LD2 (1x)
AUDIO-IN-WS	LD5 (1x)
AUDIO-MCK	LD1 (1x)
AUDIO-MCK	LD5 (2x)
AUDIO-OUT-BCK	LD2 (1x)
AUDIO-OUT-BCK	LD5 (1x)
AUDIO-OUT-DAO	LD2 (1x)
AUDIO-OUT-DAO	LD5 (1x)
AUDIO-OUT-MCK	LD2 (1x)
AUDIO-OUT-MCK	LD5 (1x)
AUDIO-OUT-WS	LD2 (1x)
AUDIO-OUT-WS	LD5 (1x)
AUDIO-WS	LD1 (1x)
AUDIO-WS	LD5 (2x)
A-VS	LD2 (1x)
A-VS	LD3 (1x)
BACKLIGHT	LD3 (1x)
BACKLIGHT	LD5 (1x)
BACKLIGHT-IN	LD1 (1x)
BACKLIGHT-IN	LD2 (1x)
BACKLIGHT-IN	LD5 (1x)
BACKLIGHT-OUT	LD2 (1x)
BACKLIGHT-OUT	LD5 (1x)
B-B0	LD2 (1x)
B-B0	LD3 (1x)
B-B1	LD2 (1x)
B-B1	LD3 (1x)
B-B2	LD2 (1x)
B-B2	LD3 (1x)
B-B3	LD2 (1x)
B-B3	LD3 (1x)
B-B4	LD2 (1x)
B-B4	LD3 (1x)
B-B5	LD2 (1x)
B-B5	LD3 (1x)
B-B6	LD2 (1x)
B-B6	LD3 (1x)
B-B7	LD2 (1x)
B-B7	LD3 (1x)
B-B8	LD2 (1x)
B-B8	LD3 (1x)
B-B9	LD2 (1x)
B-B9	LD3 (1x)
B-CLK	LD2 (1x)
B-CLK	LD3 (1x)
B-DE	LD2 (1x)
B-DE	LD3 (1x)
B-G0	LD2 (1x)
B-G0	LD3 (1x)
B-G1	LD2 (1x)
B-G1	LD3 (1x)
B-G2	LD2 (1x)
B-G2	LD3 (1x)
B-G3	LD2 (1x)
B-G3	LD3 (1x)
B-G4	LD2 (1x)
B-G4	LD3 (1x)
B-G5	LD2 (1x)
B-G5	LD3 (1x)
B-G6	LD2 (1x)
B-G6	LD3 (1x)
B-G7	LD2 (1x)
B-G7	LD3 (1x)
B-G8	LD2 (1x)
B-G8	LD3 (1x)
B-G9	LD2 (1x)
B-G9	LD3 (1x)
B-HS	LD2 (1x)
B-HS	LD3 (1x)
B-R0	LD2 (1x)
B-R0	LD3 (1x)
B-R1	LD2 (1x)
B-R1	LD3 (1x)
B-R2	LD2 (1x)
B-R2	LD3 (1x)
B-R3	LD2 (1x)
B-R3	LD3 (1x)
B-R4	LD2 (1x)
B-R4	LD3 (1x)
B-R5	LD2 (1x)
B-R5	LD3 (1x)
B-R6	LD2 (1x)
B-R6	LD3 (1x)
B-R7	LD2 (1x)
B-R7	LD3 (1x)
B-R8	LD2 (1x)
B-R8	LD3 (1x)
B-R9	LD2 (1x)
B-R9	LD3 (1x)
BS-10	LD3 (1x)
BS-11	LD3 (1x)
BS-12	LD3 (1x)
BS-5	LD3 (1x)
BS-6	LD3 (1x)
BS-7	LD3 (1x)
BS-8	LD3 (1x)
BS-9	LD3 (1x)
B-VS	LD2 (1x)
B-VS	LD3 (1x)
CLK-FPGA	LD2 (1x)
CLK-FPGA	LD3 (1x)
CONF-DONE	LD2 (1x)
CONF-DONE	LD5 (1x)
DATA0	LD2 (1x)
DATA0	LD5 (1x)
DCLK	LD2 (1x)
DCLK	LD5 (1x)
DPRX-0N	LD3 (2x)
DPRX-0P	LD3 (2x)
DPRX-1N	LD3 (2x)
DPRX-1P	LD3 (2x)
DPRX-2N	LD3 (2x)
DPRX-2P	LD3 (2x)
DPRX-3N	LD3 (2x)
DPRX-3P	LD3 (2x)
DPRX-AUXN	LD3 (2x)
DPRX-AUXP	LD3 (2x)
DPRX-HPD	LD3 (2x)
FAN1-DRV	LD4 (2x)
FAN1-OUT	LD4 (2x)
GCLK	LD3 (2x)
GEN-BCK	LD3 (1x)
GEN-BCK	LD5 (2x)
GEN-DAO	LD3 (1x)
GEN-DAO	LD5 (2x)
GEN-MCK	LD5 (2x)
GEN-WS	LD3 (1x)
GEN-WS	LD5 (2x)
INTR-OUT-BS-0	LD3 (1x)
nCONFIG	LD2 (1x)
nCONFIG	LD5 (1x)
nCSO	LD2 (1x)
nCSO	LD5 (1x)
RC	LD1 (1x)
RC	LD3 (1x)
RESET-SYSTEM	LD1 (1x)
RESET-SYSTEM	LD3 (1x)
RX1A-	LD1 (1x)
RX1A-	LD2 (1x)
RX1A+	LD1 (1x)
RX1A+	LD2 (1x)
RX1B-	LD1 (1x)
RX1B-	LD2 (1x)
RX1B+	LD1 (1x)
RX1B+	LD2 (1x)
RX1C-	LD1 (1x)
RX1C-	LD2 (1x)
RX1C+	LD1 (1x)
RX1C+	LD2 (1x)
RX1CLK-	LD1 (1x)
RX1CLK-	LD2 (1x)
RX1CLK+	LD1 (1x)
RX1CLK+	LD2 (1x)
RX1D-	LD1 (1x)
RX1D-	LD2 (1x)
RX1D+	LD1 (1x)
RX1D+	LD2 (1x)
RX1E-	LD1 (1x)
RX1E-	LD2 (1x)
RX1E+	LD1 (1x)
RX1E+	LD2 (1x)
RX2A-	LD1 (1x)
RX2A-	LD2 (1x)
RX2A+	LD1 (1x)
RX2A+	LD2 (1x)
RX2B-	LD1 (1x)
RX2B-	LD2 (1x)
RX2B+	LD1 (1x)
RX2B+	LD2 (1x)
RX2C-	LD1 (1x)
RX2C-	LD2 (1x)
RX2C+	LD1 (1x)
RX2C+	LD2 (1x)
RX2CLK-	LD1 (1x)
RX2CLK-	LD2 (1x)
RX2CLK+	LD1 (1x)
RX2CLK+	LD2 (1x)
RX2D-	LD1 (1x)
RX2D-	LD2 (1x)
RX2D+	LD1 (1x)
RX2D+	LD2 (1x)
RX2E-	LD1 (1x)
RX2E-	LD2 (1x)
RX2E+	LD1 (1x)
RX2E+	LD2 (1x)
RX3A-	LD1 (1x)
RX3A-	LD2 (1x)
RX3A+	LD1 (1x)
RX3A+	LD2 (1x)
RX3B-	LD1 (1x)
RX3B-	LD2 (1x)
RX3B+	LD1 (1x)
RX3B+	LD2 (1x)
RX3C-	LD1 (1x)
RX3C-	LD2 (1x)
RX3C+	LD1 (1x)
RX3C+	LD2 (1x)
RX3CLK-	LD1 (1x)
RX3CLK-	LD2 (1x)
RX3CLK+	LD1 (1x)
RX3CLK+	LD2 (1x)
RX3D-	LD1 (1x)
RX3D-	LD2 (1x)
RX3D+	LD1 (1x)
RX3D+	LD2 (1x)
RX3E-	LD1 (1x)
RX3E-	LD2 (1x)
RX3E+	LD1 (1x)
RX3E+	LD2 (1x)
RX4A-	LD1 (1x)
RX4A-	LD2 (1x)
RX4A+	LD1 (1x)
RX4A+	LD2 (1x)
RX4B-	LD1 (1x)
RX4B-	LD2 (1x)
RX4B+	LD1 (1x)
RX4B+	LD2 (1x)
RX4C-	LD1 (1x)
RX4C-	LD2 (1x)
RX4C+	LD1 (1x)
RX4C+	LD2 (1x)
RX4CLK-	LD1 (1x)
RX4CLK-	LD2 (1x)
RX4CLK+	LD1 (1x)
RX4CLK+	LD2 (1x)
RX4D-	LD1 (1x)
RX4D-	LD2 (1x)
RX4D+	LD1 (1x)
RX4D+	LD2 (1x)
RX4E-	LD1 (1x)
RX4E-	LD2 (1x)
RX4E+	LD1 (1x)
RX4E+	LD2 (1x)
SCL-DISP	LD1 (1x)
SCL-DISP	LD2 (1x)
SCL-DISP	LD3 (2x)
SCL-DISP	LD4 (2x)
SCL-HDCP	LD3 (2x)
SDA-DISP	LD1 (1x)
SDA-DISP	LD2 (1x)
SDA-DISP	LD3 (2x)
SDA-DISP	LD4 (2x)
SDA-HDCP	LD3 (2x)
SPI-CLK	LD3 (2x)
SPI-CSN-BS-1	LD3 (2x)
SPI-DI	LD3 (2x)
SPI-DO-BS-3	LD3 (2x)
TACH01	LD4 (2x)
TACH01-INV	LD4 (2x)
TCK	LD2 (1x)
TCK	LD5 (1x)
TCLK	LD3 (2x)
TDI	LD2 (1x)
TDI	LD5 (1x)
TDO	LD2 (1x)
TDO	LD5 (1x)
TMS	LD2 (1x)
TMS	LD5 (1x)
UA-RX	LD3 (2x)
UA-TX-BS-4	LD3 (2x)

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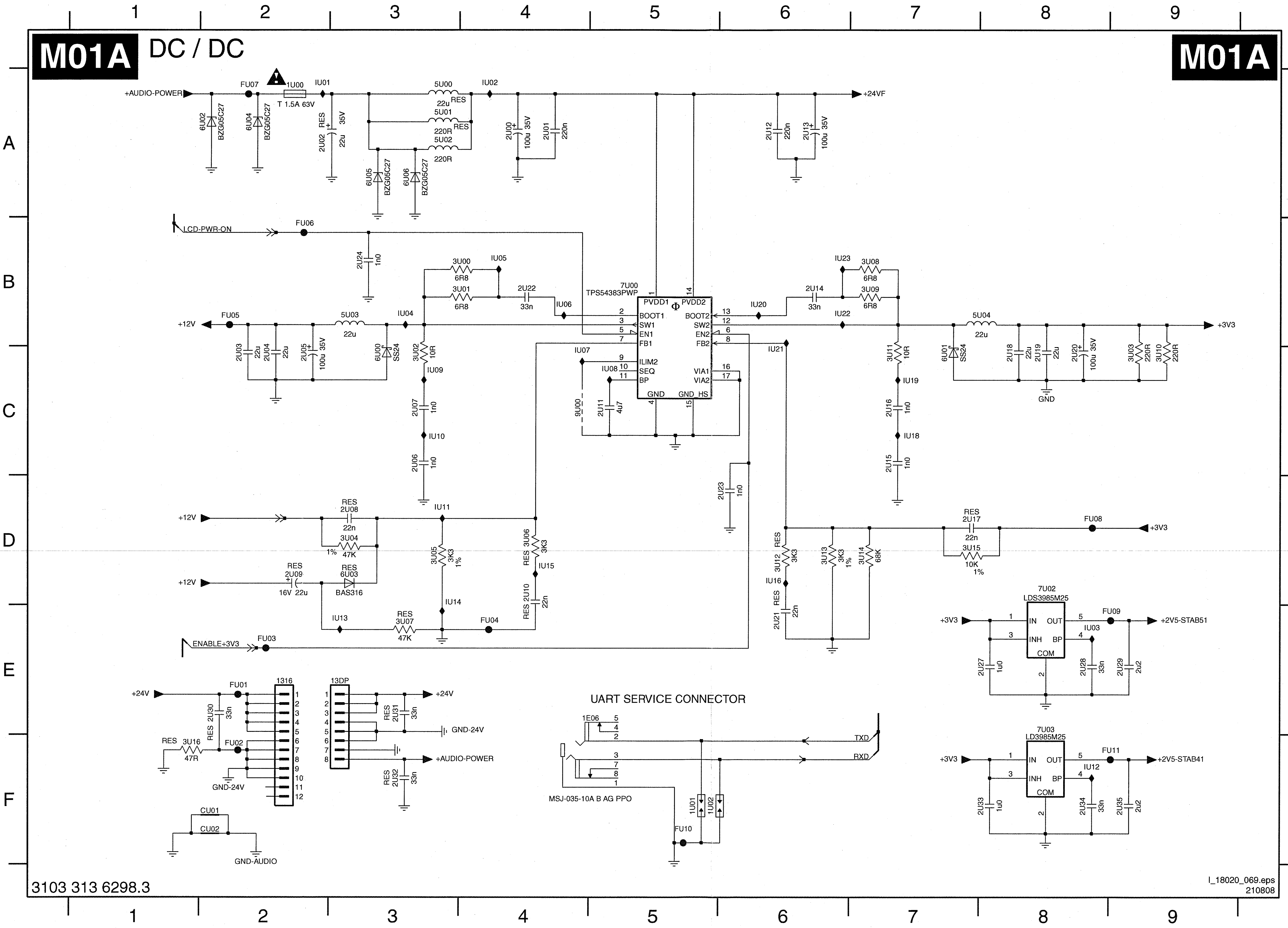
PHIL-06076 / DRUCK:83

Monitor Panel: DC/DC


M01A
DC / DC
+AUDIO-POWER
FU07
1U00
T 1.5A 63V
IU01
5U00
22u
RES
IU02
5U01
220R
5U02
+24VF
6U02 BZG05C27
6U04 BZG05C27
2U02 22u 35V
6U05 BZG05C27
6U06 BZG05C27
2U00 100u 35V
2U01 220n
2U12 220n
2U13 100u 35V
LCD-PWR-ON
FU06
2U24 1n0
3U00 6R8
IU05
3U01 6R8
2U22 33n
IU06
7U00
TPS54383PWP
PVDD1
PVDD2
BOOT1
SW1
EN1
FB1
ILIM2
SEQ
BP
GND
GND_HS
BOOT2
SW2
EN2
FB2
VIA1
VIA2
IU20
2U14 33n
IU23
3U08 6R8
3U09 6R8
IU22
5U04 22u
+3V3
+12V
FU05
5U03 22u
IU04
2U03 22u
2U04 22u
2U05 100u 35V
6U00 SS24
3U02 10R
IU09
IU07
IU08
9U00
2U11 4u7
IU21
3U11 10R
IU19
6U01 SS24
2U18 22u
2U19 22u
2U20 100u 35V
3U03 220R
3U10 220R
GND
2U07 1n0
IU10
2U06 1n0
2U16 1n0
IU18
2U15 1n0
2U23 1n0
RES
2U08 22n
IU11
3U04 47K 1%
3U05 3K3 1%
3U06 3K3
IU15
2U09 16V 22u
6U03 BAS316
2U10 22n
IU14
IU13
3U07 47K
FU04
ENABLE+3V3
FU03
2U17 22n
FU08
3U15 10K 1%
3U12 3K3
IU16
2U21 22n
3U13 3K3 1%
3U14 68K
7U02
LD3985M25
IN
OUT
INH
BP
COM
FU09
IU03
+2V5-STAB51
2U27 1u0
2U28 33n
2U29 2u2
7U03
LD3985M25
FU11
IU12
+2V5-STAB41
2U33 1u0
2U34 33n
2U35 2u2
+24V
FU01
1316
2U30 33n
3U16 47R
FU02
GND-24V
13DP
2U31 33n
2U32 33n
UART SERVICE CONNECTOR
1E06
TXD
RXD
MSJ-035-10A B AG PPO
1U01
1U02
FU10
CU01
CU02
GND-AUDIO
3103 313 6298.3
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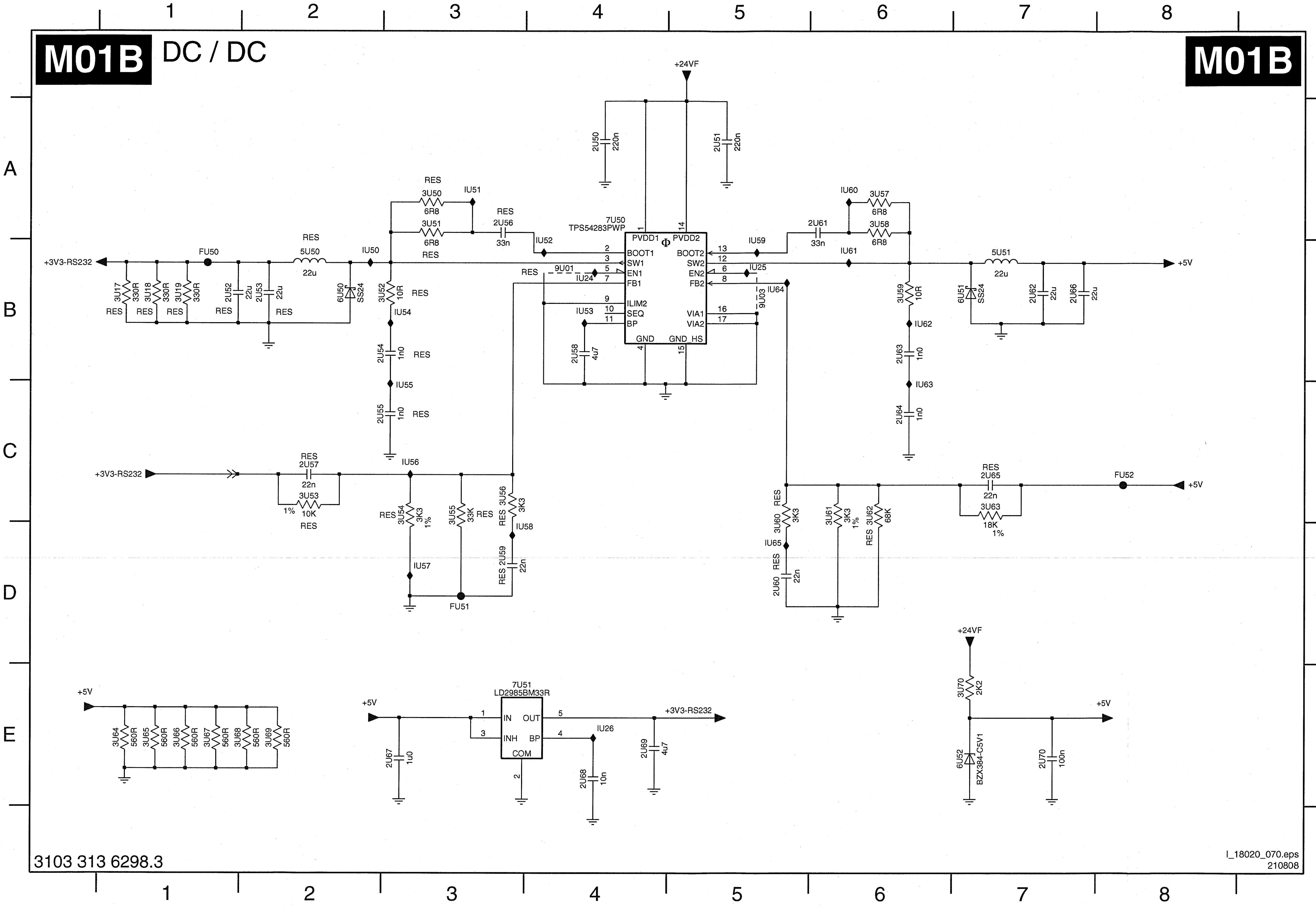
1316	E2
13DP	E3
1E06	E5
1U00	A2
1U01	F5
1U02	F5
2U00	A4
2U01	A4
2U02	A2
2U03	C2
2U04	C2
2U05	C2
2U06	C3
2U07	C3
2U08	D3
2U09	D2
2U10	D4
2U11	C5
2U12	A6
2U13	A6
2U14	B6
2U15	C7
2U16	C7
2U17	D7
2U18	C8
2U19	C8
2U20	C8
2U21	E6
2U22	B4
2U23	D6
2U24	B3
2U27	E8
2U28	E8
2U29	E9
2U30	E2
2U31	E3
2U32	F3
2U33	F8
2U34	F8
2U35	F9
3U00	B4
3U01	B4
3U02	C3
3U03	C9
3U04	D3
3U05	D3
3U06	D4
3U07	E3
3U08	B7
3U09	B7
3U10	C9
3U11	C7
3U12	D6
3U13	D6
3U14	D7
3U15	D7
3U16	F1
5U00	A3
5U01	A3
5U02	A3
5U03	B3
5U04	B8
6U00	C3
6U01	C7
6U02	A2
6U03	D3
6U04	A2
6U05	A3
6U06	A3
7U00	B5
7U02	D8
7U03	E8
9U00	C4
CU01	F2
CU02	F2
FU01	E2
FU02	F2
FU03	E2
FU04	E4
FU05	B2
FU06	B2
FU07	A2
FU08	D8
FU09	E9
FU10	F5
FU11	F9
IU01	A2
IU02	A4
IU03	E8
IU04	B3
IU05	B4
IU06	B4
IU07	C4
IU08	C5
IU09	C3
IU10	C3
IU11	D3
IU12	F8
IU13	E3
IU14	D3
IU15	D4
IU16	D6
IU18	C7
IU19	C7
IU20	B6
IU21	C6
IU22	B6
IU23	B6

Monitor Panel: DC/DC


M01B
DC / DC
M01B
+24VF
2U50 220n
2U51 220n
7U50
TPS54283PWP
PVDD1
PVDD2
BOOT1
SW1
EN1
FB1
ILIM2
SEQ
BP
GND
GND_HS
BOOT2
SW2
EN2
FB2
VIA1
VIA2
RES
3U50 6R8
IU51
3U51 6R8
2U56 33n
IU52
IU59
2U61 33n
IU60
3U57 6R8
3U58 6R8
IU61
5U51 22u
+5V
+3V3-RS232
FU50
5U50 22u
IU50
9U01
IU24
IU25
9U03
IU64
3U17 330R
3U18 330R
3U19 330R
2U52 22u
2U53 22u
6U50 SS24
3U52 10R
IU54
2U54 1n0
IU55
2U55 1n0
IU53
2U58 4u7
3U59 10R
IU62
2U63 1n0
IU63
2U64 1n0
6U51 SS24
2U62 22u
2U66 22u
2U57 22n
3U53 10K
1%
IU56
3U54 3K3
3U55 33K
3U56 3K3
IU58
2U59 22n
IU57
FU51
3U60 3K3
IU65
2U60 22n
3U61 3K3
3U62 68K
2U65 22n
3U63 18K
FU52
7U51
LD2985BM33R
IN
OUT
INH
BP
COM
IU26
2U67 1u0
2U68 10n
2U69 4u7
3U64 560R
3U65 560R
3U66 560R
3U67 560R
3U68 560R
3U69 560R
3U70 2K2
6U52 BZX384-C5V1
2U70 100n
1 2 3 4 5 6 7 8
A B C D E

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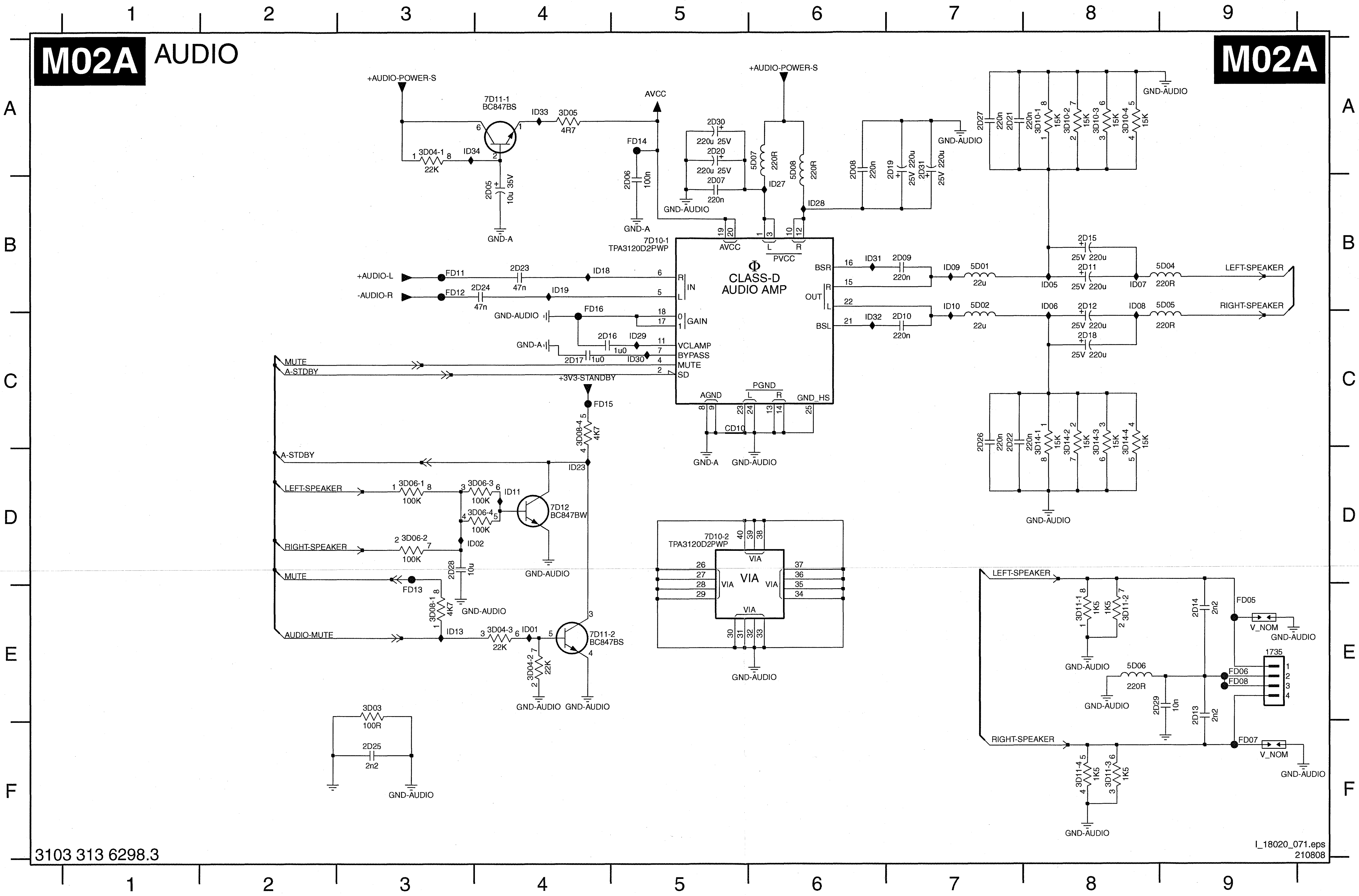
2U50	A4
2U51	A5
2U52	B1
2U53	B2
2U54	B3
2U55	C3
2U56	A3
2U57	C2
2U58	B4
2U59	D3
2U60	D5
2U61	A6
2U62	B7
2U63	B6
2U64	C6
2U65	C7
2U66	B7
2U67	E3
2U68	E4
2U69	E4
2U70	E7
3U17	B1
3U18	B1
3U19	B1
3U50	A3
3U51	A3
3U52	B3
3U53	C2
3U54	C3
3U55	C3
3U56	C3
3U57	A6
3U58	A6
3U59	B6
3U60	D5
3U61	C6
3U62	C6
3U63	C7
3U64	E1
3U65	E1
3U66	E1
3U67	E1
3U68	E2
3U69	E2
3U70	E7
5U50	B2
5U51	B7
6U50	B2
6U51	B7
6U52	E7
7U50	A4
7U51	E3
9U01	B4
9U03	B5
FU50	B1
FU51	D3
FU52	C8
IU24	B4
IU25	B5
IU26	E4
IU50	B2
IU51	A3
IU52	B4
IU53	B4
IU54	B3
IU55	C3
IU56	C3
IU57	D3
IU58	D3
IU59	B5
IU60	A6
IU61	B6
IU62	B6
IU63	C6
IU64	B5
IU65	D5

Monitor Panel: Audio


M02A AUDIO
M02A
+AUDIO-POWER-S
7D11-1
BC847BS
ID33
3D05
4R7
AVCC
3D04-1
22K
ID34
2D05
10u 35V
GND-A
FD14
2D06
100n
2D30
220u 25V
2D20
220u 25V
2D07
220n
GND-AUDIO
5D07
220R
5D08
220R
ID27
ID28
2D08
220n
2D19
25V 220u
2D31
25V 220u
2D27
220n
2D21
220n
3D10-1
3D10-2
3D10-3
3D10-4
15K
7D10-1
TPA3120D2PWP
AVCC
PVCC
Φ
CLASS-D
AUDIO AMP
IN
GAIN
VCLAMP
BYPASS
MUTE
SD
BSR
OUT
BSL
AGND
PGND
GND_HS
+AUDIO-L
-AUDIO-R
FD11
FD12
2D23
47n
2D24
47n
ID18
ID19
FD16
2D16
1u0
ID29
2D17
1u0
ID30
+3V3-STANDBY
FD15
3D08-4
4K7
ID31
2D09
220n
ID32
2D10
220n
ID09
5D01
22u
ID10
5D02
22u
ID05
ID06
2D15
25V 220u
2D11
25V 220u
2D12
25V 220u
2D18
25V 220u
ID07
ID08
5D04
220R
5D05
220R
LEFT-SPEAKER
RIGHT-SPEAKER
CD10
2D26
220n
2D22
220n
3D14-1
3D14-2
3D14-3
3D14-4
15K
MUTE
A-STDBY
ID23
3D06-1
100K
3D06-3
100K
3D06-4
100K
ID11
7D12
BC847BW
3D06-2
100K
ID02
2D28
10u
FD13
3D08-1
4K7
AUDIO-MUTE
ID13
3D04-3
22K
ID01
7D11-2
BC847BS
3D04-2
22K
7D10-2
TPA3120D2PWP
VIA
3D03
100R
2D25
2n2
3D11-1
1K5
3D11-2
1K5
2D14
2n2
FD05
V_NOM
1735
5D06
220R
FD06
FD08
2D29
10n
2D13
2n2
FD07
3D11-4
1K5
3D11-3
1K5
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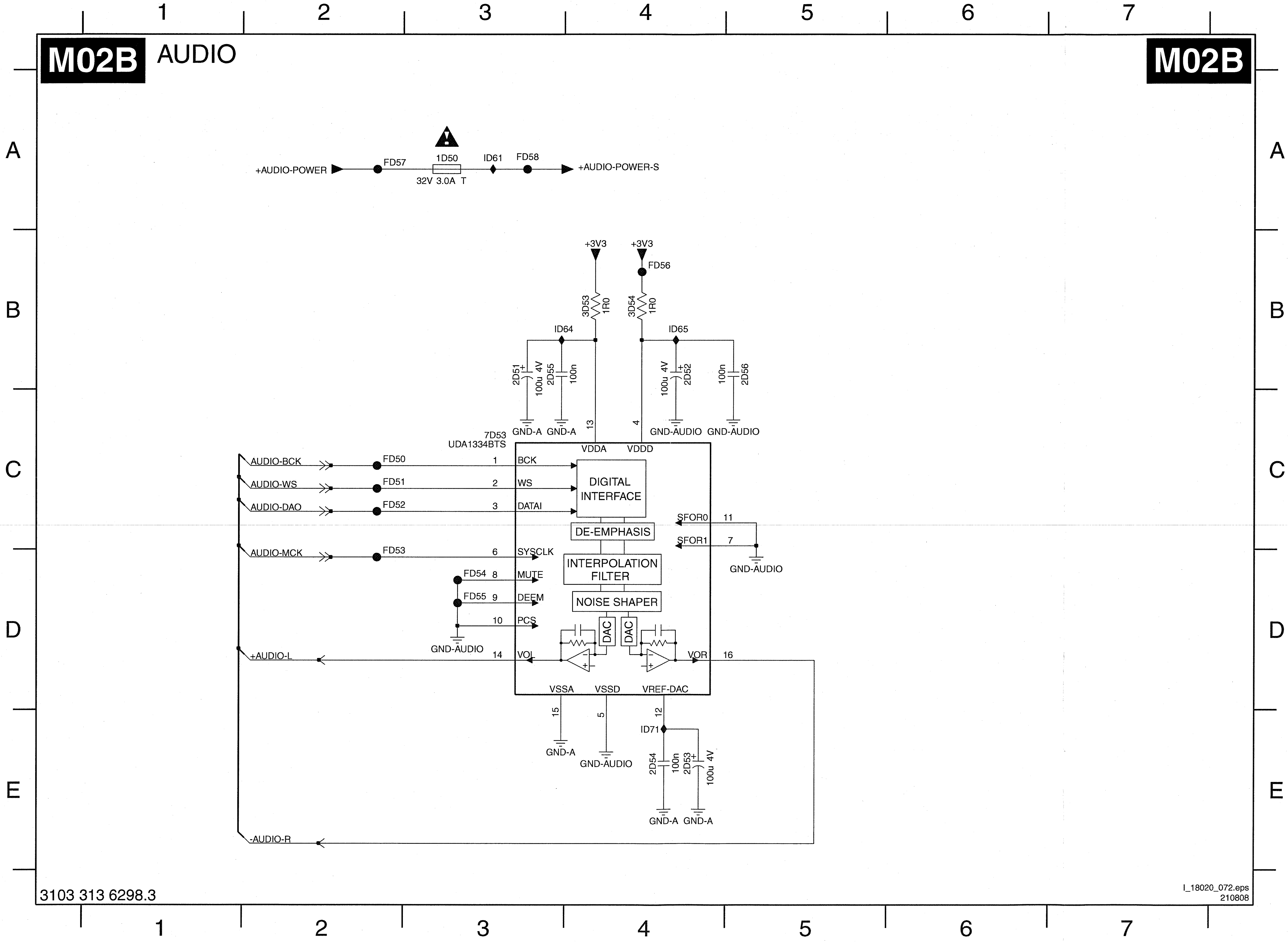
1735 E9
2D05 B4
2D06 B5
2D07 B5
2D08 A6
2D09 B7
2D10 C7
2D11 B8
2D12 B8
2D13 E9
2D14 E9
2D15 B8
2D16 C4
2D17 C4
2D18 C8
2D19 A7
2D20 A5
2D21 A7
2D22 C7
2D23 B4
2D24 B4
2D25 F3
2D26 C7
2D27 A7
2D28 D3
2D29 E8
2D30 A5
2D31 A7
3D03 E3
3D04-1 A3
3D04-2 E4
3D04-3 E4
3D05 A4
3D06-1 D3
3D06-2 D3
3D06-3 D4
3D06-4 D4
3D08-1 E3
3D08-4 C4
3D10-1 A8
3D10-2 A8
3D10-3 A8
3D10-4 A8
3D11-1 E8
3D11-2 E8
3D11-3 F8
3D11-4 F8
3D14-1 C8
3D14-2 C8
3D14-3 C8
3D14-4 C8
5D01 B7
5D02 B7
5D04 B9
5D05 B9
5D06 E8
5D07 A6
5D08 A6
7D10-1 B5
7D10-2 D5
7D11-1 A4
7D11-2 E4
7D12 D4
CD10 C5
FD05 E9
FD06 E9
FD07 F9
FD08 E9
FD11 B3
FD12 B3
FD13 E3
FD14 A5
FD15 C4
FD16 B4
ID01 E4
ID02 D4
ID05 B8
ID06 B8
ID07 B8
ID08 B8
ID09 B7
ID10 B7
ID11 D4
ID13 E3
ID18 B4
ID19 B4
ID23 D4
ID27 B6
ID28 B6
ID29 C5
ID30 C5
ID31 B6
ID32 C6
ID33 A4
ID34 A3

Monitor Panel: Audio


1 2 3 4 5 6 7
A B C D E
M02B
AUDIO
M02B
+AUDIO-POWER
FD57
1D50
32V 3.0A T
ID61
FD58
+AUDIO-POWER-S
+3V3
+3V3
FD56
3D53
1R0
3D54
1R0
ID64
ID65
2D51
100u 4V
2D55
100n
100u 4V
2D52
100n
2D56
GND-A
GND-A
GND-AUDIO
GND-AUDIO
13
4
7D53
UDA1334BTS
VDDA
VDDD
AUDIO-BCK
FD50
1
BCK
AUDIO-WS
FD51
2
WS
AUDIO-DAO
FD52
3
DATAI
DIGITAL INTERFACE
DE-EMPHASIS
SFOR0
11
SFOR1
7
GND-AUDIO
AUDIO-MCK
FD53
6
SYSCLK
INTERPOLATION FILTER
FD54
8
MUTE
FD55
9
DEEM
NOISE SHAPER
10
PCS
DAC
DAC
GND-AUDIO
+AUDIO-L
14
VOL
VOR
16
VSSA
VSSD
VREF-DAC
15
5
12
ID71
GND-A
GND-AUDIO
2D54
100n
2D53
100u 4V
GND-A
GND-A
-AUDIO-R
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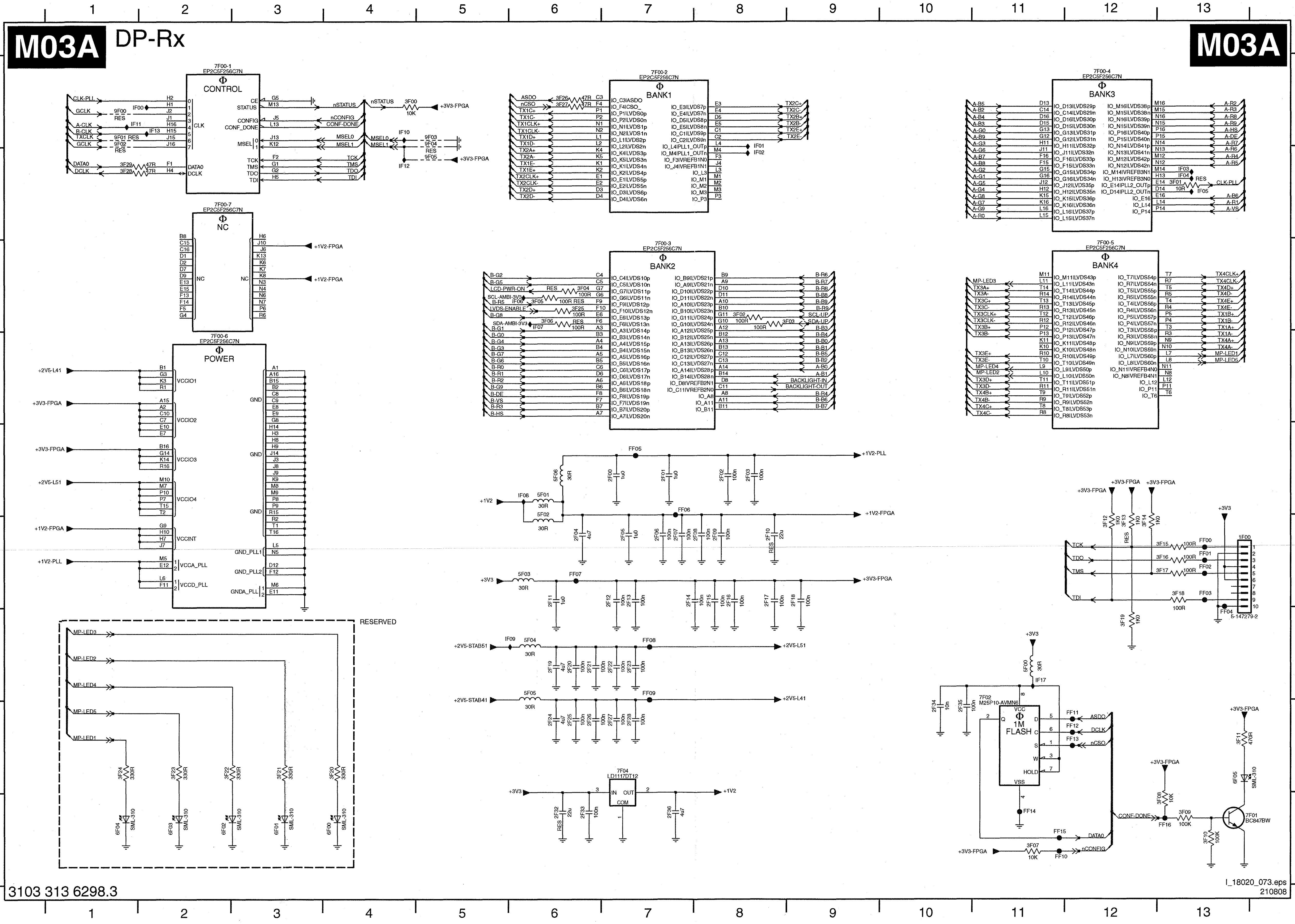
1D50	A3
2D51	B3
2D52	B4
2D53	E4
2D54	E4
2D55	B3
2D56	B5
3D53	B4
3D54	B4
7D53	C3
FD50	C2
FD51	C2
FD52	C2
FD53	D2
FD54	D3
FD55	D3
FD56	B4
FD57	A2
FD58	A3
ID61	A3
ID64	B3
ID65	B4
ID71	E4

Monitor Panel: DP-Rx


M03A
DP-Rx
7F00-1 EP2C5F256C7N CONTROL
7F00-7 EP2C5F256C7N NC
7F00-6 EP2C5F256C7N POWER
7F00-2 EP2C5F256C7N BANK1
7F00-3 EP2C5F256C7N BANK2
7F00-4 EP2C5F256C7N BANK3
7F00-5 EP2C5F256C7N BANK4
7F02 M25P10-AVMN6 1M FLASH
7F04 LD1117DT12
7F01 BC847BW
1F00 5-147279-2
RESERVED
+3V3-FPGA
+1V2-FPGA
+1V2-PLL
+2V5-L51
+2V5-L41
+2V5-STAB51
+2V5-STAB41
+3V3
+1V2
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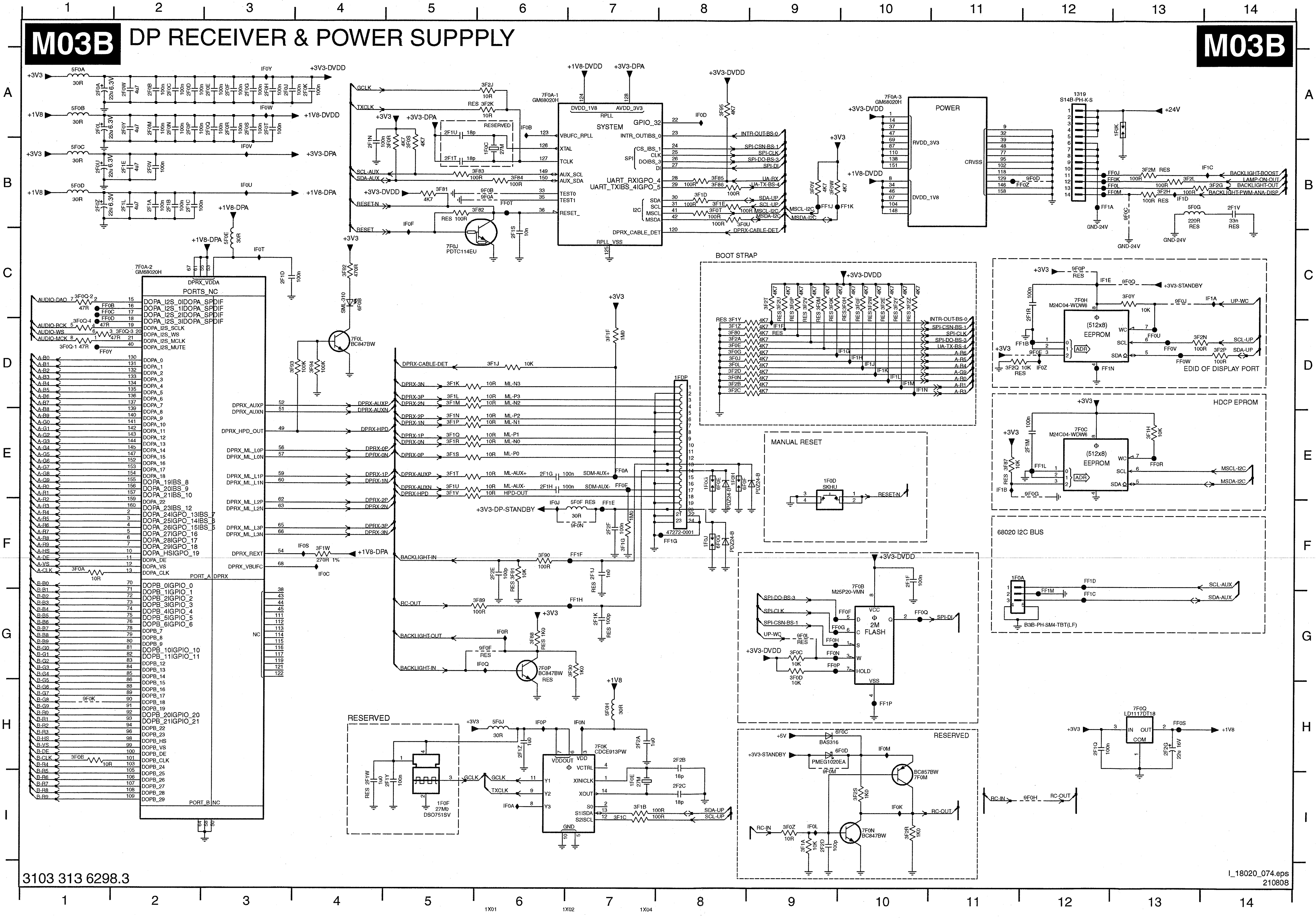
1F00	F13	IF00	A1
2F00	E7	IF01	A8
2F01	E7	IF02	B8
2F02	E8	IF03	B13
2F03	E8	IF04	B13
2F04	F6	IF05	B13
2F05	F7	IF06	C6
2F06	F7	IF07	C6
2F07	F7	IF08	E6
2F08	F8	IF09	G6
2F09	F8	IF10	A4
2F10	F8	IF11	A1
2F11	F6	IF12	B4
2F12	F7	IF13	A2
2F13	F7	IF17	G11
2F14	F7		
2F15	F8		
2F16	F8		
2F17	F8		
2F18	F9		
2F19	G6		
2F20	G6		
2F21	G6		
2F22	G7		
2F23	G7		
2F24	H6		
2F25	H6		
2F26	H6		
2F27	H7		
2F28	H7		
2F32	I6		
2F33	I6		
2F34	H10		
2F35	H10		
2F36	I7		
3F00	A4		
3F01	B13		
3F02	C8		
3F03	C9		
3F04	C6		
3F05	C6		
3F06	C6		
3F07	I11		
3F08	I13		
3F09	I13		
3F10	I13		
3F11	H13		
3F12	F12		
3F13	F12		
3F14	F12		
3F15	F13		
3F16	F13		
3F17	F13		
3F18	F13		
3F19	G12		
3F20	H4		
3F21	H3		
3F22	H2		
3F23	H2		
3F24	H1		
3F25	C6		
3F26	A6		
3F27	A6		
3F28	B1		
3F29	B1		
5F00	G11		
5F01	E6		
5F02	F6		
5F03	F6		
5F04	G6		
5F05	G6		
5F06	E6		
6F00	I4		
6F01	I3		
6F02	I2		
6F03	I2		
6F04	I1		
6F05	H13		
7F00-1	A2		
7F00-2	A7		
7F00-3	C7		
7F00-4	A12		
7F00-5	C12		
7F00-6	D2		
7F00-7	B2		
7F01	I13		
7F02	G11		
7F04	H7		
9F00	A1		
9F01	A1		
9F02	A1		
9F03	A5		
9F04	A5		
9F05	B5		
FF00	F13		
FF01	F13		
FF02	F13		
FF03	F13		
FF04	G13		
FF05	E7		
FF06	E7		
FF07	F6		
FF08	G7		
FF09	G7		
FF10	I11		
FF11	H12		
FF12	H12		
FF13	H12		
FF14	I11		
FF15	I11		
FF16	I13		

Monitor Panel: DP-Receiver & Power



1319	A12	3F2C	D8	FF1M	G12
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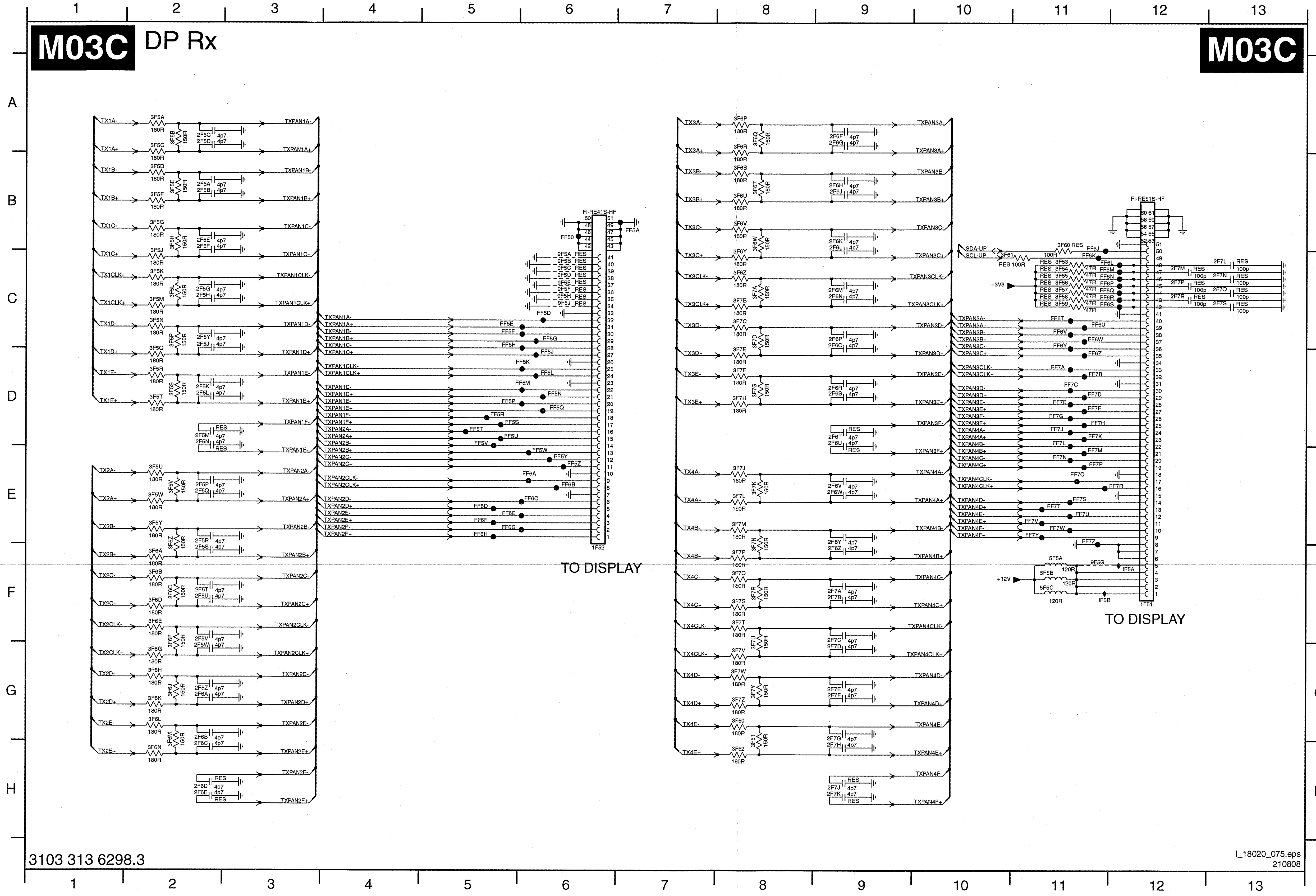
1F0C	B6	3F2E	C10	FF1P	H10
1F0D	E9	3F2G	B14	IF0A	I6
1F0E	I7	3F2H	B13	IF0B	A6
1F0F	I5	3F2J	A6	IF0C	F4
1F0G	E8	3F2K	A6	IF0D	A8
1F0H	E8	3F2L	B13	IF0F	B5
1F0J	F8	3F2M	B13	IF0J	F6
1F0K	A13	3F2N	D13	IF0K	I10
1FDP	D8	3F2P	D14	IF0L	I9
2F0A	A1	3F2Q	D11	IF0M	H10
2F0B	A2	3F2R	I10	IF0N	H7
2F0C	A2	3F2S	I10	IF0P	H6
2F0D	A2	3F2T	C9	IF0Q	G6
2F0E	A3	3F2U	C9	IF0R	G6
2F0F	A3	3F2V	C9	IF0S	F4
2F0G	A3	3F2W	C10	IF0T	C3
2F0H	A3	3F2Y	C10	IF0U	B3
2F0J	A3	3F2Z	C10	IF0V	B3
2F0K	A4	3F30	G7	IF0W	A3
2F0L	A1	3F80	D8	IF0Y	A3
2F0M	A2	3F81	B5	IF0Z	D12
2F0N	A2	3F82	B6	IF1A	C14
2F0P	A2	3F83	B6	IF1B	E11
2F0Q	A3	3F84	B6	IF1C	B14
2F0R	A3	3F85	B8	IF1D	B13
2F0S	A3	3F86	B8	IF1E	C12
2F0T	A3	3F87	E11	IF1F	D9
2F0U	B1	3F88	G6	IF1G	D10
2F0V	B2	3F89	G6	IF1H	D10
2F0W	A2	3F90	F6	IF1J	D10
2F0Y	A2	3F91	F6	IF1K	D10
2F0Z	B1	3F92	C4	IF1L	D10
2F1A	B2	3F93	D3	IF1M	D10
2F1B	B2	3F94	D4	IF1N	D10
2F1C	B2	3F95	A8		
2F1D	C3	5F0A	A1		
2F1E	B2	5F0B	A1		
2F1F	F10	5F0C	B1		
2F1G	E6	5F0D	B1		
2F1H	E6	5F0E	C3		
2F1J	F7	5F0F	F7		
2F1K	G7	5F0G	B13		
2F1L	B2	5F0H	H7		
2F1M	E12	5F0J	H6		
2F1N	B4	6F0B	C4		
2F1Q	H12	6F0C	H10		
2F1R	C12	6F0D	H10		
2F1S	C6	6F0E	E8		
2F1T	B5	6F0F	E8		
2F1U	A5	6F0G	F8		
2F1V	B14	7F0A-1	A6		
2F1W	I4	7F0A-2	C2		
2F1Y	I5	7F0A-3	A10		
2F1Z	H6	7F0B	F10		
2F2A	H7	7F0C	E12		
2F2B	H8	7F0H	C12		
2F2C	I8	7F0J	C5		
2F2D	I9	7F0K	H7		
2F2E	F6	7F0L	D4		
2F2F	F7	7F0M	I10		
2F2G	H13	7F0N	I10		
3F0A	F1	7F0P	G6		
3F0B	H1	7F0Q	H13		
3F0C	G9	9F0A	B6		
3F0D	G9	9F0B	B6		
3F0E	D8	9F0C	B13		
3F0F	C10	9F0D	B12		
3F0G	D8	9F0E	D12		
3F0H	C10	9F0F	G6		
3F0J	D8	9F0G	E12		
3F0K	C9	9F0H	I12		
3F0L	D8	9F0J	C13		
3F0M	C9	9F0K	H1		
3F0N	D8	9F0L	G9		
3F0P	C9	9F0M	I9		
3F0Q-1	D1	9F0N	F7		
3F0Q-2	C1	9F0P	C12		
3F0Q-3	D2	9F0Q	C13		
3F0Q-4	D1	FF0A	E7		
3F0R	B5	FF0B	C1		
3F0S	B5	FF0C	C1		
3F0T	B8	FF0D	D1		
3F0U	B8	FF0E	E7		
3F0V	B9	FF0F	G10		
3F0W	B9	FF0G	G9		
3F0Y	C13	FF0H	G9		
3F0Z	I9	FF0J	B13		
3F1A	I9	FF0K	B13		
3F1B	I7	FF0L	B13		
3F1C	I7	FF0M	B13		
3F1D	B8	FF0N	G9		
3F1E	B8	FF0P	G9		
3F1F	D7	FF0Q	G10		
3F1G	F7	FF0R	E13		
3F1H	E13	FF0S	H13		
3F1J	D6	FF0T	B6		
3F1K	D5	FF0U	D13		
3F1L	D5	FF0V	D13		
3F1M	D5	FF0W	D13		
3F1N	E5	FF0Y	D1		
3F1P	E5	FF0Z	B12		
3F1Q	E5	FF1A	B12		
3F1R	E5	FF1B	D12		
3F1S	E5	FF1C	G12		
3F1T	E5	FF1D	F12		
3F1U	E5	FF1E	F7		
3F1V	E5	FF1F	F7		
3F1W	F4	FF1G	F8		
3F1Y	D8	FF1H	G7		
3F1Z	D8	FF1J	B9		
3F2A	D8	FF1K	B10		
3F2B	D8	FF1L	E12		

Monitor Panel: DP-Rx



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1F52	F6
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2F5B	B2
2F5C	A2
2F5D	A2
2F5E	B2
2F5F	B2
2F5G	C2
2F5H	C2
2F5J	C2
2F5K	D2
2F5L	D2
2F5M	D2
2F5N	D2
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2F5Q	E2
2F5R	E2
2F5S	F2
2F5T	F2
2F5U	F2
2F5V	F2
2F5W	G2
2F5Y	C2
2F5Z	G2
2F6A	G2
2F6B	G2
2F6C	H2
2F6D	H2
2F6E	H2
2F6F	A9
2F6G	A9
2F6H	B9
2F6J	B9
2F6K	B9
2F6L	B9
2F6M	C9
2F6N	C9
2F6P	C9
2F6Q	C9
2F6R	D9
2F6S	D9
2F6T	D9
2F6U	D9
2F6V	E9
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2F6Y	E9
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2F7D	G9
2F7E	G9
2F7F	G9
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2F7J	H9
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2F7P	C12
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2F7S	C13
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3F5E	B2
3F5F	B2
3F5G	B2
3F5H	B2
3F5J	C2
3F5K	C2
3F5L	C2
3F5M	C2
3F5N	C2
3F5P	C2
3F5Q	D2
3F5R	D2
3F5S	D2
3F5T	D2
3F5U	E2
3F5V	E2
3F5W	E2
3F5Y	E2
3F5Z	E2
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3F61	C11
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3F6C	F2
3F6D	F2
3F6E	F2
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3F6H	G2
3F6J	G2
3F6K	G2
3F6L	G2
3F6M	G2
3F6N	H2
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3F6R	A8
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3F7B	C8
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3F7Q	F8
3F7R	F8
3F7S	F8
3F7T	F8
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3F7V	G8
3F7W	G8
3F7Y	G8
3F7Z	G8
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5F5C	F11
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9F5B	C6
9F5C	C6
9F5D	C6
9F5E	C6
9F5F	C6
9F5G	F11
9F5H	C6
9F5J	C6
FF50	B6
FF5A	B7
FF5D	C6
FF5E	C5
FF5F	C5
FF5G	C6
FF5H	C5
FF5J	D6
FF5K	D6
FF5L	D6
FF5M	D6
FF5N	D6
FF5P	D5
FF5Q	D6
FF5R	D5
FF5S	D5
FF5T	D5
FF5U	D5
FF5V	D5
FF5W	E6
FF5Y	E6
FF5Z	E6
FF6A	E6
FF6B	E6
FF6C	E6
FF6D	E5
FF6E	E5
FF6F	E5
FF6G	E5
FF6H	E5
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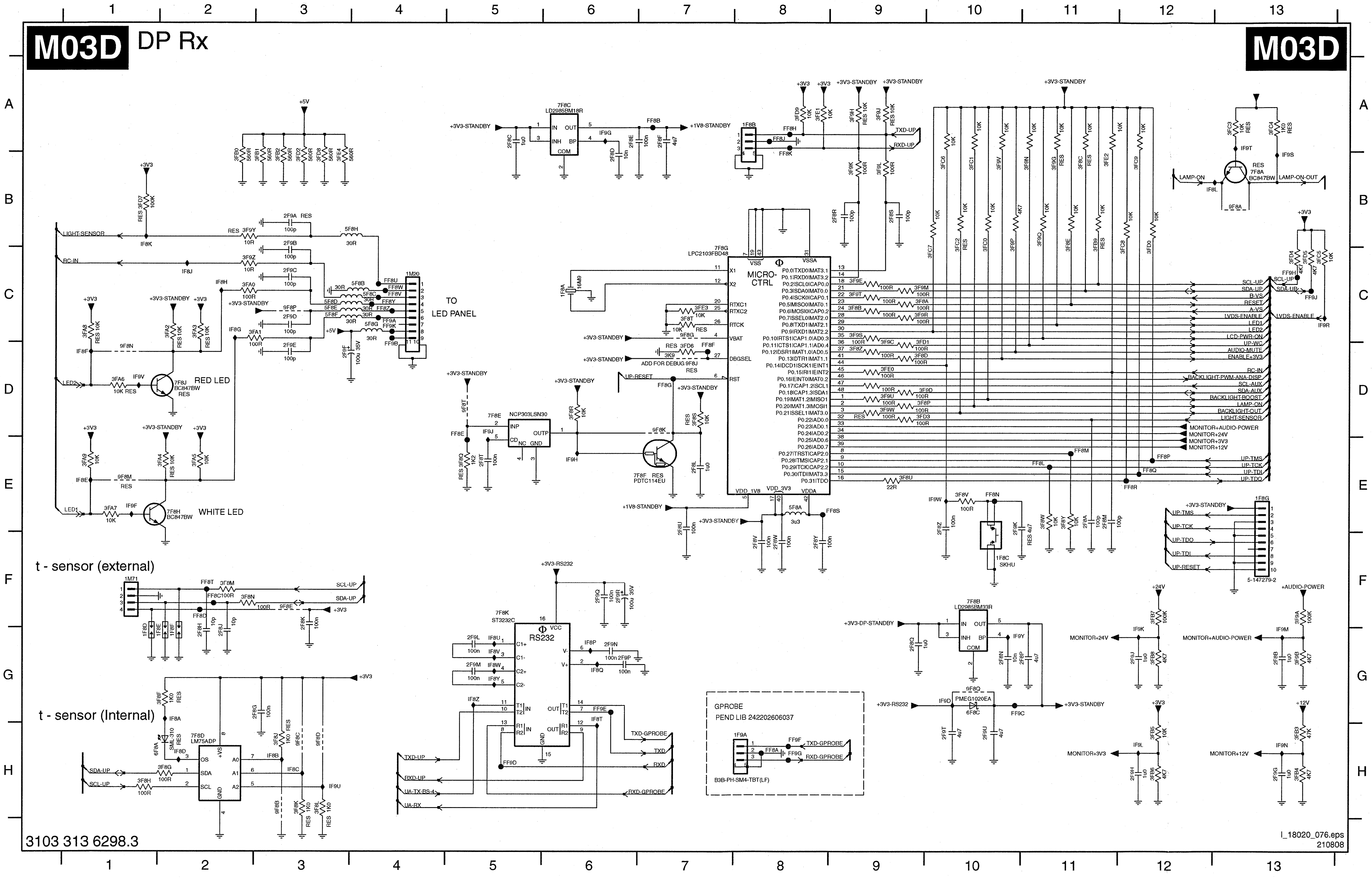
FF6L	C11
FF6M	C11
FF6N	C11
FF6P	C11
FF6Q	C11
FF6R	C11
FF6S	C11
FF6T	C11
FF6U	C11
FF6V	C11
FF6W	C11
FF6Y	C11
FF6Z	D11
FF7A	D11
FF7B	D11
FF7C	D11
FF7D	D11
FF7E	D11
FF7F	D11
FF7G	D11
FF7H	D11
FF7J	D11
FF7K	D11
FF7L	D11
FF7M	E11
FF7N	E11
FF7P	E11
FF7Q	E11
FF7R	E12
FF7S	E11
FF7T	E11
FF7U	E11
FF7V	E11
FF7W	E11
FF7Y	E11
FF7Z	E11
IF5A	F12
IF5B	F11

Monitor Panel: DP-Rx


M03D
DP Rx
M03D
MICRO-CTRL
LPC2103FBD48
TO LED PANEL
RED LED
WHITE LED
t - sensor (external)
t - sensor (Internal)
RS232
ST3232C
LM75ADP
NCP303LSN30
LD2985BM18R
LD2985BM33R
PMEG1020EA
GPROBE
PEND LIB 242202606037
B3B-PH-SM4-TBT(LF)
LIGHT-SENSOR
RC-IN
LAMP-ON
LAMP-ON-OUT
SCL-UP
SDA-UP
TXD-UP
RXD-UP
UA-TX-BS-4
UA-RX
TXD-GPROBE
RXD-GPROBE
UP-TMS
UP-TCK
UP-TDO
UP-TDI
UP-RESET
MONITOR+24V
MONITOR+AUDIO-POWER
MONITOR+3V3
MONITOR+12V
+3V3-STANDBY
+1V8-STANDBY
+3V3-RS232
3103 313 6298.3
I_18020_076.eps
210808

1F8A	C6
1F8B	A8
1F8C	F10
1F8D	G1
1F8E	G2
1F8F	G2
1F8G	E13
1F9A	H8
1M20	C4
1M71	F1
2F8A	E11
2F8B	G13
2F8C	A5
2F8D	B6
2F8E	A6
2F8F	A7
2F8G	G3
2F8H	G2
2F8J	G2
2F8K	F3
2F8L	E7
2F8M	E11
2F8N	G10
2F8P	G11
2F8Q	G9
2F8R	B9
2F8S	B9
2F8T	E5
2F8U	E7
2F8V	F8
2F8W	F8
2F8Y	F8
2F8Z	E10
2F9A	B3
2F9B	B3
2F9C	C3
2F9D	C3
2F9E	D3
2F9F	D3
2F9G	H13
2F9H	H12
2F9J	G12
2F9K	E10
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2F9M	G5
2F9N	G6
2F9P	G6
2F9Q	F6
2F9R	F6
2F9T	H10
2F9U	H10
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3F8W	E11
3F8Y	E11
3F8Z	D9
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3F9B	G13
3F9C	D9
3F9D	D10
3F9E	C9
3F9G	B11
3F9H	A9
3F9J	A9
3F9K	B9
3F9L	B9
3F9M	C9
3F9N	B11
3F9P	B10
3F9Q	B11
3F9R	C9
3F9S	C9
3F9T	C9
3F9U	D9
3F9V	B10
3F9W	D9
3F9Y	B2
3F9Z	C2
3FA0	C2
3FA1	C3
3FA2	C2
3FA3	C2
3FA4	E2
3FA5	E2
3FA6	D1
3FA7	E1
3FA8	C1
3FA9	E1
3FB0	B2
3FB1	B3
3FB2	B3
3FB3	H13
3FB4	H13
3FB5	H12
3FB6	H12
3FB7	F12
3FB8	G12
3FB9	B11
3FC0	B10
3FC1	B10
3FC2	B10
3FC3	A13
3FC4	A13
3FC5	C13
3FC6	B10
3FC7	C10
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3FC9	B12
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3FD2	B3
3FD3	D9
3FD4	C13
3FD5	C13
3FD6	D7
3FD7	B1
3FD8	B3
3FD9	A8
3FE0	D9
3FE1	A8
3FE2	B11
3FE3	C7
3FE4	B3
5F8A	E8
5F8B	C4
5F8C	C4
5F8D	C3
5F8E	C3
5F8F	C3
5F8G	C4
5F8H	B4
6F8A	H2
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7F8F	E6
7F8G	C7
7F8H	E2
7F8J	D2
7F8K	F5
9F8A	B13
9F8B	H3
9F8C	H3
9F8D	H3
9F8E	F3
9F8G	C7
9F8J	D7
9F8K	D7
9F8M	E1
9F8N	D1
9F8P	C3
9F8Q	G10
9F8T	D5
FF8A	H8
FF8B	A7
FF8C	F2
FF8D	F2
FF8E	D5
FF8F	D7
FF8G	D7
FF8H	A8
FF8J	A8
FF8K	B8
FF8L	E11
FF8M	E11
FF8N	E10
FF8P	E12
FF8Q	E12
FF8R	E12
FF8S	E9
FF8T	F2
FF8U	C4
FF8V	C4
FF8W	C4
FF8Y	C4
FF8Z	C4
FF9A	C4
FF9B	D4
FF9C	G10
FF9D	H5
FF9E	G6
FF9F	H8
FF9G	H8
FF9H	C13
FF9J	C13
FF9K	C4
IF8A	G2
IF8B	H3
IF8C	H3
IF8D	H2
IF8E	E1
IF8F	D1
IF8G	C2
IF8H	C2
IF8J	C2
IF8K	B1
IF8L	B12
IF8P	G6
IF8Q	G6
IF8T	G6
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IF8V	G5
IF8W	G5
IF8Y	G5
IF8Z	G5
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IF9G	A6
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IF9L	H12
IF9M	G13
IF9N	H13
IF9R	C13
IF9S	B13
IF9T	A13
IF9U	H3
IF9V	D1
IF9W	E10
IF9Y	G10

Monitor: SRP List

Netname	Diagram
+12V	M1A
+12V	M3C
+12V	M3D
+1V2	M3A
+1V2-FPGA	M3A
+1V2-PLL	M3A
+1V8	M3B
+1V8-DPA	M3B
+1V8-DVDD	M3B
+1V8-STANDBY	M3D
+24V	M1A
+24V	M3B
+24V	M3D
+24VF	M1A
+24VF	M1B
+2V5-L41	M3A
+2V5-L51	M3A
+2V5-STAB41	M1A
+2V5-STAB41	M3A
+2V5-STAB51	M1A
+2V5-STAB51	M3A
+3V3	M1A
+3V3	M2B
+3V3	M3A
+3V3	M3B
+3V3	M3C
+3V3	M3D
+3V3-DPA	M3B
+3V3-DP-STANDBY	M3B
+3V3-DP-STANDBY	M3D
+3V3-DVDD	M3B
+3V3-FPGA	M3A
+3V3-RS232	M1B
+3V3-RS232	M3D
+3V3-STANDBY	M2A
+3V3-STANDBY	M3B
+3V3-STANDBY	M3D
+5V	M1B
+5V	M3B
+5V	M3D
+AUDIO-L	M2A
+AUDIO-POWER	M1A
+AUDIO-POWER	M2B
+AUDIO-POWER	M3D
+AUDIO-POWER-S	M2A
+AUDIO-POWER-S	M2B
A-B0	M3A (1x)
A-B0	M3B (1x)
A-B1	M3A (1x)
A-B1	M3B (1x)
A-B2	M3A (1x)
A-B2	M3B (1x)
A-B3	M3A (1x)
A-B3	M3B (1x)
A-B4	M3A (1x)
A-B4	M3B (1x)
A-B5	M3A (1x)
A-B5	M3B (1x)
A-B6	M3A (1x)
A-B6	M3B (1x)
A-B7	M3A (1x)
A-B7	M3B (1x)
A-B8	M3A (1x)
A-B8	M3B (1x)
A-B9	M3A (1x)
A-B9	M3B (1x)
A-CLK	M3A (1x)
A-CLK	M3B (1x)
A-DE	M3A (1x)
A-DE	M3B (1x)
A-G0	M3A (1x)
A-G0	M3B (1x)
A-G1	M3A (1x)
A-G1	M3B (1x)
A-G2	M3A (1x)
A-G2	M3B (1x)
A-G3	M3A (1x)
A-G3	M3B (1x)
A-G4	M3A (1x)
A-G4	M3B (1x)
A-G5	M3A (1x)
A-G5	M3B (1x)
A-G6	M3A (1x)
A-G6	M3B (1x)
A-G7	M3A (1x)
A-G7	M3B (1x)
A-G8	M3A (1x)
A-G8	M3B (1x)
A-G9	M3A (1x)
A-G9	M3B (2x)
A-HS	M3A (1x)
A-HS	M3B (1x)
A-R0	M3A (1x)
A-R0	M3B (2x)
A-R1	M3A (1x)
A-R1	M3B (2x)
A-R2	M3A (1x)
A-R2	M3B (1x)
A-R3	M3A (1x)
A-R3	M3B (2x)
A-R4	M3A (1x)
A-R4	M3B (2x)
A-R5	M3A (1x)
A-R5	M3B (2x)
A-R6	M3A (1x)
A-R6	M3B (2x)
A-R7	M3A (1x)
A-R7	M3B (1x)
A-R8	M3A (1x)
A-R8	M3B (1x)
A-R9	M3A (1x)
A-R9	M3B (1x)
ASDO	M3A (2x)
A-STDBY	M2A (2x)
AUDIO-BCK	M2B (1x)
AUDIO-BCK	M3B (1x)
AUDIO-DAO	M2B (1x)
AUDIO-DAO	M3B (1x)
AUDIO-MCK	M2B (1x)
AUDIO-MCK	M3B (1x)
AUDIO-MUTE	M2A (1x)
AUDIO-MUTE	M3D (1x)
-AUDIO-R	M2A (1x)
AUDIO-WS	M2B (1x)
AUDIO-WS	M3B (1x)
AVCC	M2A (1x)
A-VS	M3A (1x)
A-VS	M3B (1x)
A-VS	M3D (1x)
BACKLIGHT-BOOST	M3B (1x)
BACKLIGHT-BOOST	M3D (1x)
BACKLIGHT-IN	M3A (1x)
BACKLIGHT-IN	M3B (2x)
BACKLIGHT-OUT	M3A (1x)
BACKLIGHT-OUT	M3B (2x)
BACKLIGHT-OUT	M3D (1x)
BACKLIGHT-PWM-ANA-DISP	M3B (1x)
BACKLIGHT-PWM-ANA-DISP	M3D (1x)
B-B0	M3A (1x)
B-B0	M3B (1x)
B-B1	M3A (1x)
B-B1	M3B (1x)
B-B2	M3A (1x)
B-B2	M3B (1x)
B-B3	M3A (1x)
B-B3	M3B (1x)
B-B4	M3A (1x)
B-B4	M3B (1x)
B-B5	M3A (1x)
B-B5	M3B (1x)
B-B6	M3A (1x)
B-B6	M3B (1x)
B-B7	M3A (1x)
B-B7	M3B (1x)
B-B8	M3A (1x)
B-B8	M3B (1x)
B-B9	M3A (1x)
B-B9	M3B (1x)
B-CLK	M3A (1x)
B-CLK	M3B (1x)
B-DE	M3A (1x)
B-DE	M3B (1x)
B-G0	M3A (1x)
B-G0	M3B (1x)
B-G1	M3A (1x)
B-G1	M3B (1x)
B-G2	M3A (1x)
B-G2	M3B (1x)
B-G3	M3A (1x)
B-G3	M3B (1x)
B-G4	M3A (1x)
B-G4	M3B (1x)
B-G5	M3A (1x)
B-G5	M3B (1x)
B-G6	M3A (1x)
B-G6	M3B (1x)
B-G7	M3A (1x)
B-G7	M3B (1x)
B-G8	M3A (1x)
B-G8	M3B (1x)
B-G9	M3A (1x)
B-G9	M3B (1x)
B-HS	M3A (1x)
B-HS	M3B (1x)
B-R0	M3A (1x)
B-R0	M3B (1x)
B-R1	M3A (1x)
B-R1	M3B (1x)
B-R2	M3A (1x)
B-R2	M3B (1x)
B-R3	M3A (1x)
B-R3	M3B (1x)
B-R4	M3A (1x)
B-R4	M3B (1x)
B-R5	M3A (1x)
B-R5	M3B (1x)
B-R6	M3A (1x)
B-R6	M3B (1x)
B-R7	M3A (1x)
B-R7	M3B (1x)
B-R8	M3A (1x)
B-R8	M3B (1x)
B-R9	M3A (1x)
B-R9	M3B (1x)
B-VS	M3A (1x)
B-VS	M3B (1x)
B-VS	M3D (1x)
CLK-PLL	M3A (2x)
CONF-DONE	M3A (2x)
DATA0	M3A (2x)
DCLK	M3A (2x)
DPRX-0N	M3B (2x)
DPRX-0P	M3B (2x)
DPRX-1N	M3B (2x)
DPRX-1P	M3B (2x)
DPRX-2N	M3B (2x)
DPRX-2P	M3B (2x)
DPRX-3N	M3B (2x)
DPRX-3P	M3B (2x)
DPRX-AUXN	M3B (2x)
DPRX-AUXP	M3B (2x)
DPRX-CABLE-DET	M3B (2x)
DPRX-HPD	M3B (2x)
ENABLE+3V3	M1A (1x)
ENABLE+3V3	M3D (1x)
GCLK	M3A (2x)
GCLK	M3B (3x)
GND-24V	M1A (2x)
GND-24V	M3B (3x)
GND-A	M2A (4x)
GND-A	M2B (5x)
GND-AUDIO	M1A (1x)
GND-AUDIO	M2A (17x)
GND-AUDIO	M2B (5x)
INTR-OUT-BS-0	M3B (2x)
LAMP-ON	M3D (2x)
LAMP-ON-OUT	M3B (1x)
LAMP-ON-OUT	M3D (1x)
LCD-PWR-ON	M1A (1x)
LCD-PWR-ON	M3A (1x)
LCD-PWR-ON	M3D (1x)
LED1	M3D (2x)
LED2	M3D (2x)
LEFT-SPEAKER	M2A (3x)
LIGHT-SENSOR	M3D (2x)
LVDS-ENABLE	M3A (1x)
LVDS-ENABLE	M3D (2x)
MONITOR+12V	M3D (3x)
MONITOR+24V	M3D (2x)
MONITOR+3V3	M3D (2x)
MONITOR+AUDIO-POWER	M3D (2x)
MP-LED1	M3A (2x)
MP-LED2	M3A (2x)
MP-LED3	M3A (2x)
MP-LED4	M3A (2x)
MP-LED5	M3A (2x)
MSCL-I2C	M3B (3x)
MSDA-I2C	M3B (3x)
MSEL0	M3A (2x)
MSEL1	M3A (2x)
MUTE	M2A (2x)
nCONFIG	M3A (2x)
nCSO	M3A (2x)
nSTATUS	M3A (2x)
RC-IN	M3B (2x)
RC-IN	M3D (2x)
RC-OUT	M3B (3x)
RESET	M3B (1x)
RESET	M3D (1x)
RESET-N	M3B (2x)
RIGHT-SPEAKER	M2A (3x)
RXD	M1A (1x)
RXD	M3D (1x)
RXD-GPROBE	M3D (2x)
RXD-UP	M3D (2x)
SCL-AUX	M3B (2x)
SCL-AUX	M3D (1x)
SCL-UP	M3A (1x)
SCL-UP	M3B (3x)
SCL-UP	M3C (1x)
SCL-UP	M3D (4x)
SDA-AUX	M3B (2x)
SDA-AUX	M3D (1x)
SDA-UP	M3A (1x)
SDA-UP	M3B (3x)
SDA-UP	M3C (1x)
SDA-UP	M3D (4x)
SPI-CLK	M3B (3x)
SPI-CSN-BS-1	M3B (3x)
SPI-DI	M3B (2x)
SPI-DO-BS-3	M3B (3x)
TCK	M3A (2x)
TDI	M3A (2x)
TDO	M3A (2x)
TMS	M3A (2x)
TX1A-	M3A (1x)
TX1A-	M3C (1x)
TX1A+	M3A (1x)
TX1A+	M3C (1x)
TX1B-	M3A (1x)
TX1B-	M3C (1x)
TX1B+	M3A (1x)
TX1B+	M3C (1x)
TX1C-	M3A (1x)
TX1C-	M3C (1x)
TX1C+	M3A (1x)
TX1C+	M3C (1x)
TX1CLK-	M3A (1x)
TX1CLK-	M3C (1x)
TX1CLK+	M3A (1x)
TX1CLK+	M3C (1x)
TX1D-	M3A (1x)
TX1D-	M3C (1x)
TX1D+	M3A (1x)
TX1D+	M3C (1x)
TX1E-	M3A (1x)
TX1E-	M3C (1x)
TX1E+	M3A (1x)
TX1E+	M3C (1x)
TX2A-	M3A (1x)
TX2A-	M3C (1x)
TX2A+	M3A (1x)
TX2A+	M3C (1x)
TX2B-	M3A (1x)
TX2B-	M3C (1x)
TX2B+	M3A (1x)
TX2B+	M3C (1x)
TX2C-	M3A (1x)
TX2C-	M3C (1x)
TX2C+	M3A (1x)
TX2C+	M3C (1x)
TX2CLK-	M3A (1x)
TX2CLK-	M3C (1x)
TX2CLK+	M3A (1x)
TX2CLK+	M3C (1x)
TX2D-	M3A (1x)
TX2D-	M3C (1x)
TX2D+	M3A (1x)
TX2D+	M3C (1x)
TX2E-	M3A (1x)
TX2E-	M3C (1x)
TX2E+	M3A (1x)
TX2E+	M3C (1x)
TX3A-	M3A (1x)
TX3A-	M3C (1x)
TX3A+	M3A (1x)
TX3A+	M3C (1x)
TX3B-	M3A (1x)
TX3B-	M3C (1x)
TX3B+	M3A (1x)
TX3B+	M3C (1x)
TX3C-	M3A (1x)
TX3C-	M3C (1x)
TX3C+	M3A (1x)
TX3C+	M3C (1x)
TX3CLK-	M3A (1x)
TX3CLK-	M3C (1x)
TX3CLK+	M3A (1x)
TX3CLK+	M3C (1x)
TX3D-	M3A (1x)
TX3D-	M3C (1x)
TX3D+	M3A (1x)
TX3D+	M3C (1x)
TX3E-	M3A (1x)
TX3E-	M3C (1x)
TX3E+	M3A (1x)
TX3E+	M3C (1x)
TX4A-	M3A (1x)
TX4A-	M3C (1x)
TX4A+	M3A (1x)
TX4A+	M3C (1x)
TX4B-	M3A (1x)
TX4B-	M3C (1x)
TX4B+	M3A (1x)
TX4B+	M3C (1x)
TX4C-	M3A (1x)
TX4C-	M3C (1x)
TX4C+	M3A (1x)
TX4C+	M3C (1x)
TX4CLK-	M3A (1x)
TX4CLK-	M3C (1x)
TX4CLK+	M3A (1x)
TX4CLK+	M3C (1x)
TX4D-	M3A (1x)
TX4D-	M3C (1x)
TX4D+	M3A (1x)
TX4D+	M3C (1x)
TX4E-	M3A (1x)
TX4E-	M3C (1x)
TX4E+	M3A (1x)
TX4E+	M3C (1x)
TXCLK	M3A (1x)
TXCLK	M3B (2x)
TXD	M1A (1x)
TXD	M3D (1x)
TXD-GPROBE	M3D (2x)
TXD-UP	M3D (2x)
TXPAN1A-	M3C (2x)
TXPAN1A+	M3C (2x)
TXPAN1B-	M3C (2x)
TXPAN1B+	M3C (2x)
TXPAN1C-	M3C (2x)
TXPAN1C+	M3C (2x)
TXPAN1CLK-	M3C (2x)
TXPAN1CLK+	M3C (2x)
TXPAN1D-	M3C (2x)
TXPAN1D+	M3C (2x)
TXPAN1E-	M3C (2x)
TXPAN1E+	M3C (2x)
TXPAN1F-	M3C (2x)
TXPAN1F+	M3C (2x)
TXPAN2A-	M3C (2x)
TXPAN2A+	M3C (2x)
TXPAN2B-	M3C (2x)
TXPAN2B+	M3C (2x)
TXPAN2C-	M3C (2x)
TXPAN2C+	M3C (2x)
TXPAN2CLK-	M3C (2x)
TXPAN2CLK+	M3C (2x)
TXPAN2D-	M3C (2x)
TXPAN2D+	M3C (2x)
TXPAN2E-	M3C (2x)
TXPAN2E+	M3C (2x)
TXPAN2F-	M3C (2x)
TXPAN2F+	M3C (2x)
TXPAN3A-	M3C (2x)
TXPAN3A+	M3C (2x)
TXPAN3B-	M3C (2x)
TXPAN3B+	M3C (2x)
TXPAN3C-	M3C (2x)
TXPAN3C+	M3C (2x)
TXPAN3CLK-	M3C (2x)
TXPAN3CLK+	M3C (2x)
TXPAN3D-	M3C (2x)
TXPAN3D+	M3C (2x)
TXPAN3E-	M3C (2x)
TXPAN3E+	M3C (2x)
TXPAN3F-	M3C (2x)
TXPAN3F+	M3C (2x)
TXPAN4A-	M3C (2x)
TXPAN4A+	M3C (2x)
TXPAN4B-	M3C (2x)
TXPAN4B+	M3C (2x)
TXPAN4C-	M3C (2x)
TXPAN4C+	M3C (2x)
TXPAN4CLK-	M3C (2x)
TXPAN4CLK+	M3C (2x)
TXPAN4D-	M3C (2x)
TXPAN4D+	M3C (2x)
TXPAN4E-	M3C (2x)
TXPAN4E+	M3C (2x)
TXPAN4F-	M3C (2x)
TXPAN4F+	M3C (2x)
UA-RX	M3B (1x)
UA-RX	M3D (1x)
UA-TX-BS-4	M3B (2x)
UA-TX-BS-4	M3D (1x)
UP-RESET	M3D (1x)
UP-TCK	M3D (2x)
UP-TDI	M3D (2x)
UP-TDO	M3D (2x)
UP-TMS	M3D (2x)
UP-WC	M3B (2x)
UP-WC	M3D (1x)

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Layout Monitor Panel (Top Side)

1316	C3
1319	B1
13DP	C2
1735	A3
1D50	B3
1E06	C3
1F00	A3
1F0A	A1
1F0C	B2
1F0D	C1
1F51	A2
1F52	A3
1F8B	B1
1F8C	B2
1F8G	C2
1F9A	C1
1FDP	C1
1M20	A1
1M71	A1
1U00	C3
2D05	A2
2D07	A3
2D08	A3
2D09	A3
2D10	A3
2D11	A3
2D12	A3
2D15	A3
2D18	A3
2D19	B3
2D20	B3
2D25	A3
2D30	B3
2D31	B3
2D51	B2
2D52	B3
2D53	B3
2F0A	B2
2F0L	B2
2F0U	A2
2F0Y	B2
2F0Z	C2
2F11	A2
2F1E	A2
2F1G	C1
2F1H	C1
2F1Q	A2
2F1T	B2
2F1U	B2
2F1V	A1
2F2G	B2
2F8G	A1
2F8H	A1
2F8J	A1
2F8K	A1
2F8N	C1
2F8P	C1
2F8Q	C1
2F8R	B1
2F8S	C1
2F9F	A1
2F9R	C1
2U00	C3
2U01	B3
2U02	C3
2U03	B3
2U04	B3
2U05	B3
2U09	B3
2U11	B3
2U12	B3
2U13	C2
2U18	B2
2U19	B2
2U20	C2
2U30	C3
2U31	C2
2U32	C2
2U50	C3
2U51	C3
2U52	C2
2U53	C2
2U62	C3
2U66	C3
3D03	A3
3D11	A3
3F08	A1
3F09	A1
3F0A	B1
3F10	A1
3F11	A1
3F1K	C1
3F1L	C1
3F1M	C1
3F1N	C1
3F1P	C1
3F1Q	C1
3F1R	C1
3F1S	C1
3F1T	C1
3F1U	C1
3F1V	C1
3F20	A1
3F21	A1
3F22	A1
3F23	A1
3F24	A1
3F29	A2
3F2G	B1
3F2H	B1
3F2L	B1
3F2M	B1
3F50	A2
3F51	A2
3F52	A2
3F5A	A2
3F5B	A2
3F5C	A2
3F5D	A2
3F5E	A2
3F5F	A2
3F5G	A2
3F5H	A2
3F5J	A2
3F5K	A2
3F5L	A2
3F5M	A2
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3F5P	A2
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3F5U	A2
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3F6R	A1
3F6S	A1
3F6T	A1
3F6U	A1
3F6V	A1
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3F6Y	A1
3F6Z	A1
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3F7M	A2
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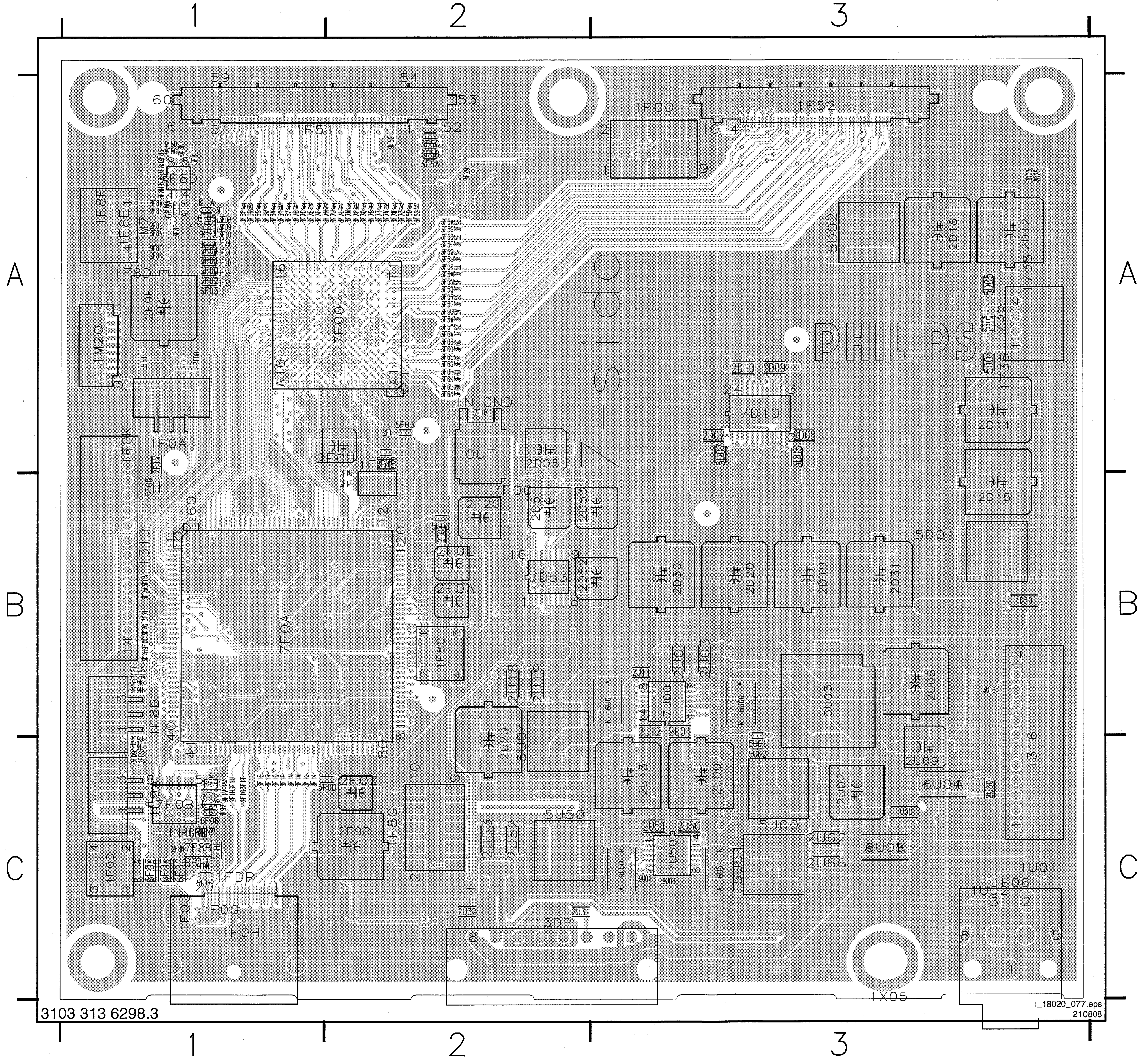
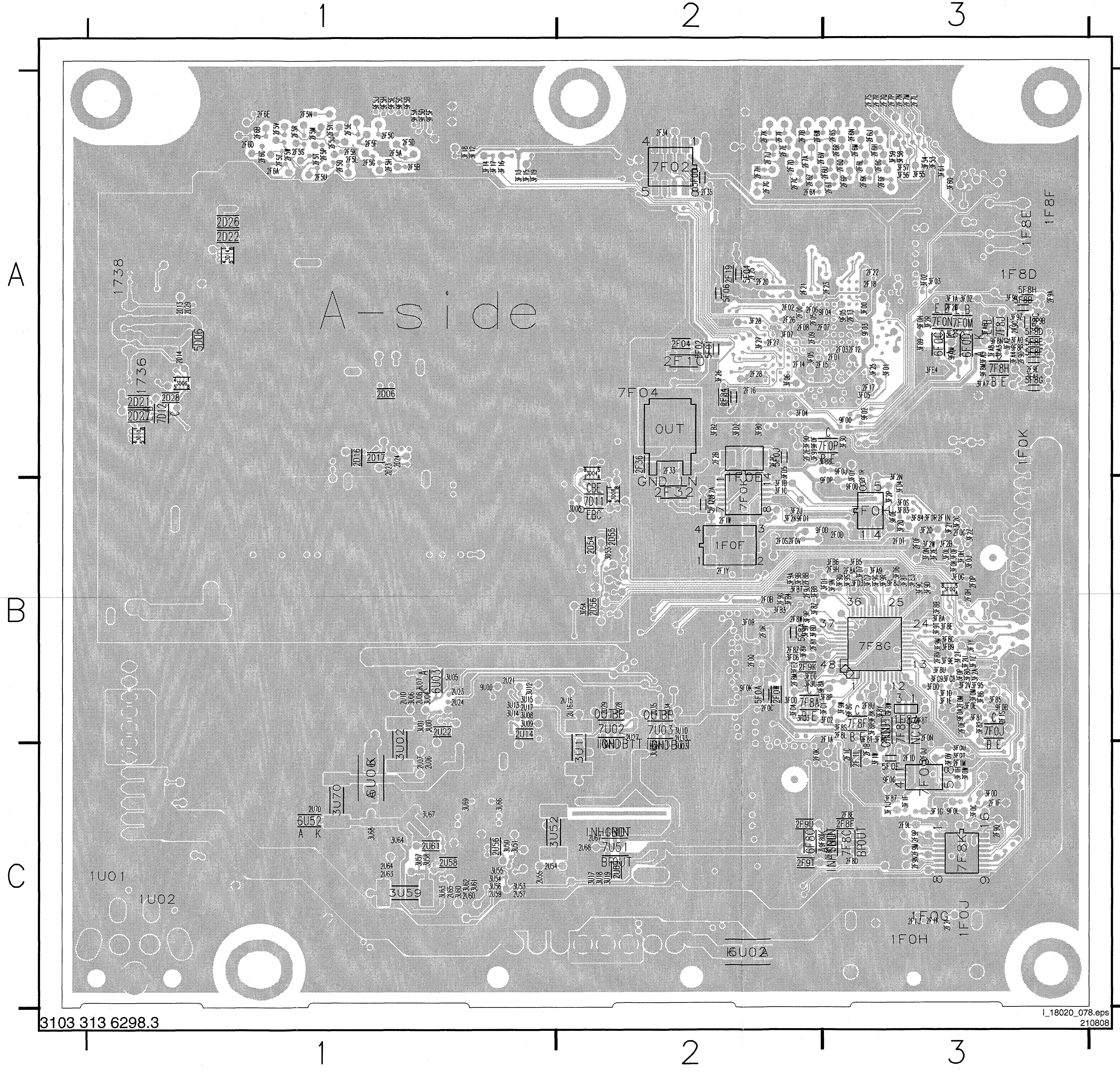
3F7P	A2
3F7Q	A2
3F7R	A2
3F7S	A2
3F7T	A2
3F7U	A2
3F7V	A2
3F7W	A2
3F7Y	A2
3F7Z	A2
3F8F	A1
3F8G	A1
3F8H	A1
3F8J	A1
3F8K	A1
3F8L	A1
3F8M	A1
3F8N	A1
3F92	C1
3F93	C1
3F94	C1
3F9H	B1
3F9J	C1
3F9K	B1
3F9L	C1
3FB1	A1
3FD8	A1
3FD9	C1
3FE1	B1
3U16	B3
5D01	B3
5D02	A3
5D04	A3
5D05	A3
5D07	A3
5D08	A3
5F03	A2
5F0B	B2
5F0C	A2
5F0D	C2
5F0F	C1
5F0G	B1
5F5A	A2
5F5B	A2
5F5C	A2
5U00	C3
5U01	C3
5U02	C3
5U03	B3
5U04	B2
5U50	C2
5U51	C3
6F00	A1
6F01	A1
6F02	A1
6F03	A1
6F04	A1
6F05	A1
6F0B	C1
6F0E	C1
6F0F	C1
6F0G	C1
6F8A	A1
6U00	B3
6U01	B2
6U04	C3
6U05	C3
6U50	C3
6U51	C3
7D10	A3
7D53	B2
7F00	A2
7F01	A1
7F0A	B1
7F0B	C1
7F0L	C1
7F0Q	B2
7F8B	C1
7F8D	A1
7U00	B3
7U50	C3
9F0C	B1
9F0N	C1
9F5G	A2
9F8B	A1
9F8C	A1
9F8D	A1
9F8E	A1
9U01	C3
9U03	C3


1
2
3
A
B
C
1F51
1F52
1F00
1F8F
1F8E
1M71
1F8D
2F9F
1M20
1F0A
1F0K
1319
1F8B
1F0B
7F0B
1F0D
1FDP
1F0G
1F0H
2F9R
1F8G
7F00
7F0A
2F0U
2F0L
2F0A
2F2G
2F0Z
OUT
IN GND
2D05
2D51
2D53
7D53
2D52
Z-side
PHILIPS
2D10
2D09
7D10
2D07
2D08
5D02
2D18
2D12
1735
1736
2D11
2D15
5D01
2D30
2D20
2D19
2D31
1D50
2U05
1316
2U09
6U04
5U03
7U00
2U04
2U03
2U11
2U12
2U01
2U13
2U00
5U01
5U02
2U02
2U30
1U00
2U20
5U04
2U18
2U19
5U50
2U53
2U52
2U51
2U50
7U50
5U51
5U00
2U62
2U66
6U05
1U01
1E06
1U02
13DP
2U32
2U31
1X05
3103 313 6298.3
I_18020_077.eps
210808

Layout Monitor Panel (Bottom Side)



1F0E	A2
1F0F	B2
1F8A	B3
2D06	A1
2D13	A1
2D14	A1
2D16	A1
2D17	A1
2D21	A1
2D22	A1
2D23	A1
2D24	A1
2D26	A1
2D27	A1
2D28	A1
2D29	A1
2D54	B2
2D55	B2
2D56	B2
2F00	A2
2F01	A3
2F02	A2
2F03	A3
2F04	A2
2F05	A2
2F06	A2
2F07	A3
2F08	A2
2F09	A2
2F0B	B2
2F0C	B2
2F0D	B3
2F0E	B3
2F0F	B3
2F0G	B3
2F0H	B3
2F0J	C3
2F0K	C2
2F0M	B3
2F0N	B3
2F0P	B3
2F0Q	B2
2F0R	B2
2F0S	B2
2F0T	B3
2F0V	B2
2F0W	B2
2F10	A2
2F12	A3
2F13	A3
2F14	A2
2F15	A2
2F16	A2
2F17	A3
2F18	A3
2F19	A2
2F1A	B3
2F1B	C3
2F1C	C3
2F1D	C3
2F1F	C3
2F1J	C3
2F1K	C3
2F1L	C3
2F1M	C3
2F1N	B3
2F1R	A3
2F1S	B3
2F1W	B2
2F1Y	B2
2F1Z	B2
2F20	A2
2F21	A2
2F22	A3
2F23	A3
2F24	A2
2F25	A2
2F26	A2
2F27	A2
2F28	A2
2F2A	B2
2F2B	A2
2F2C	A2
2F2D	A3
2F2E	A2
2F2F	C3
2F32	B2
2F33	A2
2F34	A2
2F35	A2
2F36	A2
2F5A	A1
2F5B	A1
2F5C	A1
2F5D	A1
2F5E	A1
2F5F	A1
2F5G	A1
2F5H	A1
2F5J	A1
2F5K	A1
2F5L	A1
2F5M	A1
2F5N	A1
2F5P	A1
2F5Q	A1
2F5R	A1
2F5S	A1
2F5T	A1
2F5U	A1
2F5V	A1
2F5W	A1
2F5Y	A1
2F5Z	A1
2F6A	A1
2F6B	A1
2F6C	A1
2F6D	A1
2F6E	A1
2F6F	A3
2F6G	A3
2F6H	A3
2F6J	A3
2F6K	A3
2F6L	A3
2F6M	A3
2F6N	A3
2F6P	A3
2F6Q	A3
2F6R	A3
2F6S	A3
2F6T	A3
2F6U	A3
2F6V	A2
2F6W	A2
2F6Y	A2
2F6Z	A2
2F7A	A2
2F7B	A2
2F7C	A2
2F7D	A2
2F7E	A2
2F7F	A2
2F7G	A2
2F7H	A2
2F7J	A2
2F7K	A2
2F7L	A3
2F7M	A3
2F7N	A3
2F7P	A3
2F7Q	A3
2F7R	A3
2F7S	A3
2F8A	B3
2F8B	B2
2F8C	C3
2F8D	C3
2F8E	C3
2F8F	C3
2F8L	B3
2F8M	B2
2F8T	B3
2F8U	B3
2F8V	B3
2F8W	B2
2F8Y	B2
2F8Z	B2
2F9A	A3
2F9B	A3
2F9C	A3
2F9D	A3
2F9E	A3
2F9G	B2
2F9H	B3
2F9J	B2
2F9K	B2
2F9L	C3
2F9M	C3
2F9N	C3
2F9P	C3
2F9Q	C3
2F9T	C2
2F9U	C2
2U06	C1
2U07	C1
2U08	B1
2U10	B1
2U14	B1
2U15	B2
2U16	B2
2U17	B1
2U21	B1
2U22	B1
2U23	B1
2U24	B1
2U27	B2
2U28	B2
2U29	B2
2U33	B2
2U34	B2
2U35	B2
2U54	C1
2U55	C1
2U56	C1
2U57	C1
2U58	C1
2U59	C1
2U60	C1
2U61	C1
2U63	C1
2U64	C1
2U65	C1
2U67	C2
2U68	C2
2U69	C2
2U70	C1
3D04	A2
3D05	B2
3D06	A1
3D08	B2
3D10	A1
3D14	A1
3D53	B2
3D54	B2
3F00	A3
3F01	A3
3F02	A3
3F03	A3
3F04	A2
3F05	A2
3F06	A2
3F07	A2
3F0B	B2
3F0C	C3
3F0D	C3
3F0E	B3
3F0F	B3
3F0G	B3
3F0H	B3
3F0J	B3
3F0K	B3
3F0L	B3
3F0M	B3
3F0N	B3
3F0P	B3
3F0Q	B3
3F0R	B3
3F0S	B3
3F0T	C3
3F0U	C3
3F0V	C3
3F0W	C3
3F0Y	A3
3F0Z	A3
3F12	A1
3F13	A1
3F14	A1
3F15	A1
3F16	A1
3F17	A1
3F18	A1
3F19	A1
3F1A	A3
3F1B	B2
3F1C	B2
3F1D	B3
3F1E	B3
3F1F	C3
3F1G	C3
3F1H	C3
3F1J	C3
3F1W	C3
3F1Y	B3
3F1Z	B3
3F25	A3
3F26	A2
3F27	A2
3F28	A2
3F2A	B3
3F2B	B3
3F2C	B3
3F2D	B3
3F2E	B3
3F2J	B2
3F2K	B2
3F2N	B3
3F2P	B3
3F2Q	B3
3F2R	A3
3F2S	A3
3F2T	B3
3F2U	B3
3F2V	B3
3F2W	B3
3F2Y	B3
3F2Z	B3
3F30	A3
3F53	A3
3F54	A3
3F55	A3
3F56	A3
3F57	A3
3F58	A3
3F59	A3
3F60	A3
3F61	A3
3F80	B3
3F81	B3
3F82	B3
3F83	B3
3F84	B3
3F85	B3
3F86	B3
3F87	C3
3F88	A3
3F89	A3
3F8A	B3
3F8B	B3
3F8C	B3
3F8D	B2
3F8E	B3
3F8P	B3
3F8Q	B3
3F8R	B3
3F8S	B3
3F8T	B3
3F8U	B3
3F8V	B2
3F8W	B3
3F8Y	B3
3F8Z	B2
3F90	A2
3F91	A2
3F95	B3
3F9A	B2
3F9B	B2
3F9C	B3
3F9D	B3
3F9E	B3
3F9G	B3
3F9M	B3
3F9N	B3
3F9P	B2
3F9Q	B3
3F9R	B3
3F9S	B3
3F9T	B3
3F9U	B2
3F9V	B2
3F9W	B3
3F9Y	A3
3F9Z	A3
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3FA3	A3
3FA4	A3
3FA5	A3
3FA6	A3
3FA7	A3
3FA8	A3
3FA9	B3
3FB0	A2
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3FB3	B2
3FB4	B2
3FB5	B3
3FB6	B3
3FB7	B2
3FB8	B2
3FB9	B3
3FC0	B2
3FC1	B3
3FC2	B3
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3FC4	B2
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3FC6	B2
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3FC8	B3
3FC9	B3
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3FD1	B3
3FD2	A2
3FD3	B3
3FD4	B3
3FD5	A2
3FD6	B3
3FD7	B3
3FE0	B2
3FE2	B2
3FE3	B3
3FE4	A3
3U00	B1
3U01	B1
3U02	B1
3U03	C2
3U04	B1
3U05	B1
3U06	B1
3U07	B1
3U08	B1
3U09	B1
3U10	B2
3U11	C2
3U12	B1
3U13	B1
3U14	B1
3U15	B1
3U17	C2
3U18	C2
3U19	C2
3U50	C1
3U51	C1
3U52	C2
3U53	C1
3U54	C1
3U55	C1
3U56	C1
3U57	C1
3U58	C1
3U59	C1
3U60	C1
3U61	C1
3U62	C1
3U63	C1
3U64	C1
3U65	C2
3U66	C1
3U67	C1
3U68	C1
3U69	C1
3U70	C1
5D06	A1
5F00	A2
5F01	A2
5F02	A2
5F04	A2
5F05	A2
5F06	A2
5F0A	B2
5F0E	C3
5F0H	B2
5F0J	A2
5F8A	B2
5F8B	A3
5F8C	A3
5F8D	A3
5F8E	A3
5F8F	A3
5F8G	A3
5F8H	A3
6F0C	A3
6F0D	A3
6F8C	C2
6U02	C2
6U03	B1
6U06	C1
6U52	C1
7D11	B2
7D12	A1
7F02	A2
7F04	A2
7F0C	C3
7F0H	B3
7F0J	C3
7F0K	B2
7F0M	A3
7F0N	A3
7F0P	A3
7F8A	B2
7F8C	C3
7F8E	B3
7F8F	B3
7F8G	B3
7F8H	A3
7F8J	A3
7F8K	C3
7U02	B2
7U03	B2
7U51	C2
9F00	A3
9F01	B2
9F02	A3
9F03	A3
9F04	A3
9F05	A3
9F0A	B3
9F0B	B3
9F0D	B2
9F0E	B3
9F0F	A2
9F0G	C3
9F0H	A3
9F0J	A3
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9F5E	A1
9F5F	A1
9F5H	A1
9F5J	A1
9F8A	B2
9F8G	B3
9F8J	B3
9F8K	B3
9F8M	A3
9F8N	A3
9F8P	A3
9F8Q	C2
9F8T	B3
9U00	B1

8. Alignments

Index of this chapter:

8.1 General Alignment Conditions
8.2 Hardware Alignments
8.3 Software Alignments
8.4 Option Settings
8.5 Reset of Repaired SSB

Note: The Service Default Mode (SDM) and Service Alignment Mode (SAM) are described in chapter 5. Menu navigation is done with the CURSOR UP, DOWN, LEFT or RIGHT keys of the remote control transmitter.

8.1 General Alignment Conditions

Perform all electrical adjustments under the following conditions:

- Power supply voltage (depends on region):
  - AP-NTSC: 120 V_{AC} or 230 V_{AC} / 50 Hz (± 10%).
  - AP-PAL-multi: 120 - 230 V_{AC} / 50 Hz (± 10%).
  - EU: 230 V_{AC} / 50 Hz (± 10%).
  - LATAM-NTSC: 120 - 230 V_{AC} / 50 Hz (± 10%).
  - US: 120 V_{AC} / 60 Hz (± 10%).
- Connect the set to the mains via an isolation transformer with low internal resistance.
- Allow the set to warm up for approximately 15 minutes.
- Measure voltages and waveforms in relation to correct ground (e.g. measure audio signals in relation to AUDIO_GND).
  Caution: It is not allowed to use heatsinks as ground.
- Test probe: Ri > 10 Mohm, Ci < 20 pF.
- Use an isolated trimmer/screwdriver to perform alignments.

8.1.1 Alignment Sequence

- First, set the correct options:
  - In SAM, select “Options”, and then “Option numbers”.
  - Fill in the option settings for “Group 1” and “Group 2” according to the set sticker (see also paragraph “Option Settings”).
  - Press OK on the remote control **before** the cursor is moved to the left.
  - In submenu “Option numbers” select “Store” and press OK on the RC.
    OR:
  - In main menu, select “Store” again and press OK on the RC.
  - Switch the set to Stand-by.
- Warming up (>15 minutes).

8.2 Hardware Alignments

Not applicable.

8.3 Software Alignments

Put the set in SAM mode (see Chapter 5 “Service Modes, Error Codes and Fault Finding”). The SAM menu will now appear on the screen. Select ALIGNMENTS and go to one of the sub menus. The alignments are explained below.

The following item can be aligned:

- Whitepoint.

To store the data:

- Press OK on the RC **before** the cursor is moved to the left.
- In main menu select “Store” and press OK on the RC.
- Press MENU on the RC to switch back to the main menu.
- Switch the set to stand-by mode.

For the next alignments, supply the following test signals via a video generator to the RF input:

- **EU/AP-PAL** models: a PAL B/G TV-signal with a signal strength of at least 1 mV and a frequency of 475.25 MHz
- **US/AP-NTSC** models: an NTSC M/N TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).
- **LATAM** models: an NTSC M TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).
- **DVB-T** models: see table “SDM default settings” in chapter 5.

8.3.1 White Point

- Set “Active control” to “Off”.
- Choose “TV menu”, “TV Settings” and then “Picture” and put:
  - “Dynamic contrast” to “Off”.
  - “Colour enhancement” to “Off”.
  - “Light sensor” to “Off” where applicable.
  - “Clear LCD” to “On” where applicable.
  - “Brightness” to “50”.
  - “Colour” to “0”.
  - “Contrast” to “100”.
- Go to the SAM and select “Alignments”-> “Whitepoint”.

White point alignment LCD screens:

- Use a 100% white screen as input signal and set the following values:
  - “Colour temperature”: “Normal”.
  - All “Whitepoint” values to: “127”.
  - “Red BL offset” values to “8”.
  - “Green BL offset” values to “8”.

In case you have a colour analyser:

- Measure with a calibrated (phosphor- independent) colour analyser in the centre of the screen. Consequently, the measurement needs to be done in a dark environment.
- Adjust the correct x,y coordinates (while holding one of the White point registers R, G or B on 127) by means of decreasing the value of one or two other white points to the correct x,y coordinates (see table “White D alignment values”). Tolerance: dx: ± 0.004, dy: ± 0.004.
- Repeat this step for the other colour temperatures that need to be aligned.
- When finished press OK on the RC and then press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 8-1 White D alignment values

Value	Cool (11000 K)	Normal (9000 K)	Warm (6500 K)
x	0.273	0.282	0.306
y	0.278	0.286	0.309

If you do not have a colour analyser, you can use the default values. This is the next best solution. The default values are average values coming from production (statistics).

- Select a COLOUR TEMPERATURE (e.g. COOL, NORMAL, or WARM).
- Set the RED, GREEN and BLUE default values according to the values in the “Tint settings” table.
- When finished press OK on the RC, then press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 8-2 Tint settings

Colour Temp.	R	G	B
Cool	113	119	123
Normal	124	117	115
Warm	127	105	77

8.4 Option Settings

8.4.1 Introduction

The microprocessor communicates with a large number of I^2C ICs in the set. To ensure good communication and to make digital diagnosis possible, the microprocessor has to know which ICs to address. The presence/absence of these specific ICs (or functions) is made known by the option codes.

Notes:

- After changing the option(s), save them by pressing the OK button on the RC **before** the cursor is moved to the left, select STORE in the SAM root menu and press OK on the RC.
- The new option setting is only active after the TV is switched “off” / “stand-by” and “on” again with the Mains switch (the NVM is then read again).

8.4.2 Dealer Options

For dealer options, in SAM select “Dealer options” and then “Personal options”.

Table 8-3 Dealer options

Menu item	Subjects	Options	Description
Personal Options	Picture Mute	On	Picture is muted / not muted in case no input signal is detected at input connectors
		Off	
	Virgin Mode	On	TV starts up / does not start up (once) with a language selection menu after the Mains switch is turned “on” for the first time (virgin mode)
		Off	

8.4.3 (Service) Options

Select the sub menu's to set the initialization codes (options) of the set via text menus.

Table 8-4 Service options

Menu-item	Subjects	Options	Description
Data	8 days EPG	Off	No possibility to program 8 days in advance using EPG
		On	Possibility to program 8 days in advance using EPG
Display	Screen	“Value”	Used screen size, type, and resolution (see table “Option code overview” in this chapter)
	Display fans	Not present / Present	Feature present / not present
	Temperature sensor	No sensor / Sensor on backside / Sensor in display	Location and presence of temperature sensor
	Temperature LUT	x	
	E-box & monitor	Off / On	E-box & monitor off / on
Video Repro	Perfect Pixel	Off / On	Perfect Pixel off / on
	Ambilight	None / Stereo / Triple / Quad	Inverter not present / one inverter / two inverters / three inverters / four inverters
	Ambilight technology	LED / Future use	LED (/future use)
	MOP ambient light	Not present / Present	MOP not present / present
	Light sensor	Not Present / Present	Light sensor not present / present
	Light sensor type	Glass / Plastic	Sensor type
Source selection	EXT1 type	“Value”	Specification
	EXT2 type	“Value”	Specification
	EXT3 type	“Value”	Specification
	HDMI 1	Present	Present
	HDMI 2	Present	Present
	HDMI 3	Present	Present
	HDMI CEC extended	Off / On	Feature not present / present
	HDMI CEC	Off / On	Feature not present / present
	USB version	“Value”	Specification
	Ethernet	Not present / Present	Feature not present / present
	Online services	Not present / Present	Feature not present / present
	PTP (Picture Transfer Protocol)	Not present / Present	Feature not present / present
	Connection assistant	Not present / Present	Feature not present / present
	Riva scroll RC support	Not present / Present	Feature not present / present
	System RC support	Not present / Present	Feature not present / present
Audio Repro	Acoustic System (Cabinet design, used for setting dynamic audio parameters)	11 / Essence 2K8 42	Cabinet specification

Menu-item	Subjects	Options	Description
Miscellaneous	Region	Europe / AP-PAL-Multi / Australia / China	Region indication
	ATSC / DVB	On / Off	ATSC / DVB-T active / not active
	Over the air download	Off / Country dependent / On	Specification
	DVB-T installation	Off / Country dependent / On	Specification
	DVB-C	Off / On	Feature not present / present
	DVB-C installation	Off / Country dependent / On	Specification
	MPEG4	Not present / present	Feature not present / present
	Tuner type	TD1716 Mk3 / TD1716 Mk4 / VA1Y9ED2008	Tuner type
	I^{2}C configuration	None / With PCA 9540	Specification
	Channel decoder	TDA10048	Channel decoder type
	Hotel mode	Off	Hotel mode not supported
	Video playback	Off / On	Feature present / not present
	Update assistant	Present	Feature present
	Board identifier	On	Board identifier supported
	LightGuide	Off / On	LightGuide off / LightGuide on
Opt. no.	Group 1		xxxxx xxxxx xxxxx xxxxx (see set sticker)
	Group 2		xxxxx xxxxx xxxxx xxxxx (see set sticker)
	Store - go right	Store - press OK	Store option settings

8.4.4 Opt. No. (Option numbers)

Select this sub menu to set all options at once (expressed in two long strings of numbers).
An option number (or "option byte") represents a number of different options. When you change these numbers directly, you can set all options very quickly. All options are controlled via eight option numbers.
When the NVM is replaced, all options will require resetting. To be certain that the factory settings are reproduced exactly, you must set both option number lines. You can find the correct option numbers on a sticker inside the TV set and in Table "Option code overview".

Example: The options sticker gives the following option numbers:

- 04368 00005 01066 08707
- 00000 00032 00512 00000

The first line (group 1) indicates hardware options 1 to 4, the second line (group 2) indicates software options 5 to 8.
Every 5-digit number represents 16 bits (so the maximum value will be 65536 if all options are set).
When all the correct options are set, the sum of the decimal values of each Option Byte (OB) will give the option number.
See tables "Option code overview" for the options.

Diversity
Not all sets with the same Commercial Type Number (CTN) necessarily have the same option code!

Use of Alternative BOM
An alternative BOM number usually indicates the use of an alternative display or power supply. This results in another display code thus in another Option code. For the power supply there is no difference. Refer to chapter 2 "Safety Instructions, Warnings, and Notes".

8.4.5 Option Code Overview

Table 8-5 Option code overview

CTN_alt BOM#	Options Group 1	Options Group 2	Displ. (code)
42PES0001D/10	16897 01419 37079 45160	10152 21792 07041 0001	168
42PES0001H/10	16897 01419 37079 45160	10152 21924 07073 0001	168

Important: after having edited the option numbers as described above, you **must** press OK on the remote control **before** the cursor is moved to the left!

8.5 Reset of Repaired SSB

A very important issue towards a repaired SSB from a service repair shop, implies the reset of the NVM on the SSB.

A repaired SSB in service should get the service Set type "00PF0000000000" and Production code "00000000000000". Also the virgin bit is to be set. To set all this, you can use the ComPair tool.

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

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9.2 Main Supply
9.3 On-board DC/DC Converters
9.4 Additional Monitor DC/DC Converters
9.5 Front-End
9.6 PNX85xx
9.7 Back-end
9.8 Audio
9.9 DLNA
9.10 Abbreviation List
9.11 IC Data Sheets

Notes:

- Only **new** circuits (circuits that are not published recently) are described.
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the wiring, block (chapter 6) and circuit diagrams (chapter 7). Where necessary, you will find a separate drawing for clarification.

9.1 Introduction

This chassis (member of the "TV522/92" platform) is a derivative from the Q529.1E LA/LB chassis. It is a new concept, introducing the separation between monitor and supporting hardware/software in a separate hub. The styling name is "ESSENCE". Hub and monitor are connected with a single cable. All I/O connectors are present on the hub, avoiding cable clutter around the screen.
The platform incorporates an improved (faster tuning, better phase noise performance, etc.) tuner block with separate support for DVB-C and DVB-T.
It's built around the PNX85xx "System on Chip" (SoC), which handles the video and audio processing, while the PNX51xx takes care of the video back-end processing. The CYCLONE II FPGA is used to process the data for the GENESIS Display Port, which transmits the data from hub to monitor.

9.1.1 Features

The main features for this chassis are:

- 1080p resolution @ 100 Hz.
- High performance back-end processing Perfect Pixel HD engine capable of 300 Mpixels/sec. With this technology, each pixel of the incoming picture is enhanced to better match the surrounding pixels, resulting in a more natural picture. Artifacts and noise in all sources from multimedia to standard TV to highly-compressed high-definition (HD) are detected and reduced. This results in a clean and razor sharp image.
- ClearLCD, a technology that uses scanning and back light dimming technology to reduce the motion blur on an LCD screen, caused by the slow response time and the "sample and hold" characteristic of LCD.
- The separation of panel and supporting electronics by introducing a separate monitor and hub, connected by a single-cable connection.
- The introduction of the Essence Smart Levelling Bracket, allowing hassle-free mounting of the screen on the wall.
- Improved tuner compared to Q528.1E LA chassis.
- Support of DVB-C reception (in some sets).
- For all other features: refer to the Q528.1E LA/LB Service Manual.

9.1.2 Delta's with respect to Q529.1E LA/LB chassis

- 3 HDMI inputs (inputs are swapped).
- ST7101-output is connected to HDMI multiplexer input 4.
- None of the HDMI inputs is associated with L/R side I/O.
- No SVHS on side I/O.
- Fan control added.
- No AmbiLight implementation > no AL EPLD.
- Audio via I^{2}S.
- Possible other startup/shutdown behaviour (due to standby SW).
- Dedicated Essence Display Port functionality (the display ports perform the interface between hub/monitor and interconnection cable).

9.1.3 TV522/Essence Architecture Overview

For details about the chassis block diagrams refer to chapter "Block diagrams, Test Point Overview, and Waveforms". An overview of the TV522/92 architecture can be found in next figure "Architecture of TV522/92 platform".
The sets use the PNX85xx SoC and the PNX5100 Video Back-end Processor for video processing.

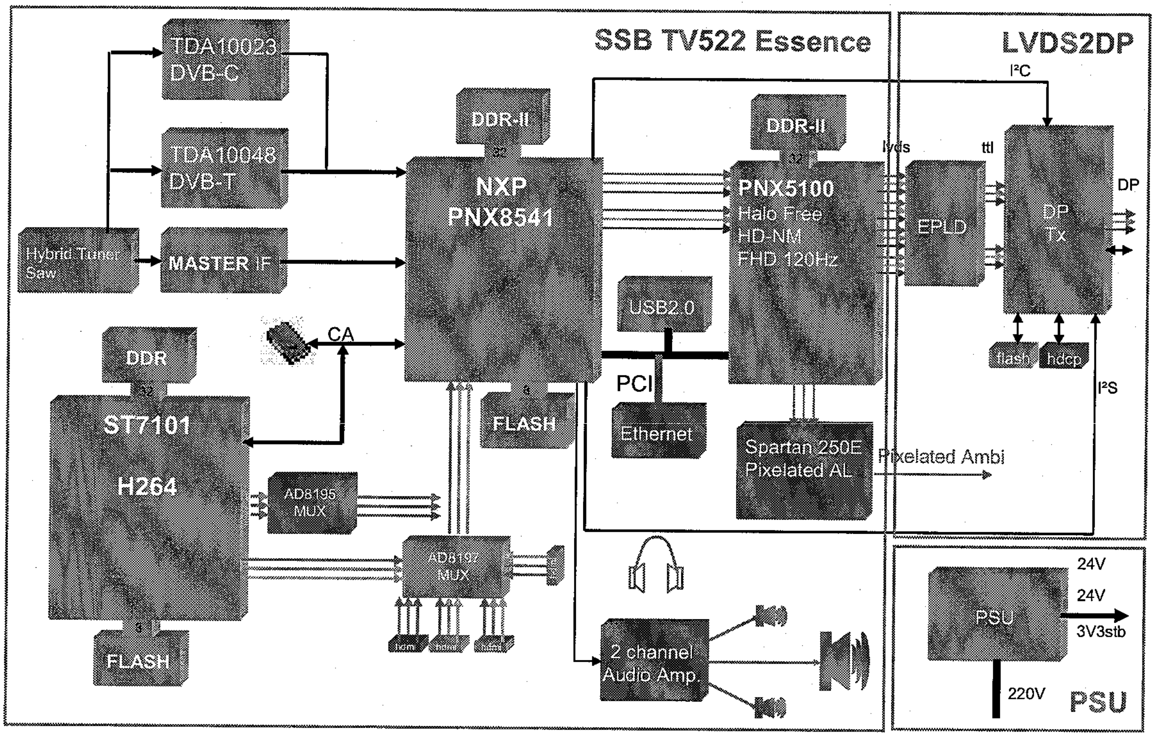
SSB TV522 Essence
LVDS2DP
TDA10023
DVB-C
TDA10048
DVB-T
Hybrid Tuner
Saw
MASTER IF
DDR-II
32
NXP
PNX8541
DDR-II
32
PNX5100
Halo Free
HD-NM
FHD 120Hz
I²C
lvds
ttl
EPLD
DP
Tx
DP
flash
hdcp
I²S
USB2.0
PCI
Ethernet
Spartan 250E
Pixelated AL
Pixelated Ambi
CA
DDR
32
ST7101
H264
FLASH
AD8195
MUX
AD8192
MUX
hdmi
hdmi
hdmi
FLASH
2 channel
Audio Amp.
PSU
24V
24V
3V3stb
220V
PSU

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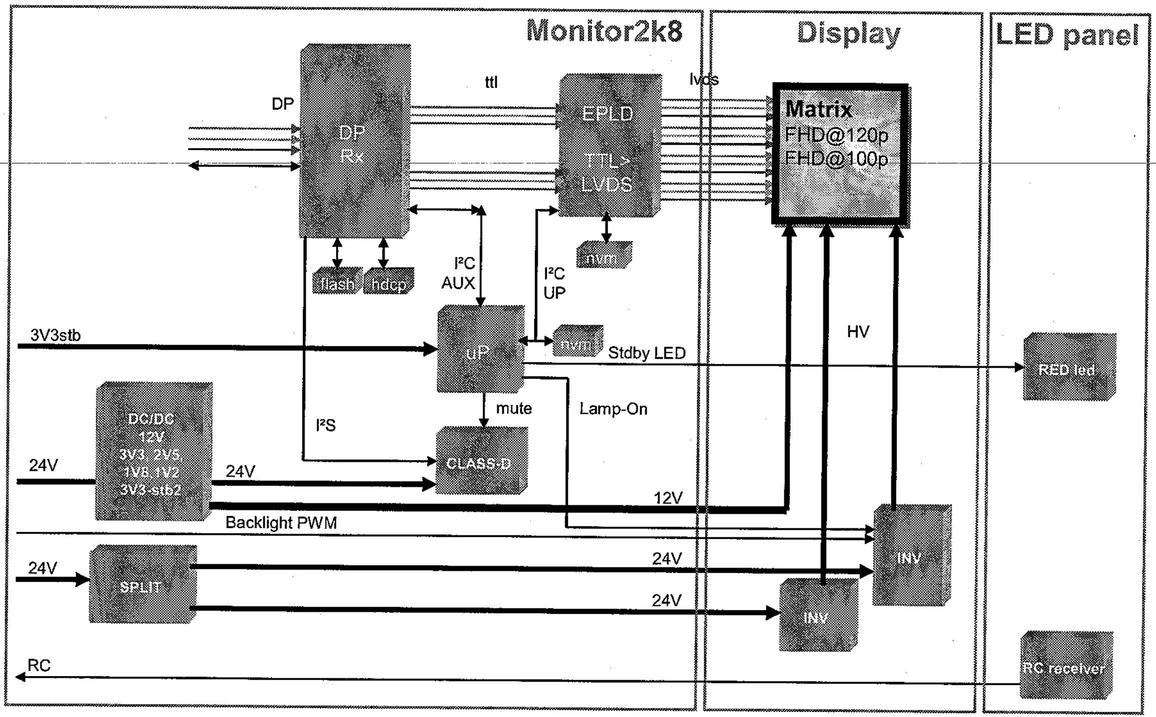
Figure 9-1 Architecture of Essence - Hub


Monitor2k8
Display
LED panel
DP
ttl
lvds
DP
Rx
EPLD
TTL>
LVDS
Matrix
FHD@120p
FHD@100p
flash
hdcp
nvm
I²C
AUX
I²C
UP
3V3stb
uP
nvm
Stdby LED
HV
RED led
mute
Lamp-On
I²S
CLASS-D
DC/DC
12V
3V3, 2V5,
1V8,1V2
3V3-stb2
24V
24V
12V
Backlight PWM
INV
24V
SPLIT
24V
24V
INV
RC
RC receiver

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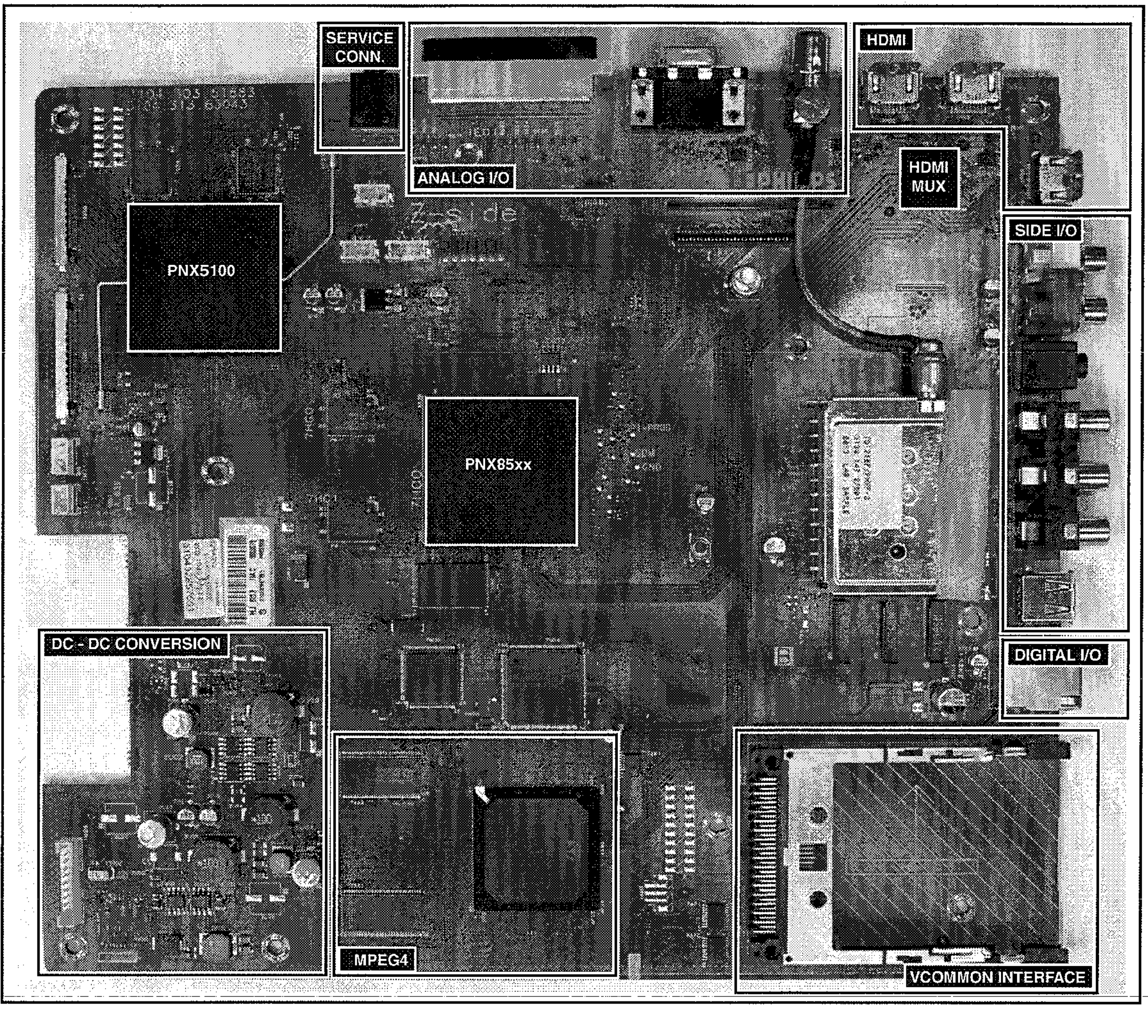
180908

Figure 9-2 Architecture of Essence - Monitor

9.1.4 SSB Cell Layout


SERVICE CONN.
ANALOG I/O
HDMI
HDMI MUX
SIDE I/O
PNX5100
PNX85xx
DIGITAL I/O
DC - DC CONVERSION
MPEG4
VCOMMON INTERFACE

I_18020_133.eps
080908

Figure 9-3 SSB top view

9.2 Main Supply

The sets in this chassis comes with a buy-in “Bobitrans” supply unit.
When defective, a new panel must be ordered and the defective panel must be sent for repair, unless the main fuse of the panel is broken. Always replace a defective fuse with one with the correct specifications! This part is available in the regular market.
Refer to the Spare Parts list for the order number of the supply unit.

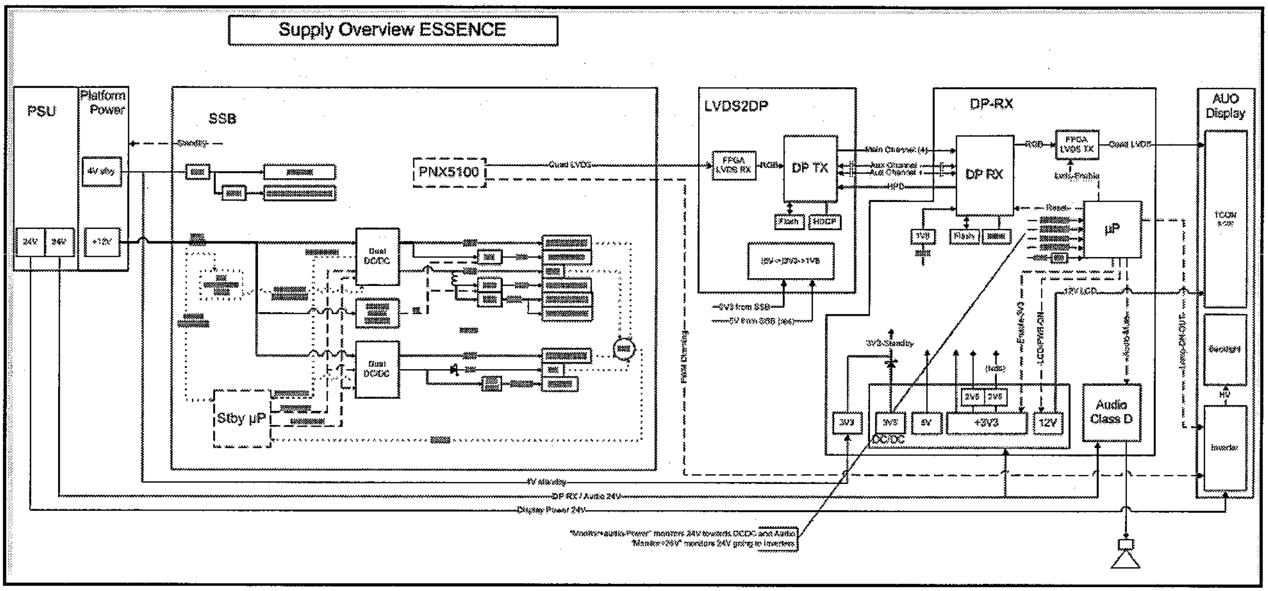


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Figure 9-4 High level Power Architecture ESSENCE

9.3 On-board DC/DC Converters

In this platform, on-board DC/DC converters have been foreseen. See also diagrams B01A, B01B and B01C.

9.3.1 PSU Start-up Sequence

1. If the input voltage of the DC/DC converters is around 12 V (measured on the decoupling capacitors 2U01/2U02) and the ENABLE signals are “low” (active), then the output voltages should have their normal values.
2. First, the Stand-by Processor activates the +1V2 supply (via ENABLE-1V2).
3. Then, after this voltage becomes present and is detected OK (about 100 ms), the other voltage of +3V3 will be activated (via ENABLE-3V3).
4. The current consumption of controller IC 7U00 is around 20 mA (that means around 200 mV drop voltage across resistor 3U01).

9.3.2 Internal Protection

- Provides a SUPPLY-FAULT signal (active “low”), when the output voltage of any DC/DC converter is out of its limits (± 10% of the normal value). In such cases, the Stand-by Processor will immediately stop the supplies by sending a “high” control signal towards the external and internal supplies: ENABLE-xVx, POD-MODE, ON-MODE, and STAND-BY.
  Note: The SUPPLY-FAULT control signal is “low” when any DC/DC converter is disabled by its control signal (ENABLE-xVx) and +12VSW is present, therefore it is ignored during start-up!
- The internal protection works together with the output over-voltage detector transistors 7U07-1 and 7U07-2.

9.3.3 1.2V and 3.3V DC/DC Converters

Introduction

The circuit used is a so-called “synchronous buck converter”. Some characteristics:

- Switching frequency: approx. 250 kHz.
- Efficiency: approx. 90%.
- Built-in output over-voltage and over-current protections
- Soft start.
- Software controlled “on/off” (via ENABLE line).

Block diagram

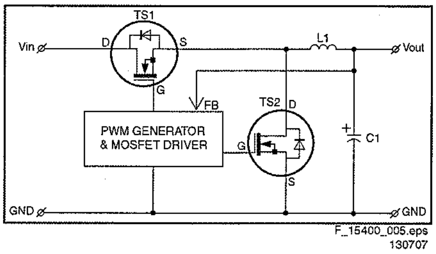

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Figure 9-5 Block diagram synchronous buck converter.

The advantage of a “synchronous buck converter” over a “classical buck converter” is its better efficiency (about 90%). The difference between the two is that in a synchronous buck converter the “low -side” diode is replaced by a MOSFET TS2 (item 7U05). This, because the voltage drop across a MOSFET is smaller than the forward voltage drop of a diode.
This second MOSFET TS2 conducts current during the “off” times of the first MOSFET TS1 (item 7U08 at the input side). The upper MOSFET TS1 conducts, to transfer energy from the input to the inductor L_1 and load R_L, while the lower MOSFET TS2 conducts to circulate the inductor current (free wheel). The synchronous PWM control block regulates the output voltage by modulating the conduction intervals of the upper and lower MOSFETs.

PWM Generator and MOSFET Drivers

This circuit is a one-chip solution (item 7U0A). It contains all the circuitry for two independent buck regulators (3V3 and 1V2). The MOSFETs 7U08, 7U02, 7U05 and 7U06 are the switching transistors, they are conducting alternatively.

- Time sequence 1: 7U08/7U02 is conducting; energy is stored in coil 5U01/5U00. The current is flowing from the +12VSW power supply source.
- Time sequence 2: 7U08/7U02 is blocked; energy is stored in coil 5U01/5U00.
- Time sequence 3: 7U05/7U06 is conducting, and the current circuit is now closed via 7U05/7U06, 5U01, 5U00, 2U06/2U0Z/2U07/2U0T/2U0U/2U0V, and the load. So the energy stored in the coil during time sequence T1 is consumed during sequence T3. The signal on the gate 7U05/7U06 is 180 degrees turned compared with the signal on the gate 7U08/7U02.

Voltage Booster

This circuit is build around capacitors 2U29 and 2U26, resistor 3U62/3UA1, diodes 6U01 and 6U00, and transistor 7U03.
It generates the +18 V boost voltage on pin 4 of item 7U00, to drive the "high-side" power MOS-FET 7U08/7U02. The voltage is generated only during normal operation of the converter; therefore, any drop in its value means an internal fault condition, which is sensed by the internal protection circuit. The AC component of the voltage on the source of transistor 7U08/7U02 is rectified by the diodes and added to the input voltage, resulting into the boost voltage. The resistor 3U02/3U1K limits the peak current through the rectifier diodes.

Over-current Detection

Over-current detection is done via components 3U05, 3U06, 3U15, 3U14, and 2U04 for the 3.3 V converter and 3U00, 3U01, 3U16, 3U17, and 2U00 for the 1.2 V converter.

Under-voltage Detection

There is an additional circuit (7U01-1, 7U01-2 and 6U04) to switch "Off" the 3.3 V converter in case the +12VS drops below 9 V.

Service Tips

- When a power MOS-FET is found defective, replace the other power MOS-FET as well.
- For a normal operation of the converter, it is important to check the switching frequency and the value of the boost voltage.

9.4 Additional Monitor DC/DC Converters

In the monitor, additional DC/DC receivers are located to eliminate a voltage drop across the interconnection cable between monitor and hub. Refer to diagrams M01A and M01B.

A +12V feedback-loop is built around items 2U09, 2U08, 3U04, 6U03, 3U07, 3U05 and 3U06.
A +3V feedback-loop is built around items 2U21, 3U12, 3U13, 3U14, 2U17 and 3U15.

Just as with the DC/DC converters in the hub, the circuit used is a so-called "synchronous buck converter". Switching frequency is approx. 300 kHz.

Following figures depict the additional Monitor DC/DC converters.

- Gain to obtain optimised channel decoder level. Control

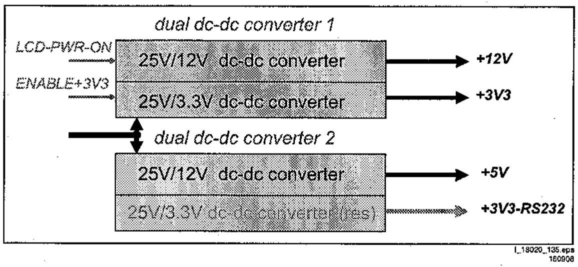

Figure 9-6 ESSENCE monitor DC/DC converters -1-

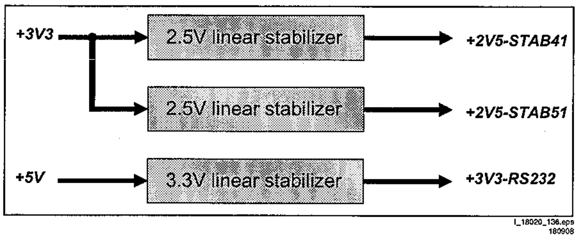

Figure 9-7 ESSENCE monitor DC/DC converters -2-

9.5 Front-End

Refer to figure "9-1 Architecture of Essence - Hub" earlier in this chapter for details. Refer also to block diagrams B02A, B02B and B02C.

9.5.1 Device specifications

Tuner (TD1716)

The tuner has the following specifications:

- Hybrid tuner with symmetrical IF output.
- Down conversion from RF to IF frequency (picture carrier 39.875 MHz at analogue reception, centre frequency 36.166 MHz at digital reception).
- AGC control signal is coming from master IF device (TDA9898).
- Only 5 V external supply needed (internal DC-DC conversion to 3.3 V).
- 4 MHz output is used by channel decoder (TDA10048) and master IF device (TDA9898).

The application in this chassis is as follows:

- I^2C address C0.
- Broadband AGC, no IF section.
- I^2C communication buffered via MUX.
- Gain to obtain optimised Master IF input level; AGC control is completely inside the tuner.
- Output level ca. 110 dBµV (for strong input signal).

Repair tip: after replacement of the tuner, the option code should be checked, even when the set appears to function correctly! Refer also to chapter 5 "Service Modes, Error Codes, and Fault Finding".

Master IF (TDA9898)

- Down conversion from IF to low-IF frequency.
- Down conversion from IF to SIF.
- CVBS output.

The application in this chassis is as follows:

- I^2C address 0x86.
- Down conversion from IF to low-IF frequency (5.166 MHz centre frequency).
- Advanced filtering (for further rejection of adjacent channels).
  signal is coming from channel decoder.

SAW filter

X6874D and X3451K

- Analogue sound for BG, I, DK, L, L'.
- DVB-T (digital reception sound **and** video).

For digital reception, the application in this chassis is as follows:

- Rejection of adjacent channels.
- Switching is done by Master IF (3 inputs).
- One SAW covering both 7 and 8 MHz channels.

X6774D

- Analogue video for BG, I, DK, L, L'.

Channel decoder (TDA10048) DVB-T

The channel decoder has the following specifications:

- I^2C address 0x10.
- Decoding from low-IF to MPEG transport stream.
- During decoding: de-modulation, de-interleaving and error correction.
- External clock buffer required.
- No start-up requirements.
- AGC monitor.

Channel decoder (TDA10023) DVB-C

The channel decoder has the following specifications:

- I^2C address 0x1C.
- Decoding from low-IF to MPEG transport stream.
- During decoding: de-modulation, de-interleaving and error correction.
- External clock buffer required.
- No start-up requirements.
- AGC monitor.

9.5.2 Digital signal processing (front-end)

Refer to figure "9-8 DVB-C signal broadcast reception block diagram" and "9-9 DVB-T signal broadcast reception block diagram" for details of digital signal processing.

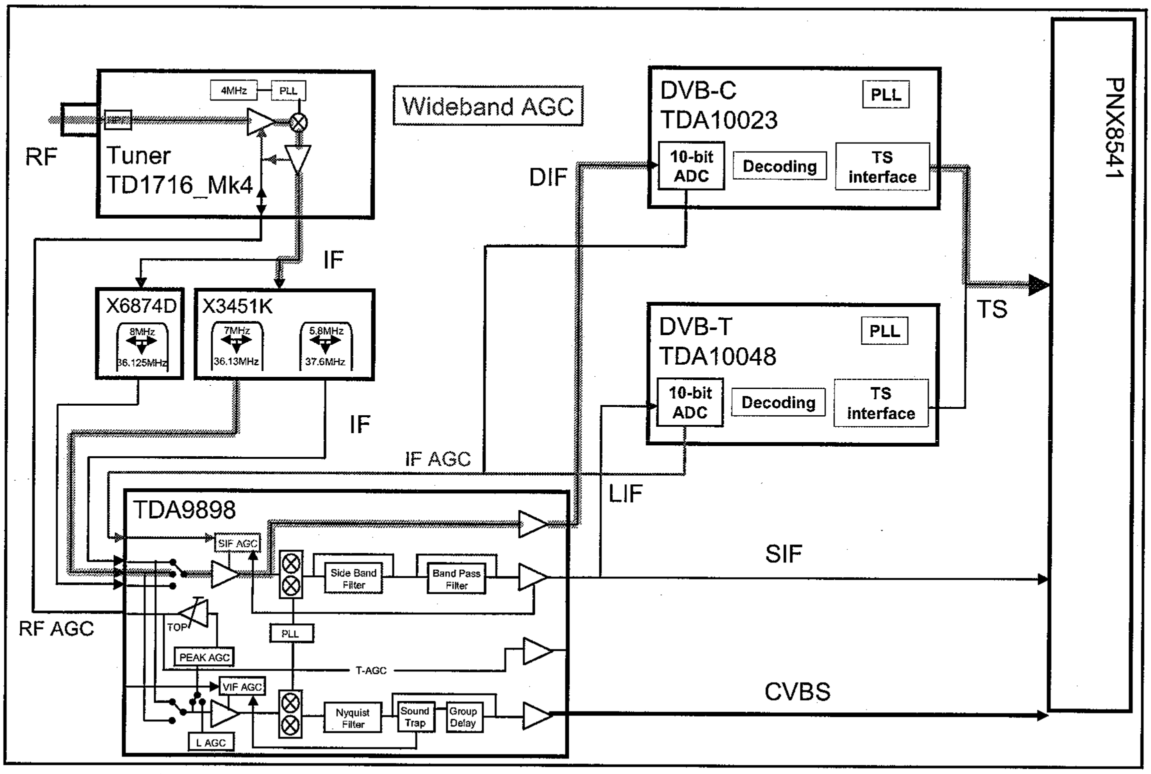
RF
Tuner
TD1716_Mk4
4MHz
PLL
HPF
Wideband AGC
DIF
IF
X6874D
8MHz
36.125MHz
X3451K
7MHz
36.13MHz
5.8MHz
37.6MHz
IF
IF AGC
LIF
DVB-C
TDA10023
PLL
10-bit ADC
Decoding
TS interface
DVB-T
TDA10048
PLL
10-bit ADC
Decoding
TS interface
TS
PNX8541
TDA9898
SIF AGC
Side Band Filter
Band Pass Filter
PLL
TOP
PEAK AGC
T-AGC
VIF AGC
L AGC
Nyquist Filter
Sound Trap
Group Delay
RF AGC
SIF
CVBS

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Figure 9-8 DVB-C signal broadcast reception block diagram

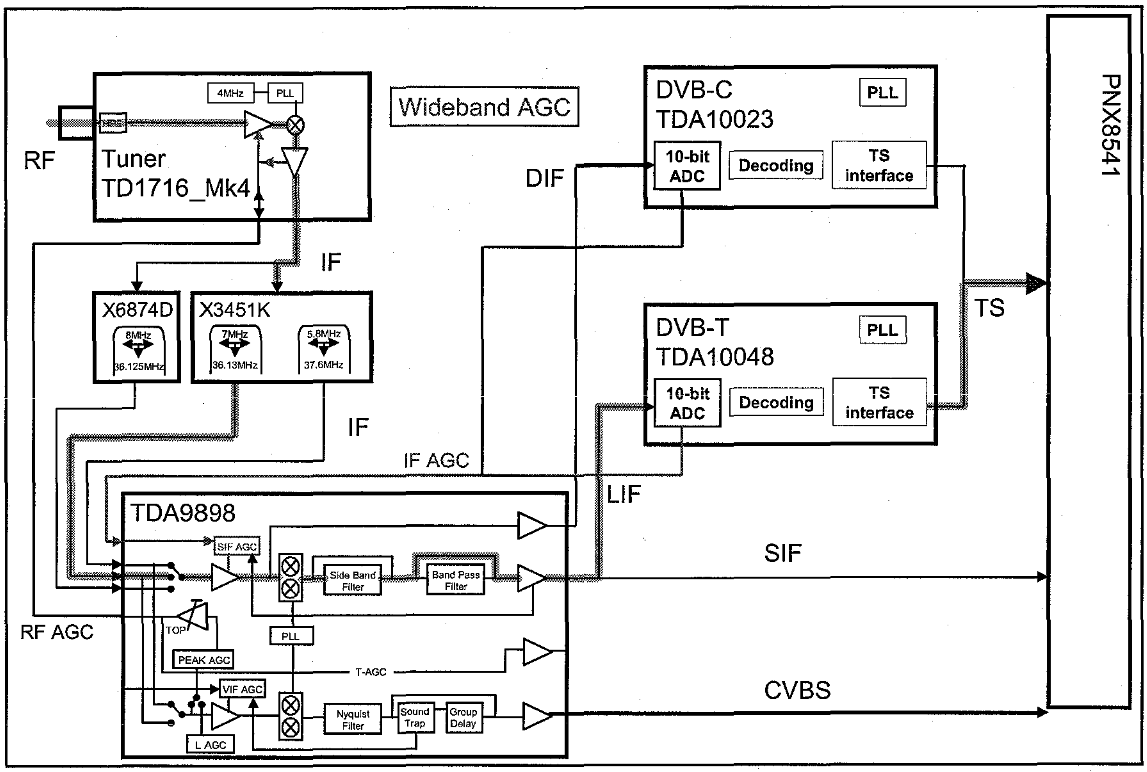
Wideband AGC
RF
Tuner
TD1716_Mk4
4MHz
PLL
IF
X6874D
8MHz
36.125MHz
X3451K
7MHz
36.13MHz
5.8MHz
37.6MHz
DVB-C
TDA10023
PLL
10-bit ADC
Decoding
TS interface
DIF
DVB-T
TDA10048
TS
IF AGC
LIF
TDA9898
SIF AGC
Side Band Filter
Band Pass Filter
SIF
RF AGC
TOP
PEAK AGC
T-AGC
VIF AGC
Nyquist Filter
Sound Trap
Group Delay
L AGC
CVBS
PNX8541

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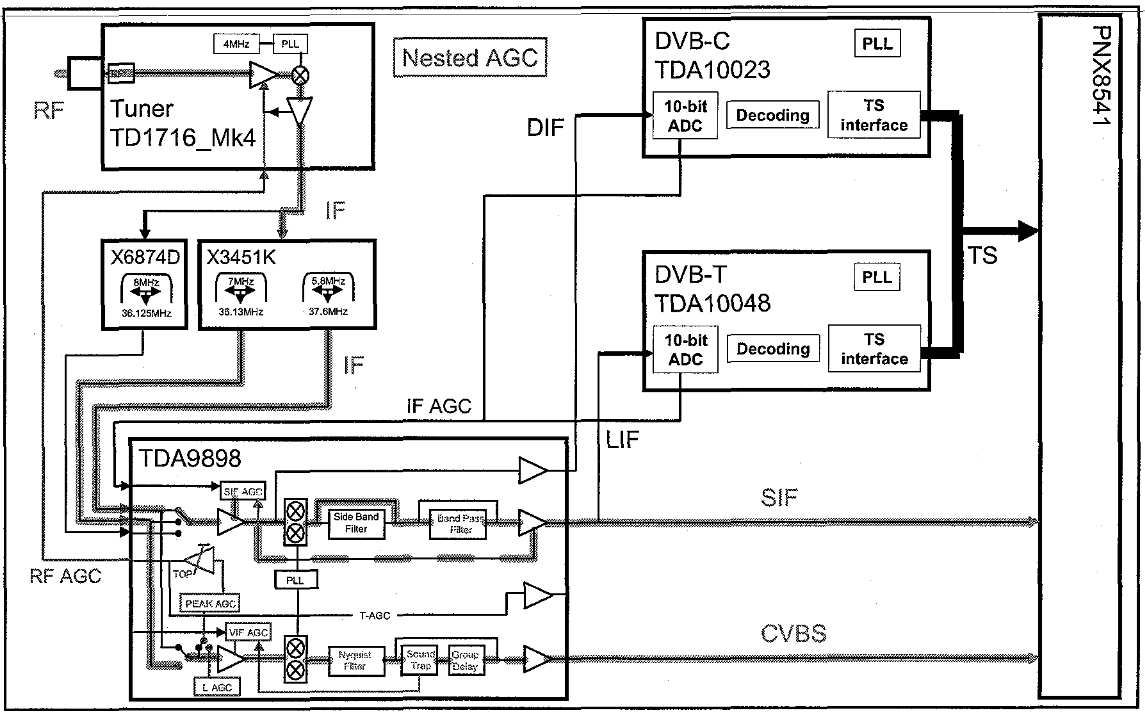
Figure 9-9 DVB-T signal broadcast reception block diagram

9.5.3 Analogue signal processing (front-end)

Refer to figure "9-10 Analog video broadcast reception block diagram" for details of analogue signal processing.


Nested AGC
RF
Tuner
TD1716_Mk4
4MHz
PLL
IF
X6874D
8MHz
36.125MHz
X3451K
7MHz
36.13MHz
5.8MHz
37.6MHz
DVB-C
TDA10023
PLL
10-bit ADC
Decoding
TS interface
DIF
DVB-T
TDA10048
TS
IF AGC
LIF
TDA9898
SIF AGC
Side Band Filter
Band Pass Filter
SIF
RF AGC
TOP
PEAK AGC
T-AGC
VIF AGC
Nyquist Filter
Sound Trap
Group Delay
L AGC
CVBS
PNX8541

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170308

Figure 9-10 Analog video broadcast reception block diagram

9.6 PNX85xx

In this chassis, the PNX85xx is responsible for the audio/video source decode functions and video improvement processing on both digital and analogue sources. It includes a multi-standard digital video decoder for MPEG2, and a multi-standard analogue video decoder for support of PAL, NTSC, and SECAM standards. Refer to diagram B04 for details.

9.6.1 Video Subsystem

Refer to figure "9-11 PNX85xx video flow diagram" for a clarification of the blocks that are used in this device.

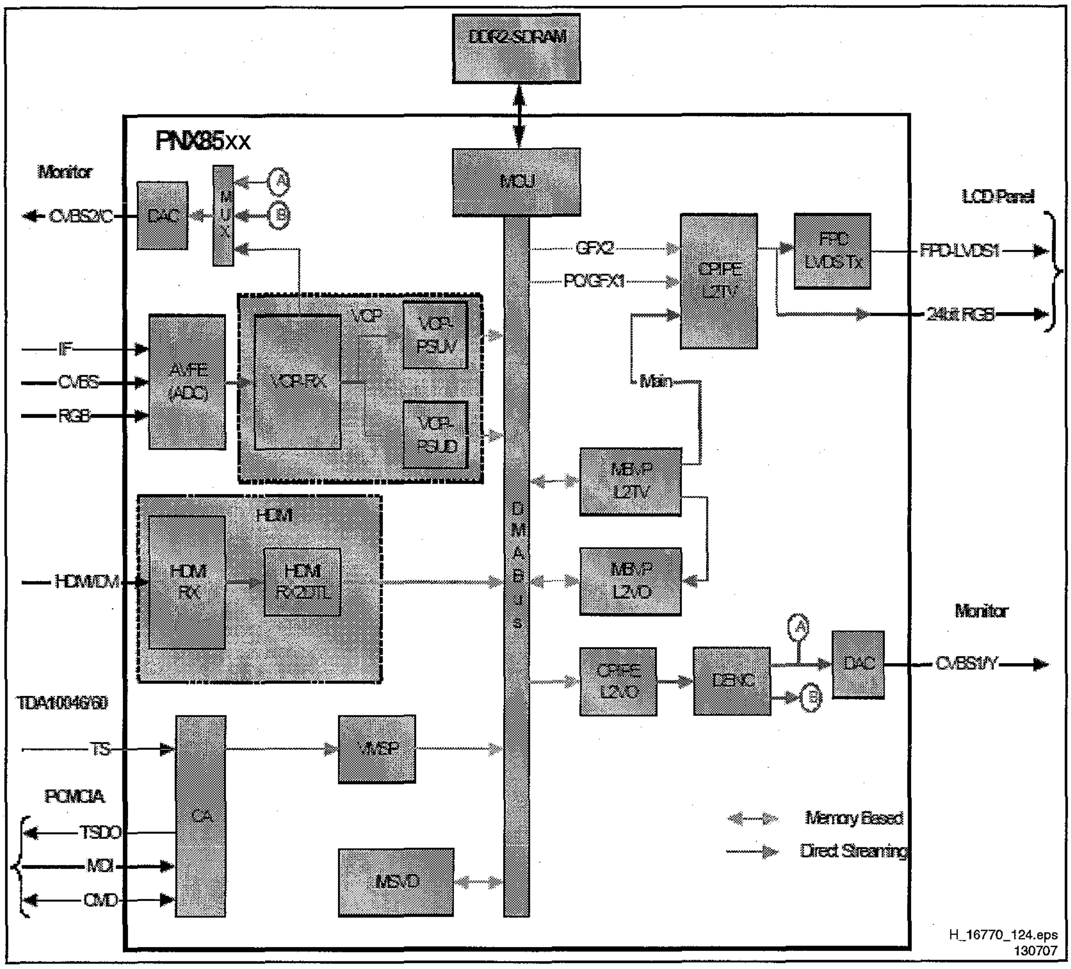
DDR2-SDRAM
PNX85xx
Monitor
CVBS2/C
DAC
MUX
A
B
MCU
IF
CVBS
RGB
AVFE (ADC)
VCP
VCP-RX
VCP-PSUV
VCP-PSUD
HDMI
HDMI/DVI
HDMI RX
HDMI RX2DTL
DMA BUS
TDA10046/60
TS
PCMCIA
TSDO
MDI
CMD
CA
VMSP
MSVD
GFX2
PO/GFX1
CPIPE L2TV
FPD LVDS Tx
LCD Panel
FPD-LVDS1
24bit RGB
Main
MBVP L2TV
MBVP L2VO
CPIPE L2VO
DENC
A
B
DAC
Monitor
CVBS1/Y
Memory Based
Direct Streaming
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Figure 9-11 PNX85xx video flow diagram

The Analogue Video Front-End (AVFE) provides the interface to external analogue baseband video sources and IF inputs. It supports the following inputs:
- 1fh - CVBS, Y/C, YPbPr, RGB.
- 2fh - YPbPr, RGB.
- IF - low-IF, SSIF.

The Video Capture Pipe (VCP) is used to capture analogue video inputs and consists of a number of blocks:
- The VCP-RX block that contains digital IF processing, a Video Decoder, a 3D-combfilter, and a VBI-Data Capture unit together with a number of smaller control functions.
- The VCP-PSUD which allows VBI data, such Teletext and Closed Captioning, to be stored in memory.
- The VCP-PSUV which allows captured video data to be stored in memory.

The HDMI receiver interface supports the capture of signals compliant with the HDMI V1.3 specification. It consists of two blocks:
- Block HDMI-RX contains the de-serializer, HDCP, audio and video data capture and info packet extraction, together with audio formatting.
- Block HDMI-RX2DTL allows captured video data to be stored in memory.

The Memory Based Video Processor TV (MBVP_L2TV) is used on the main video channel for de-interlacing and scaling of images, together with video measurement functions.

The Video Composition Pipe TV (CPIPE_L2TV) is used to perform picture improvements on video and merge the video layer and 2 graphics layers into a single stream.

The Flat Panel Display-LVDS (FPD-LVDS) provides a serial interface for 10-bit RGB output data towards the LCD panel.

The Memory Based Video Processor VO (MBVP_2LVO) is used on the main video channel for scaling of images for monitor out.

The Video Composition Pipe VO (CPIPE_VO) is used to merge a video and a graphics layer into a single stream together with insertion of VBI and CGMS data.

The Digital Encoder (DENC) supports encoding of a digital video stream from the CPIPE_VO into Analogue CVBS or Y/C.

9.6.2 Audio Subsystem

Refer to figure "9-12 PNX85xx audio flow diagram" for a clarification of the blocks that are used in this device.

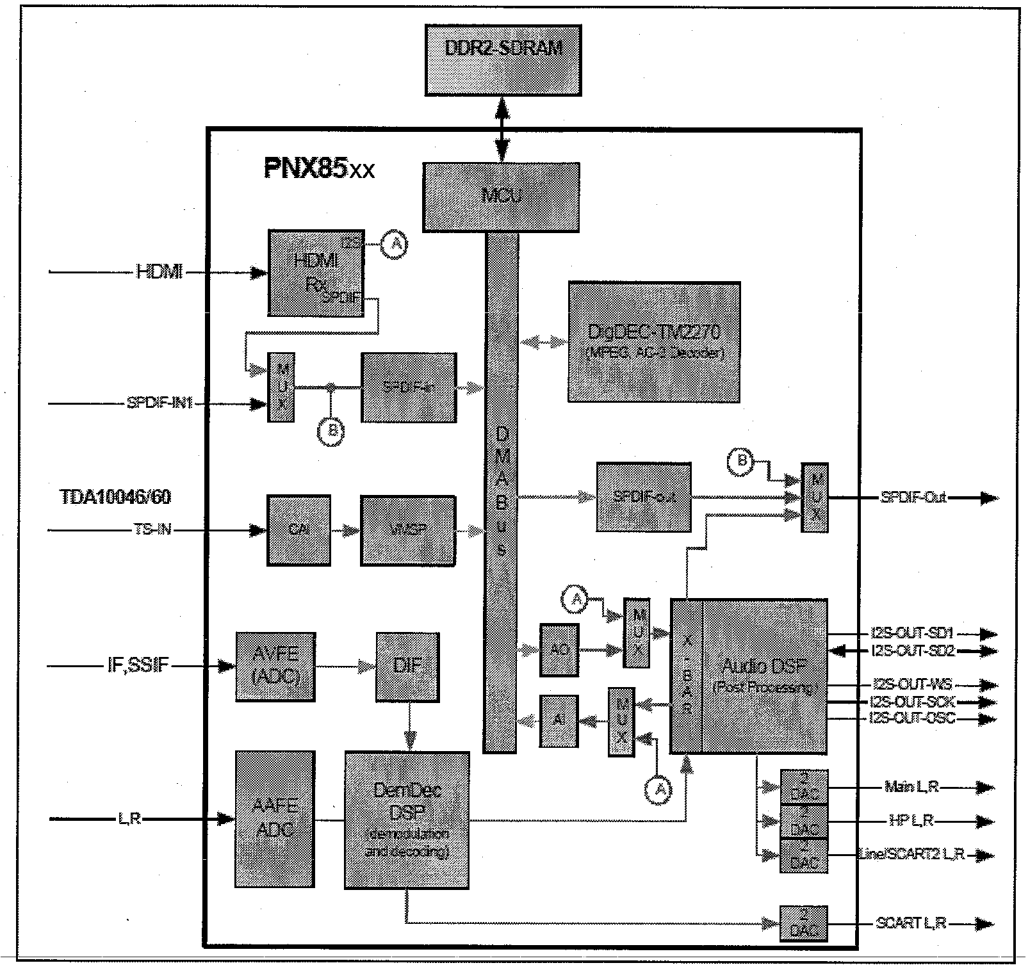
DDR2-SDRAM
PNX85xx
MCU
HDMI
HDMI Rx
I2S
SPDIF
A
SPDIF-IN1
MUX
SPDIF-in
B
DigDEC-TM2270
(MPEG, AC-3 Decoder)
DMA Bus
TDA10046/60
TS-IN
CAI
VMSP
SPDIF-out
B
MUX
SPDIF-Out
A
MUX
AO
AI
MUX
A
X-BAR
Audio DSP
(Post Processing)
I2S-OUT-SD1
I2S-OUT-SD2
I2S-OUT-WS
I2S-OUT-SCK
I2S-OUT-OSC
IF,SSIF
AVFE
(ADC)
DIF
L,R
AAFE
ADC
DemDec
DSP
(demodulation and decoding)
2 DAC
2 DAC
2 DAC
2 DAC
Main L,R
HP L,R
Line/SCART2 L,R
SCART L,R

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Figure 9-12 PNX85xx audio flow diagram

The Analogue Audio Front-End Input (AAFE) block is used to capture Baseband Audio Inputs.

The Sony/Philips Digital Interface (SPDIF) input is used to get compressed data into the system memory. The multiplexer in front of the block allows two possible sources of SPDIF signals.

The SPDIF Output is used to generate either PCM data or a compliant IEC-61937 compressed stream containing MPEG/Dolby Digital format.

The Audio Input (AI) block is used to transfer stereo audio (I^2S channel) from the Audio DSP into the system memory for "lip-sync" delay.

The Audio Output (AO) block supports output of up to four stereo I^2S channels. The AO is used to transfer data from the system memory to the Audio DSP, for post processing of the signal at a sampling frequency of 48 kHz (max.).

Demodulation & Decoding DSP is used for demodulation and decoding of all analogue terrestrial TV sound standards that the TV520 platform covers.

The Audio Post-Processing DSP supports DPLII together with volume and tone control, spatializers, and equalizers for 6 channels (max.)

Digital Audio Decoder DSP is used to decode digital compressed streams such as MPEG and AC-3. This runs as SW Codecs on the AV-DSP.

9.6.3 Audio-Video Codec Subsystem

The AV Codec subsystem consists of the modules required to capture and de-scramble Transport stream inputs together with decoding of Audio/video Streams. Refer to figure "PNX85xx video flow diagram" for a clarification.

The sub-system consists of the following modules:

The Conditional Access Interface block provides a direct interface towards a PCMCIA socket for Conditional Access. It supports both the DVB CI-CA Specification and the CableCard (POD) Interface.

The MPEG System Processor (VMSP) provides parsing an MPEG-2 transport stream, including de-scrambling, de-multiplexing and appropriate routing of data to the memory.

The Video MPEG Decoder (VMPG) performs MPEG2 decoding for both MP@ML and MP@HL streams.

9.6.4 Control and Compute Subsystem

Refer to figure “Control and compute subsystem” for a clarification of the blocks that are used in this device.

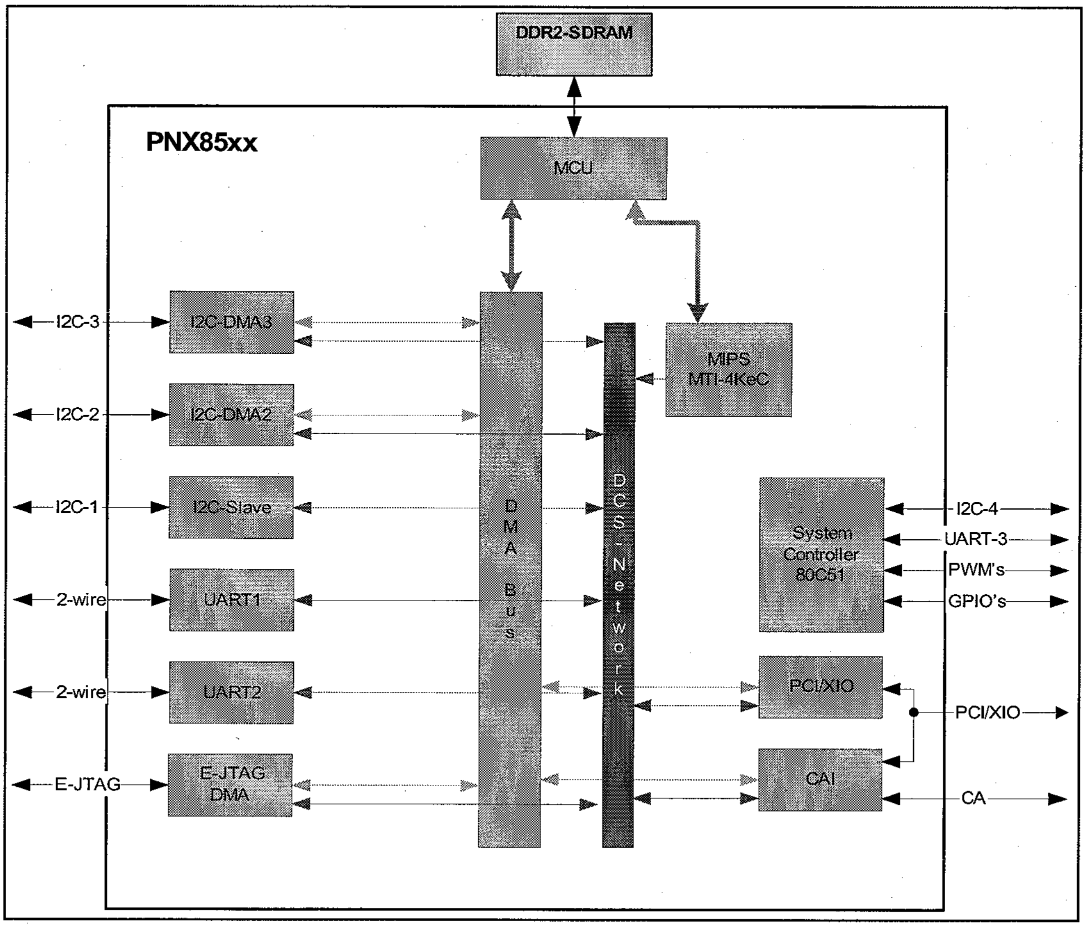

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Figure 9-13 Control and compute subsystem

The Control and compute subsystem consists of the main processor, control peripherals and the memory system.

The MIPS 4KEc is a 32-bit MIPS RISC core. It has direct access to connectivity peripherals to support system features via PCI, I^{2}C, UART or General Purpose I/O. A JTAG interface provides processor software debug capabilities.

The Memory Control Unit (MCU) is a 32-bit DDR2 SDRAM interface supporting DDR2-533 with an address range of 128 MB (max.).

The PCI/XIO interface supports PCI Rev2.2 and can be used to access 8/16-bit external NAND-Flash memory.

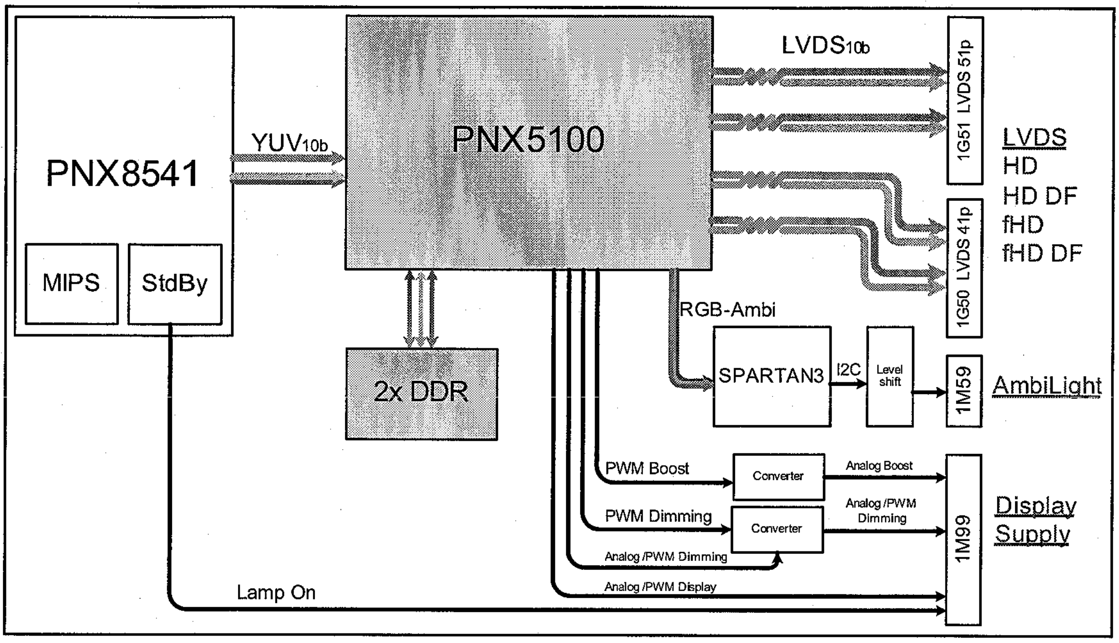
The Conditional Access Interface supports direct control and communication to the PC-Card attached to a PCMCIA interface. The interface supports the DVB CI-CA and CableCard specification.

9.7 Back-end

Refer to figures “9-1 Architecture of Essence - Hub” earlier in this chapter for details. Refer also to block diagrams B05, B05, B06 and AB.

In HD sets (50 / 100 Hz), the output signal coming from the PNX85xx is fed to the PNX5100 and then to the Spartan-3 FPGA for driving the AmbiLight units. The PNX5100 3 also generates the pulse-width modulated signal needed for the “Dimming Backlight” feature, which ensures additional motion sharpness. As some displays require an analogue signal to switch the LCD, a multiplexer is added to transform the pulse width modulated signal. An additional signal, coming from the PNX85xx, makes the selection between analogue and pulse-width modulation, depending on which display is used. Scanning back light displays require an analogue signal, and all other displays a pulse-width modulated.

Refer to figure “9-14 PNX5100 Detailed Video Block diagram”.



I_17660_145.eps
170308

Figure 9-14 PNX5100 Detailed Video Block diagram

9.7.1 PNX5100

The PNX5100 performs the following tasks:
- Picture quality improvement (Natural Motion, etc.).
- Video and graphics (On Screen Display) mixing.
- Up conversion from 50/60 to 100/120 Hz.
- Colour processing
- Sharpness processing
- Backlight control
- AmbiLight pre processing
- Switching On and Off of the display
- Pattern generator

The PNX5050 interfaces:
- Video input (CMOS).
- Graphics input (PCI).
- I^{2}C.
- Field memory (2 × DDR).
- Video output: LVDS (single, dual or quad) to display
- Backlight control: PWM for dimming and boost
- AmbiLight: CMOS sequential RGB to FPGA
- GPIO

Refer to figure “9-14 PNX5100 Detailed Video Block diagram” for details.

9.8 Audio

As a result of separation between monitor and supporting electronics (hub), some modifications are made w.r.t. previous chassis (Q529.1E LA/LB).

The delta’s are:
- All audio I/O, except side I/O, has been moved to a separate I/O panel.
- One HDMI connector less on SSB.
- Audio Amplifier is moved to Monitor panel (DPRX)
- Audio for the amplifier is sent via I^{2}S.
  The conversion to I^{2}S format is done in the FPGA.
- The amplifier type is the same as for the earlier Q529.1E LA/LB chassis.
- Application however is different as a single supply is used.
- An extra fuse is implemented in the audio supply on the monitor board as a result of the (long) supply cable
- Extra audio supply decoupling is implemented.
- DC-protection is self-contained: it will only affect the operation of the amplifier. The amplifier will go in a one-second switch on/switch off cycle when in protection.
- Audio DAC is added to convert the I^{2}S signal into the analog domain.

As a result of the audio application in this chassis, you can disconnect the speakers without the risk of damaging the amplifier. Also, the set will not go into protection anymore.

9.9 DLNA

Is an international, cross-industry collaboration of consumer electronics, computing industry and mobile device companies standard. The main objective of DLNA is the establishment of a wired and wireless inter operable network of personal computers (PC), consumer electronics (CE) and mobile devices in the home and on the road, enabling a seamless environment for sharing new digital media and content services. DLNA is focused on delivering an inter operability framework of design guidelines based on open industry standards to complete the cross-industry digital convergence. The TV522 platform is set up as Digital Media Player. It can find and play or display the content that is shared on your network by server devices. In this chassis, an Ethernet MAC/PHY for wired Ethernet is incorporated to support DLNA.

Main features:
- National Semiconductors DP83816
- Controlled over PCI interface
- Physical layer uses a top-entry RJ45 with integrated magnetics (UTP)
- Supports 10M and 100M (full and half duplex)
- Uses 3V3 only (divided into separate analog and digital supply planes)
- The network controller shares the interrupt with the USB host controller
- The network controller can access the DRAM to dump/fetch packets.

9.10 Abbreviation List

0/6/12	SCART switch control signal on A/V board. 0 = loop through (AUX to TV), 6 = play 16 : 9 format, 12 = play 4 : 3 format
2DNR	Spatial (2D) Noise Reduction
3DNR	Temporal (3D) Noise Reduction
AARA	Automatic Aspect Ratio Adaptation: algorithm that adapts aspect ratio to remove horizontal black bars; keeps the original aspect ratio
ACI	Automatic Channel Installation: algorithm that installs TV channels directly from a cable network by means of a predefined TXT page
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box
AM	Amplitude Modulation
ANR	Automatic Noise Reduction: one of the algorithms of Auto TV
AP	Asia Pacific
AR	Aspect Ratio: 4 : 3 or 16 : 9
ASF	Auto Screen Fit: algorithm that adapts aspect ratio to remove horizontal black bars without discarding video information
ATSC	Advanced Television Systems Committee, the digital TV standard in the USA
ATV	See Auto TV
Auto TV	A hardware and software control system that measures picture content, and adapts image parameters in a dynamic way
AV	External Audio Video
AVC	Audio Video Controller
AVIP	Audio Video Input Processor
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BLR	Board-Level Repair
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
B-TXT	Blue TeleteXT
C	Centre channel (audio)
CEC	Consumer Electronics Control bus: remote control bus on HDMI connections
CL	Constant Level: audio output to connect with an external amplifier
CLR	Component Level Repair
COLUMBUS	COlour LUMinance Baseband Universal Sub-system
ComPair	Computer aided rePair
CP	Connected Planet / Copy Protection
CSM	Customer Service Mode
CTI	Colour Transient Improvement: manipulates steepness of chroma transients
CVBS	Composite Video Blanking and Synchronization
DAC	Digital to Analogue Converter
DBE	Dynamic Bass Enhancement: extra low frequency amplification
DDC	See “E-DDC”
D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
DFI	Dynamic Frame Insertion
DFU	Directions For Use: owner's manual
DLNA	Digital Living Network Alliance
DMR	Digital Media Reader: card reader
DNM	Digital Natural Motion
DNR	Digital Noise Reduction: noise reduction feature of the set
DRAM	Dynamic RAM
DRM	Digital Rights Management
DSP	Digital Signal Processing
DST	Dealer Service Tool: special remote control designed for service technicians
DTCP	Digital Transmission Content Protection; A protocol for protecting digital audio/video content that is traversing a high speed serial bus, such as IEEE-1394
DVB-C	Digital Video Broadcast - Cable
DVB-T	Digital Video Broadcast - Terrestrial
DVD	Digital Versatile Disc
DVI(-d)	Digital Visual Interface (d= digital only)
E-DDC	Enhanced Display Data Channel (VESA standard for communication channel and display). Using E-DDC, the video source can read the EDID information form the display.
EDID	Extended Display Identification Data (VESA standard)
EEPROM	Electrically Erasable and Programmable Read Only Memory
EMI	Electro Magnetic Interference
EPLD	Erasable Programmable Logic Device
EU	Europe
EXT	EXTernal (source), entering the set by SCART or by cinches (jacks)
FBL	Fast BLanking: DC signal accompanying RGB signals
FDS	Full Dual Screen (same as FDW)
FDW	Full Dual Window (same as FDS)
FLASH	FLASH memory
FM	Field Memory or Frequency Modulation
FPGA	Field-Programmable Gate Array
FTV	Flat TeleVision
Gb/s	Giga bits per second
G-TXT	Green TeleteXT
GPIO	General Purpose Input/Output
H	H_sync to the module
HD	High Definition
HDD	Hard Disk Drive
HDCP	High-bandwidth Digital Content Protection: A “key” encoded into the HDMI/DVI signal that prevents video data piracy. If a source is HDCP coded and connected via HDMI/DVI without the proper HDCP decoding, the picture is put into a “snow vision” mode or changed to a low resolution. For normal content distribution the source and the display device must be enabled for HDCP “software key” decoding.
HDMI	High Definition Multimedia Interface
HP	HeadPhone
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I^2C	Inter IC bus
I^2D	Inter IC Data bus
I^2S	Inter IC Sound bus
IF	Intermediate Frequency
Interlaced	Scan mode where two fields are used to form one frame. Each field contains

	half the number of the total amount of lines. The fields are written in “pairs”, causing line flicker.
IR	Infra Red
IRQ	Interrupt Request
ITU-656	The ITU Radio communication Sector (ITU-R) is a standards body subcommittee of the International Telecommunication Union relating to radio communication. ITU-656 (a.k.a. SDI), is a digitized video format used for broadcast grade video. Uncompressed digital component or digital composite signals can be used. The SDI signal is self-synchronizing, uses 8 bit or 10 bit data words, and has a maximum data rate of 270 Mbit/s, with a minimum bandwidth of 135 MHz.
ITV	Institutional TeleVision; TV sets for hotels, hospitals etc.
JOP	Jaguar Output Processor
LS	Last Status; The settings last chosen by the customer and read and stored in RAM or in the NVM. They are called at start-up of the set to configure it according to the customer's preferences
LATAM	Latin America
LCD	Liquid Crystal Display
LED	Light Emitting Diode
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
LORE	LOcal REgression approximation noise reduction
LPL	LG.Philips LCD (supplier)
LS	Loudspeaker
LVDS	Low Voltage Differential Signalling
Mbps	Mega bits per second
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
MIPS	Microprocessor without Interlocked Pipeline-Stages; A RISC-based microprocessor
MOP	Matrix Output Processor
MOSFET	Metal Oxide Silicon Field Effect Transistor, switching device
MPEG	Motion Pictures Experts Group
MPIF	Multi Platform InterFace
MUTE	MUTE Line
NC	Not Connected
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.
NTC	Negative Temperature Coefficient, non-linear resistor
NTSC	National Television Standard Committee. Colour system mainly used in North America and Japan. Colour carrier NTSC M/N = 3.579545 MHz, NTSC 4.43 = 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non-Volatile Memory: IC containing TV related data such as alignments
O/C	Open Circuit
OSD	On Screen Display
OTC	On screen display Teletext and Control; also called Artistic (SAA5800)
P50	Project 50: communication protocol between TV and peripherals
PAL	Phase Alternating Line. Colour system mainly used in West Europe (colour carrier = 4.433619 MHz) and South America (colour carrier PAL M = 3.575612 MHz and PAL N = 3.582056 MHz)
PCB	Printed Circuit Board (same as “PWB”)
PCM	Pulse Code Modulation
PDP	Plasma Display Panel
PFC	Power Factor Corrector (or Pre-conditioner)
PIP	Picture In Picture
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
POR	Power On Reset, signal to reset the uP
Progressive Scan	Scan mode where all scan lines are displayed in one frame at the same time, creating a double vertical resolution.
PTC	Positive Temperature Coefficient, non-linear resistor
PWB	Printed Wiring Board (same as “PCB”)
PWM	Pulse Width Modulation
QRC	Quasi Resonant Converter
QTNR	Quality Temporal Noise Reduction
QVCP	Quality Video Composition Processor
RAM	Random Access Memory
RGB	Red, Green, and Blue. The primary colour signals for TV. By mixing levels of R, G, and B, all colours (Y/C) are reproduced.
RC	Remote Control
RC5 / RC6	Signal protocol from the remote control receiver
RESET	RESET signal
ROM	Read Only Memory
R-TXT	Red TeleteXT
SAM	Service Alignment Mode
S/C	Short Circuit
SCART	Syndicat des Constructeurs d'Appareils Radiorecepteurs et Televisieurs
SCL	Serial Clock I^2C
SCL-F	CLock Signal on Fast I^2C bus
SD	Standard Definition
SDA	Serial Data I^2C
SDA-F	DAta Signal on Fast I^2C bus
SDI	Serial Digital Interface, see “ITU-656”
SDRAM	Synchronous DRAM
SECAM	SÉquence Couleur Avec Mémoire. Colour system mainly used in France and East Europe. Colour carriers= 4.406250 MHz and 4.250000 MHz
SIF	Sound Intermediate Frequency
SMPS	Switched Mode Power Supply
SoC	System on Chip
SOG	Sync On Green
SOPS	Self Oscillating Power Supply
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
SSB	Small Signal Board
STBY	STand-BY
SVGA	800 × 600 (4 : 3)
SVHS	Super Video Home System
SW	Software
SWAN	Spatial temporal Weighted Averaging Noise reduction
SXGA	1280 × 1024
TFT	Thin Film Transistor
THD	Total Harmonic Distortion
TMDS	Transmission Minimized Differential Signalling
TXT	TeleteXT
TXT-DW	Dual Window with TeleteXT
UI	User Interface
uP	Microprocessor
UXGA	1600 × 1200 (4 : 3)

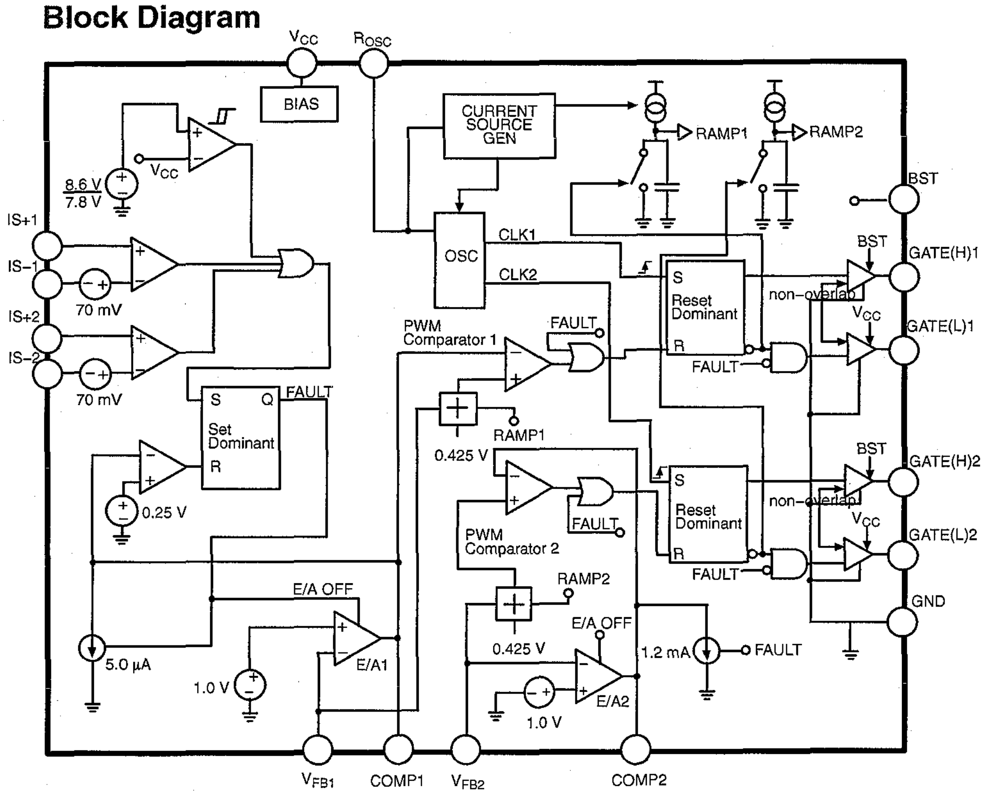
V	V-sync to the module
VCR	Video Cassette Recorder
VESA	Video Electronics Standards Association
VGA	640 × 480 (4 : 3)
VL	Variable Level out: processed audio output toward external amplifier
VSB	Vestigial Side Band; modulation method
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
WXGA	1280 × 768 (15 : 9)
XTAL	Quartz crystal
XGA	1024 × 768 (4 : 3)
Y	Luminance signal
Y/C	Luminance (Y) and Chrominance (C) signal
YPbPr	Component video. Luminance and scaled colour difference signals (B-Y and R-Y)
YUV	Component video

9.11 IC Data Sheets

This section shows the internal block diagrams and pin configurations of ICs that are drawn as “black boxes” in the electrical diagrams (with the exception of “memory” and “logic” ICs).

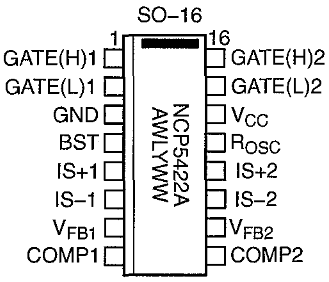
9.11.1 Diagram B01A, B01C, NCP5422AD (IC 7U0A, 7U0L)

Block Diagram



V_CC
R_OSC
BIAS
CURRENT SOURCE GEN
RAMP1
RAMP2
BST
GATE(H)1
GATE(L)1
GATE(H)2
GATE(L)2
GND
8.6 V
7.8 V
V_CC
IS+1
IS-1
IS+2
IS-2
70 mV
70 mV
OSC
CLK1
CLK2
PWM Comparator 1
FAULT
S Q
Set Dominant
R
FAULT
0.25 V
S
Reset Dominant
R
FAULT
non-overlap
V_CC
0.425 V
RAMP1
PWM Comparator 2
FAULT
RAMP2
S
Reset Dominant
R
FAULT
non-overlap
V_CC
E/A OFF
E/A1
5.0 µA
1.0 V
0.425 V
E/A OFF
E/A2
1.0 V
1.2 mA
FAULT
V_FB1
COMP1
V_FB2
COMP2

Pin Configuration



SO–16
1
16
GATE(H)1
GATE(L)1
GND
BST
IS+1
IS–1
V_FB1
COMP1
GATE(H)2
GATE(L)2
V_CC
R_OSC
IS+2
IS–2
V_FB2
COMP2
NCP5422A
AWLYWW

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

F_15400_129.eps
240505

Figure 9-15 Internal block diagram and pin configuration

9.11.2 Diagram B01B, LD2985BM33R (IC7U73)

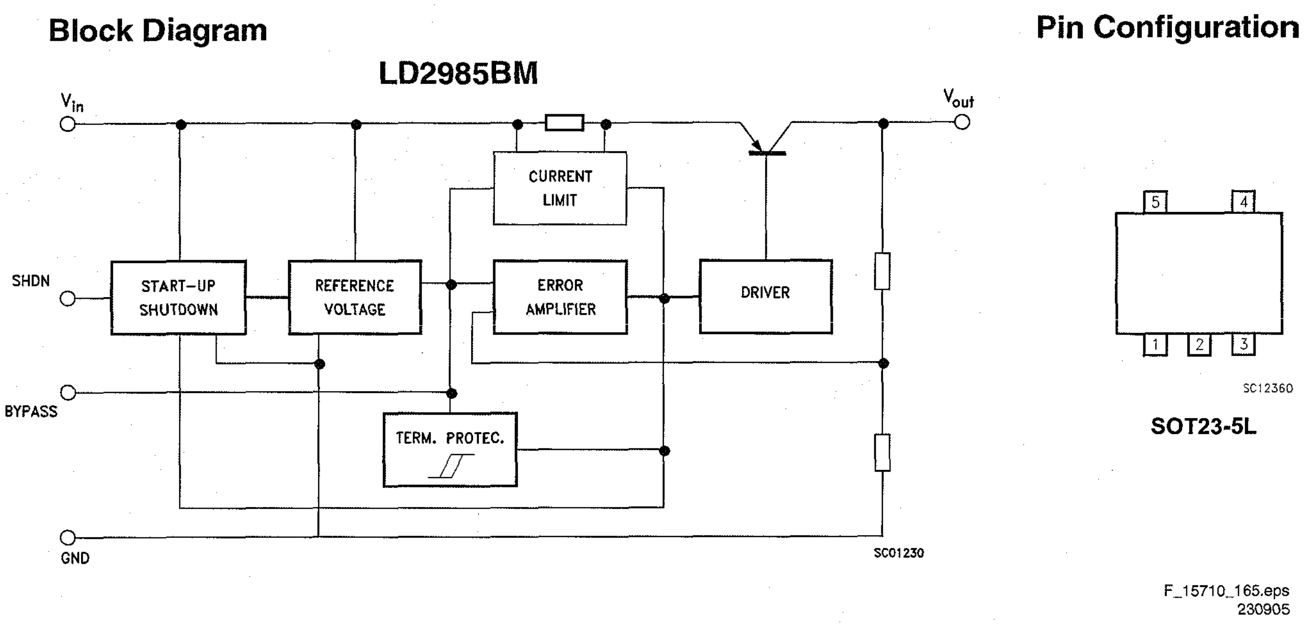
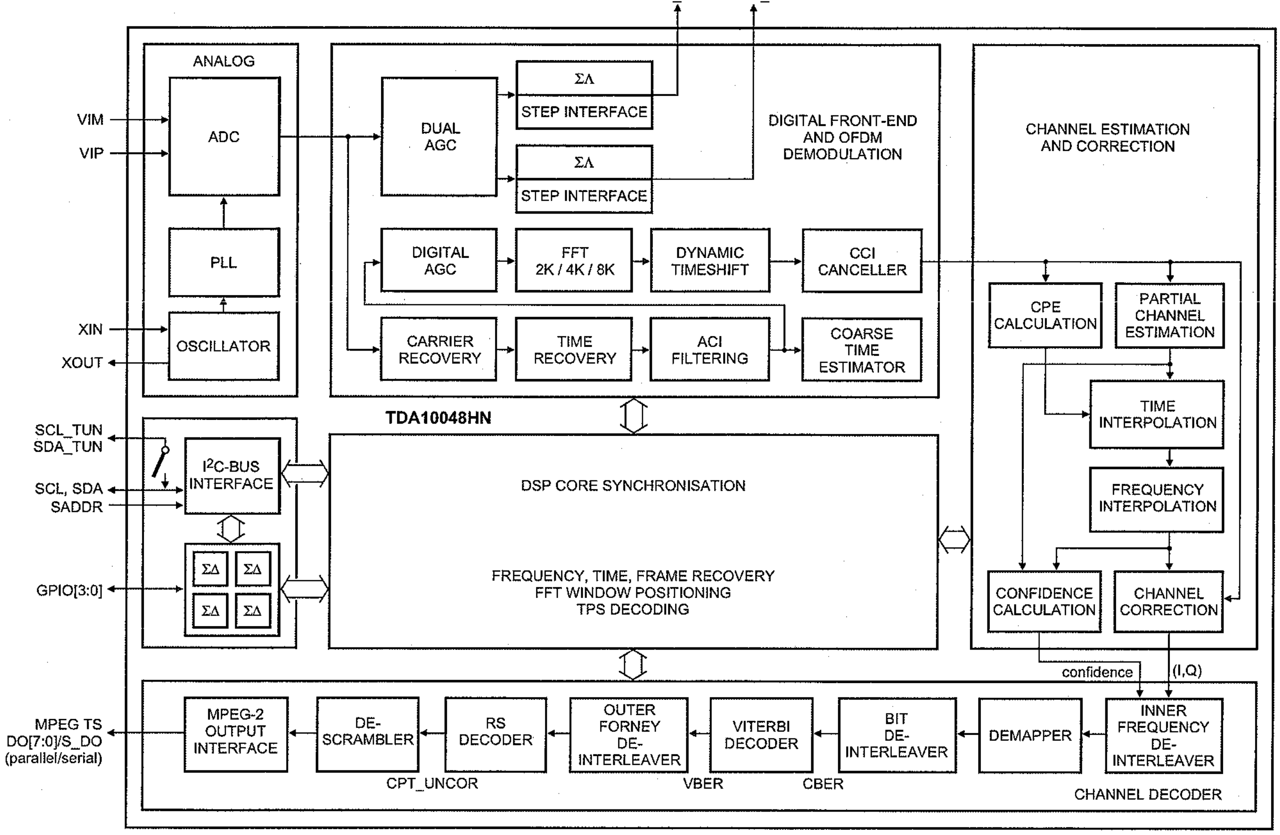

Block Diagram
LD2985BM
V_{in}
V_{out}
CURRENT LIMIT
SHDN
START-UP SHUTDOWN
REFERENCE VOLTAGE
ERROR AMPLIFIER
DRIVER
BYPASS
TERM. PROTEC.
GND
SC01230
Pin Configuration
5
4
1
2
3
SC12360
SOT23-5L
F_15710_165.eps
230905

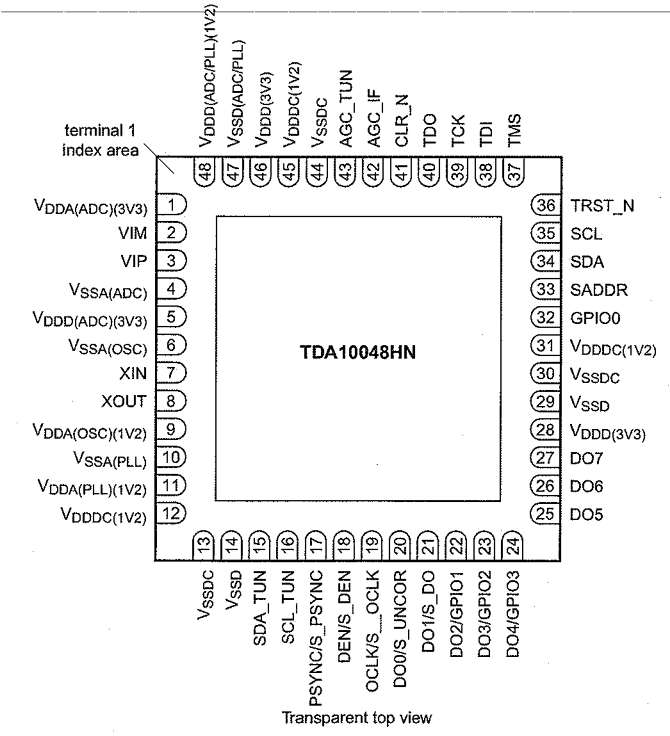
Figure 9-16 Internal block diagram and pin configuration

9.11.3 Diagram B02A, TDA10048HN (IC7T17-1)

Block Diagram


AGC_TUN
AGC_IF
ANALOG
VIM
VIP
ADC
PLL
XIN
XOUT
OSCILLATOR
DUAL AGC
ΣΔ
STEP INTERFACE
ΣΔ
STEP INTERFACE
DIGITAL FRONT-END AND OFDM DEMODULATION
DIGITAL AGC
FFT 2K / 4K / 8K
DYNAMIC TIMESHIFT
CCI CANCELLER
CARRIER RECOVERY
TIME RECOVERY
ACI FILTERING
COARSE TIME ESTIMATOR
CHANNEL ESTIMATION AND CORRECTION
CPE CALCULATION
PARTIAL CHANNEL ESTIMATION
TIME INTERPOLATION
FREQUENCY INTERPOLATION
CONFIDENCE CALCULATION
CHANNEL CORRECTION
TDA10048HN
SCL_TUN
SDA_TUN
SCL, SDA
SADDR
I2C-BUS INTERFACE
GPIO[3:0]
ΣΔ
ΣΔ
ΣΔ
ΣΔ
DSP CORE SYNCHRONISATION
FREQUENCY, TIME, FRAME RECOVERY
FFT WINDOW POSITIONING
TPS DECODING
confidence
(I,Q)
MPEG TS
DO[7:0]/S_DO
(parallel/serial)
MPEG-2 OUTPUT INTERFACE
DE-SCRAMBLER
RS DECODER
OUTER FORNEY DE-INTERLEAVER
VITERBI DECODER
BIT DE-INTERLEAVER
DEMAPPER
INNER FREQUENCY DE-INTERLEAVER
CPT_UNCOR
VBER
CBER
CHANNEL DECODER

Pin Configuration

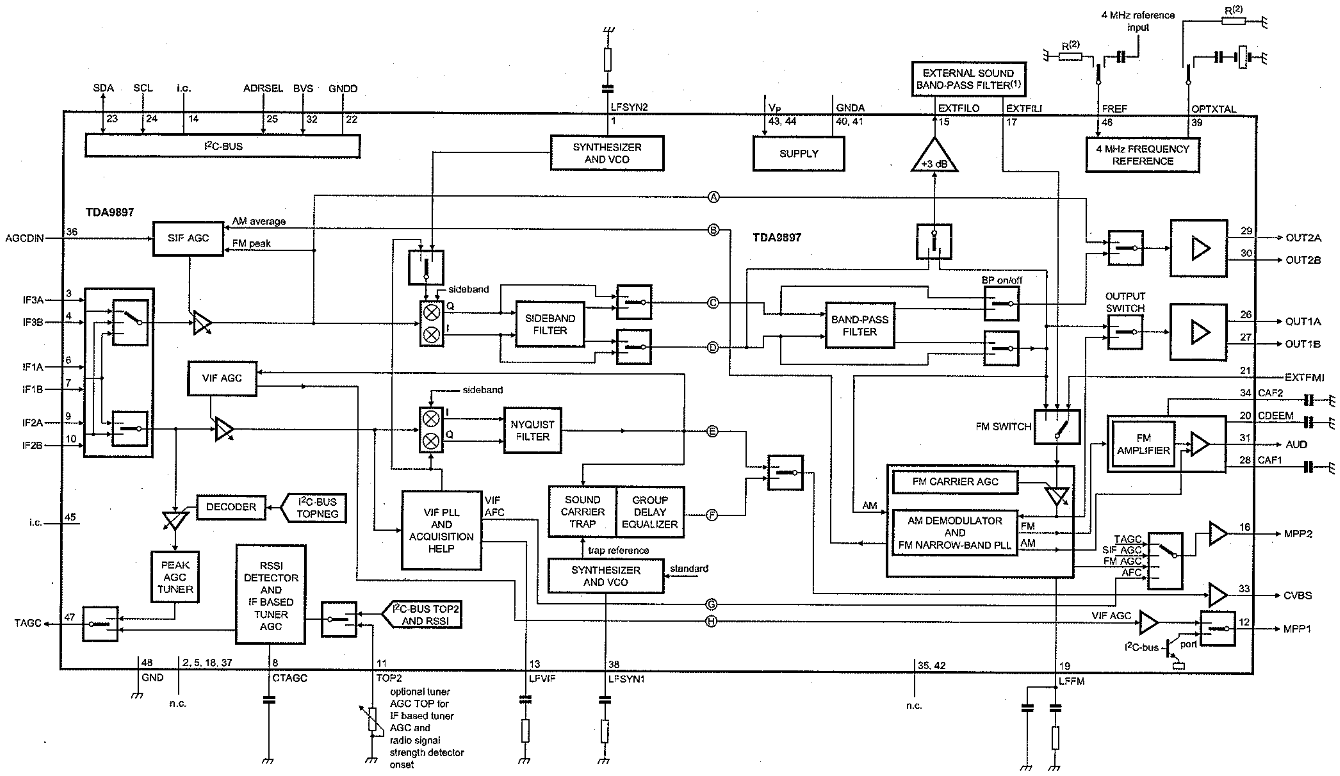

terminal 1 index area
TDA10048HN
1 VDDA(ADC)(3V3)
2 VIM
3 VIP
4 VSSA(ADC)
5 VDDD(ADC)(3V3)
6 VSSA(OSC)
7 XIN
8 XOUT
9 VDDA(OSC)(1V2)
10 VSSA(PLL)
11 VDDA(PLL)(1V2)
12 VDDDC(1V2)
13 VSSDC
14 VSSD
15 SDA_TUN
16 SCL_TUN
17 PSYNC/S_PSYNC
18 DEN/S_DEN
19 OCLK/S__OCLK
20 DO0/S_UNCOR
21 DO1/S_DO
22 DO2/GPIO1
23 DO3/GPIO2
24 DO4/GPIO3
25 DO5
26 DO6
27 DO7
28 VDDD(3V3)
29 VSSD
30 VSSDC
31 VDDDC(1V2)
32 GPIO0
33 SADDR
34 SDA
35 SCL
36 TRST_N
37 TMS
38 TDI
39 TCK
40 TDO
41 CLR_N
42 AGC_IF
43 AGC_TUN
44 VSSDC
45 VDDDC(1V2)
46 VDDD(3V3)
47 VSSD(ADC/PLL)
48 VDDD(ADC/PLL)(1V2)
Transparent top view

H_16800_127.eps
090507

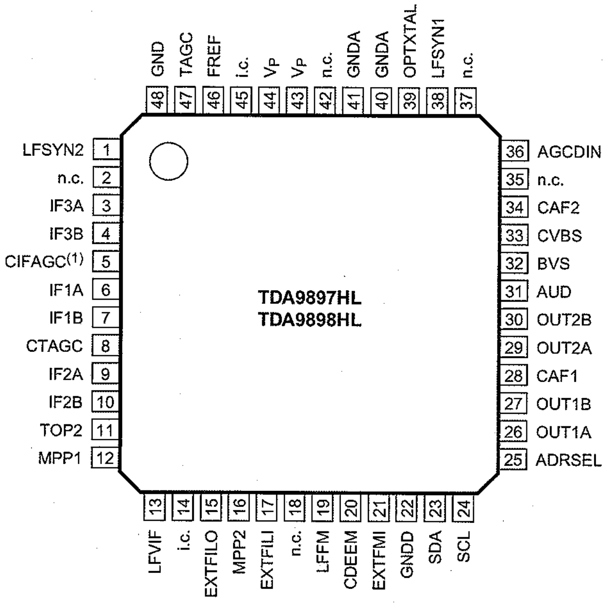
Figure 9-17 Internal block diagram and pin configuration

9.11.4 Diagram B02B, TDA9898HL (IC7T57)

Block Diagram


SDA
SCL
i.c.
ADRSEL
BVS
GNDD
23
24
14
25
32
22
I²C-BUS
LFSYN2
1
SYNTHESIZER AND VCO
Vp
43, 44
GNDA
40, 41
SUPPLY
EXTERNAL SOUND BAND-PASS FILTER(1)
EXTFILO
15
EXTFILI
17
+3 dB
4 MHz reference input
R(2)
FREF
46
OPTXTAL
39
4 MHz FREQUENCY REFERENCE
TDA9897
AGCDIN
36
SIF AGC
AM average
FM peak
IF3A
IF3B
IF1A
IF1B
IF2A
IF2B
3
4
6
7
9
10
sideband
Q
I
SIDEBAND FILTER
BP on/off
BAND-PASS FILTER
OUTPUT SWITCH
29
OUT2A
30
OUT2B
26
OUT1A
27
OUT1B
21
EXTFMI
34
CAF2
20
CDEEM
31
AUD
28
CAF1
VIF AGC
NYQUIST FILTER
FM SWITCH
FM AMPLIFIER
FM CARRIER AGC
AM
AM DEMODULATOR AND FM NARROW-BAND PLL
FM
i.c.
45
DECODER
I²C-BUS TOPNEG
VIF PLL AND ACQUISITION HELP
VIF AFC
SOUND CARRIER TRAP
GROUP DELAY EQUALIZER
trap reference
SYNTHESIZER AND VCO
standard
TAGC
SIF AGC
FM AGC
AFC
16
MPP2
33
CVBS
VIF AGC
12
MPP1
I²C-bus
port
PEAK AGC TUNER
RSSI DETECTOR AND IF BASED TUNER AGC
I²C-BUS TOP2 AND RSSI
TAGC
47
48
GND
2, 5, 18, 37
n.c.
8
CTAGC
11
TOP2
optional tuner AGC TOP for IF based tuner AGC and radio signal strength detector onset
13
LFVIF
38
LFSYN1
35, 42
n.c.
19
LFFM
A
B
C
D
E
F
G
H

Pin Configuration

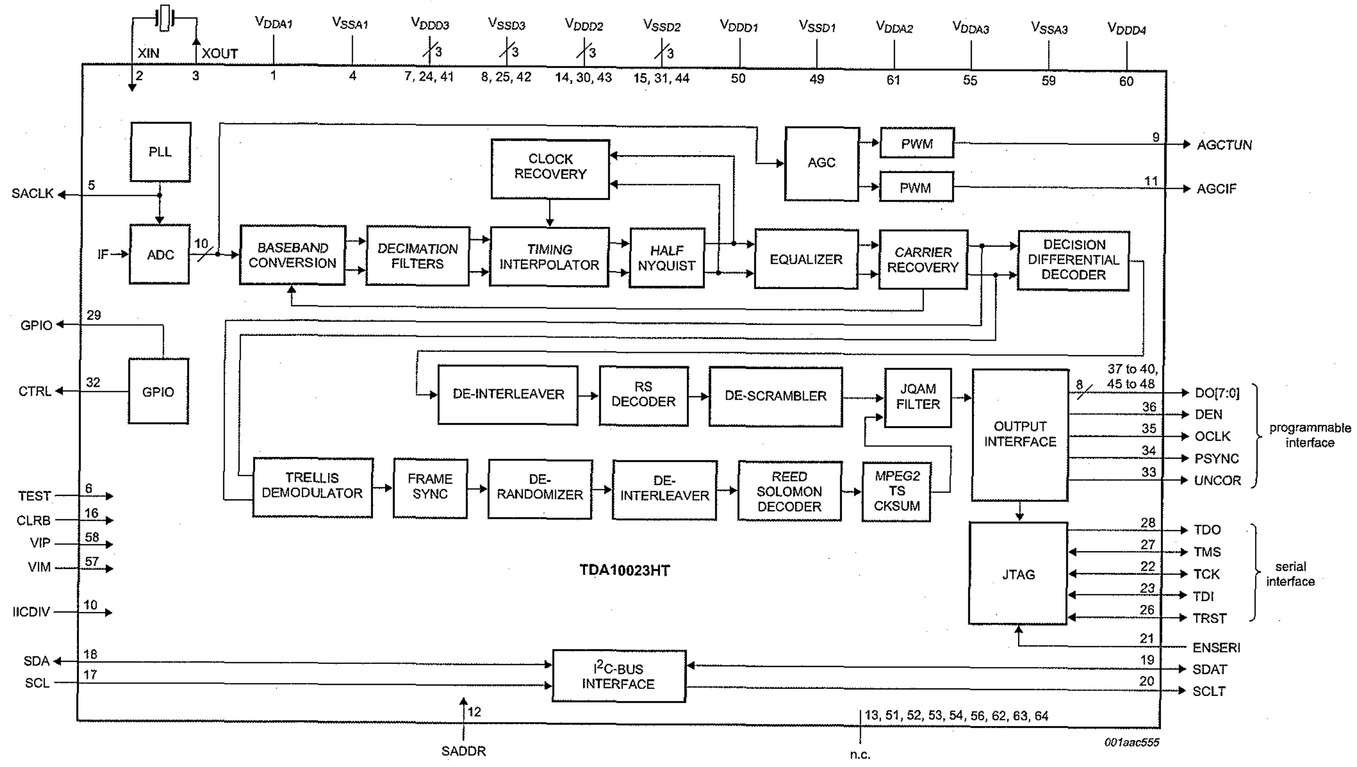

GND
TAGC
FREF
i.c.
Vp
Vp
n.c.
GNDA
GNDA
OPTXTAL
LFSYN1
n.c.
48
47
46
45
44
43
42
41
40
39
38
37
LFSYN2 1
n.c. 2
IF3A 3
IF3B 4
CIFAGC(1) 5
IF1A 6
IF1B 7
CTAGC 8
IF2A 9
IF2B 10
TOP2 11
MPP1 12
36 AGCDIN
35 n.c.
34 CAF2
33 CVBS
32 BVS
31 AUD
30 OUT2B
29 OUT2A
28 CAF1
27 OUT1B
26 OUT1A
25 ADRSEL
TDA9897HL
TDA9898HL
13
14
15
16
17
18
19
20
21
22
23
24
LFVIF
i.c.
EXTFILO
MPP2
EXTFILI
n.c.
LFFM
CDEEM
EXTFMI
GNDD
SDA
SCL

H_16800_029.eps
111007

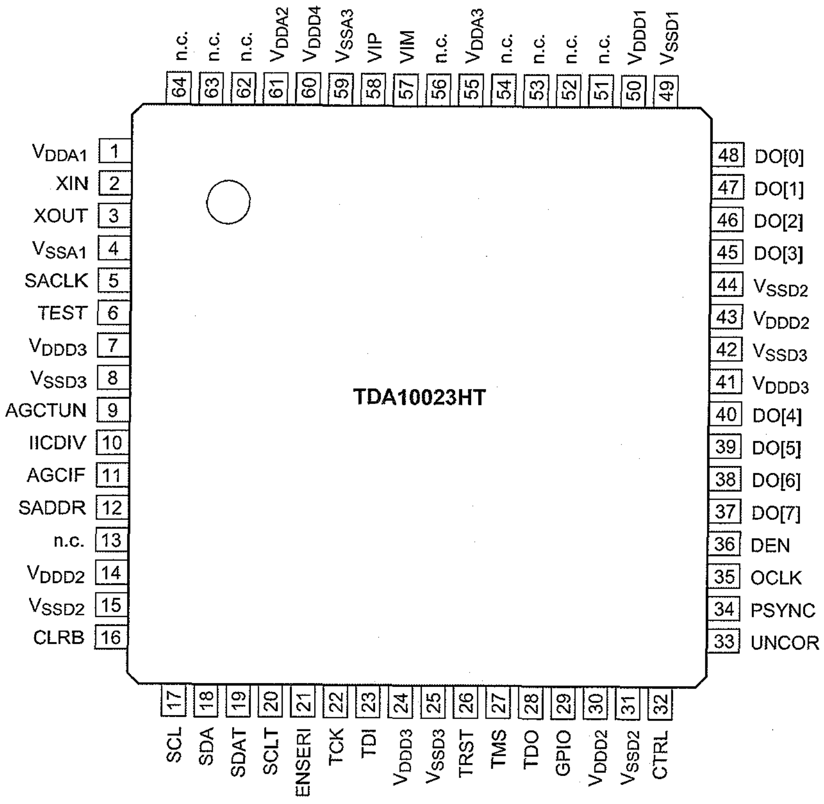
Figure 9-18 Pin configuration

9.11.5 Diagram B02C, TDA10023HT (IC7TA4)

Block Diagram


XIN
XOUT
VDDA1
VSSA1
VDDD3
VSSD3
VDDD2
VSSD2
VDDD1
VSSD1
VDDA2
VDDA3
VSSA3
VDDD4
2
3
1
4
7, 24, 41
8, 25, 42
14, 30, 43
15, 31, 44
50
49
61
55
59
60
PLL
CLOCK RECOVERY
AGC
PWM
PWM
AGCTUN
AGCIF
SACLK
IF
ADC
BASEBAND CONVERSION
DECIMATION FILTERS
TIMING INTERPOLATOR
HALF NYQUIST
EQUALIZER
CARRIER RECOVERY
DECISION DIFFERENTIAL DECODER
GPIO
CTRL
GPIO
DE-INTERLEAVER
RS DECODER
DE-SCRAMBLER
JQAM FILTER
OUTPUT INTERFACE
37 to 40, 45 to 48
DO[7:0]
DEN
OCLK
PSYNC
UNCOR
programmable interface
TRELLIS DEMODULATOR
FRAME SYNC
DE-RANDOMIZER
DE-INTERLEAVER
REED SOLOMON DECODER
MPEG2 TS CKSUM
JTAG
TDO
TMS
TCK
TDI
TRST
serial interface
ENSERI
TEST
CLRB
VIP
VIM
IICDIV
TDA10023HT
SDA
SCL
I2C-BUS INTERFACE
SDAT
SCLT
SADDR
13, 51, 52, 53, 54, 56, 62, 63, 64
n.c.
001aac555

Pin Configuration

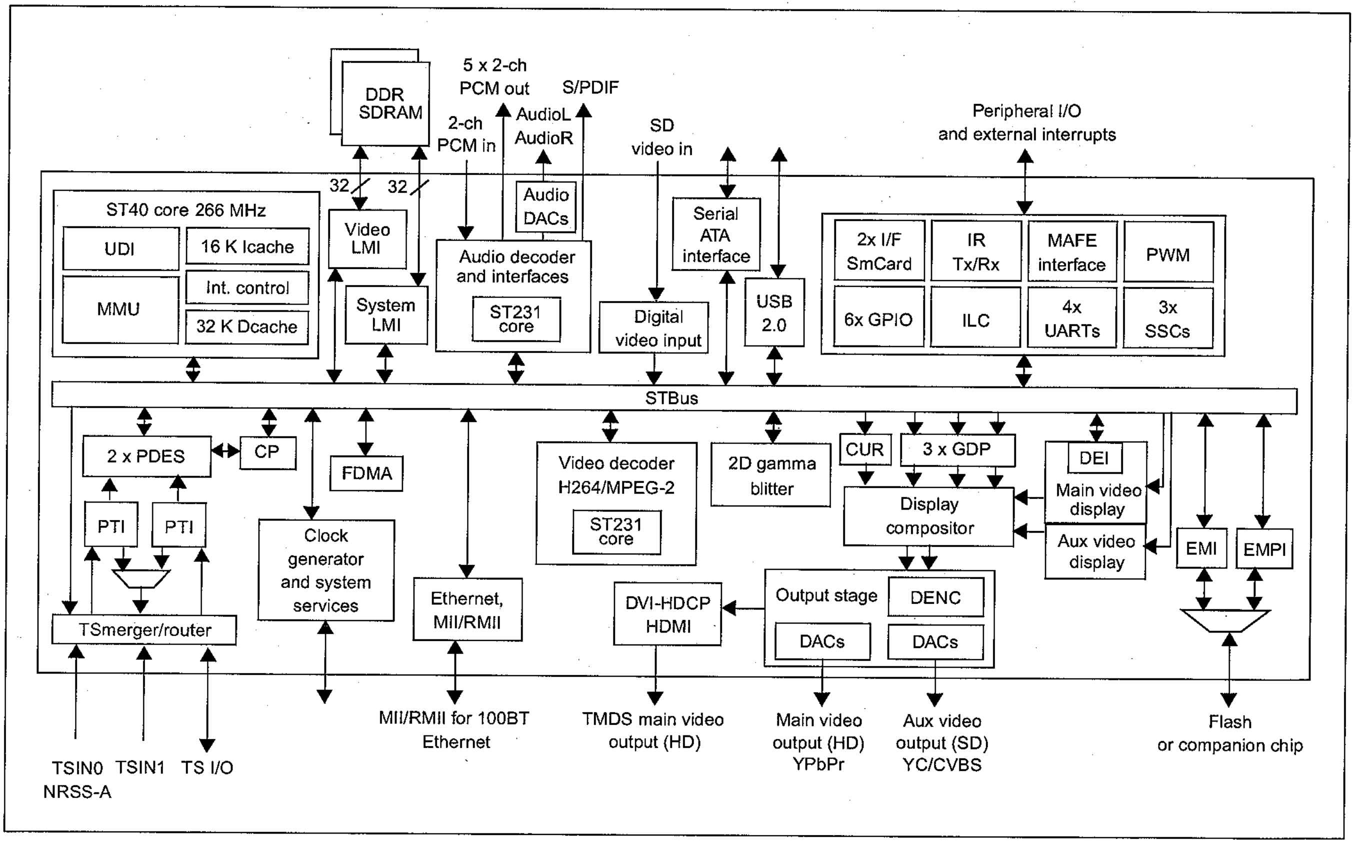

TDA10023HT
1 VDDA1
2 XIN
3 XOUT
4 VSSA1
5 SACLK
6 TEST
7 VDDD3
8 VSSD3
9 AGCTUN
10 IICDIV
11 AGCIF
12 SADDR
13 n.c.
14 VDDD2
15 VSSD2
16 CLRB
17 SCL
18 SDA
19 SDAT
20 SCLT
21 ENSERI
22 TCK
23 TDI
24 VDDD3
25 VSSD3
26 TRST
27 TMS
28 TDO
29 GPIO
30 VDDD2
31 VSSD2
32 CTRL
33 UNCOR
34 PSYNC
35 OCLK
36 DEN
37 DO[7]
38 DO[6]
39 DO[5]
40 DO[4]
41 VDDD3
42 VSSD3
43 VDDD2
44 VSSD2
45 DO[3]
46 DO[2]
47 DO[1]
48 DO[0]
49 VSSD1
50 VDDD1
51 n.c.
52 n.c.
53 n.c.
54 n.c.
55 VDDA3
56 n.c.
57 VIM
58 VIP
59 VSSA3
60 VDDD4
61 VDDA2
62 n.c.
63 n.c.
64 n.c.

H_17650_072.eps
150108

Figure 9-19 Internal block diagram and pin configuration

9.11.6 Diagram B03x, STi7100 (IC7A00)

Block Diagram

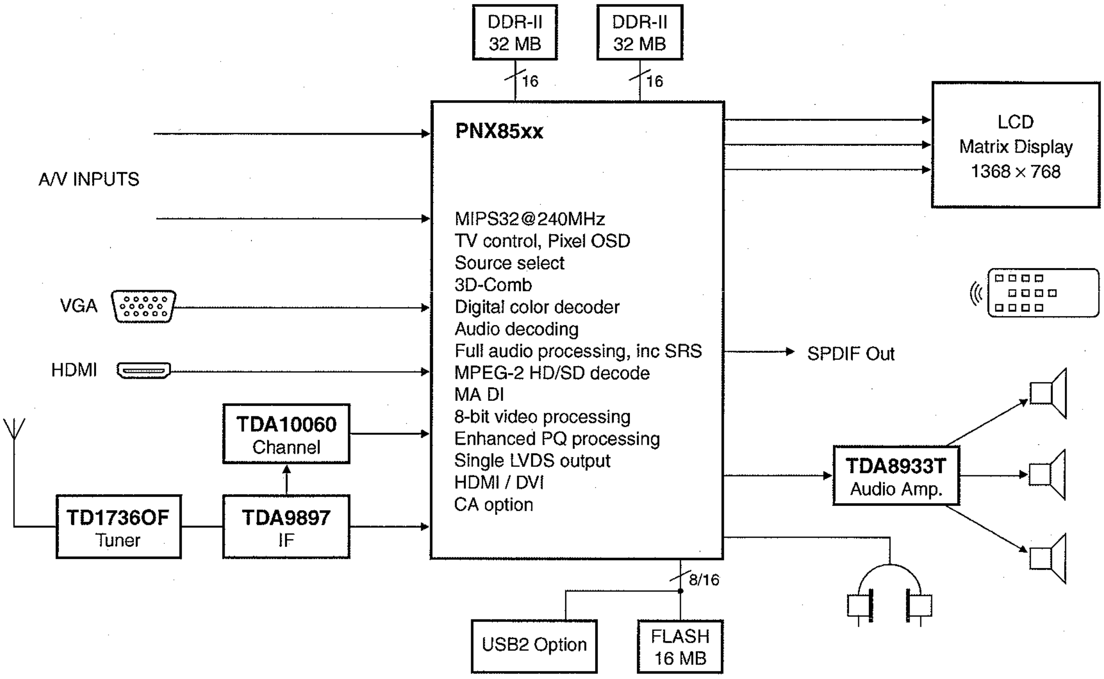

DDR
SDRAM
5 x 2-ch
PCM out
S/PDIF
2-ch
PCM in
AudioL
AudioR
SD
video in
Peripheral I/O
and external interrupts
32
32
ST40 core 266 MHz
UDI
16 K Icache
MMU
Int. control
32 K Dcache
Video
LMI
System
LMI
Audio
DACs
Audio decoder
and interfaces
ST231
core
Serial
ATA
interface
Digital
video input
USB
2.0
2x I/F
SmCard
IR
Tx/Rx
MAFE
interface
PWM
6x GPIO
ILC
4x
UARTs
3x
SSCs
STBus
2 x PDES
CP
FDMA
PTI
PTI
Clock
generator
and system
services
TSmerger/router
Ethernet,
MII/RMII
Video decoder
H264/MPEG-2
ST231
core
2D gamma
blitter
CUR
3 x GDP
DEI
Main video
display
Display
compositor
Aux video
display
EMI
EMPI
DVI-HDCP
HDMI
Output stage
DENC
DACs
DACs
TSIN0
NRSS-A
TSIN1
TS I/O
MII/RMII for 100BT
Ethernet
TMDS main video
output (HD)
Main video
output (HD)
YPbPr
Aux video
output (SD)
YC/CVBS
Flash
or companion chip

H_16780_085.eps
070907

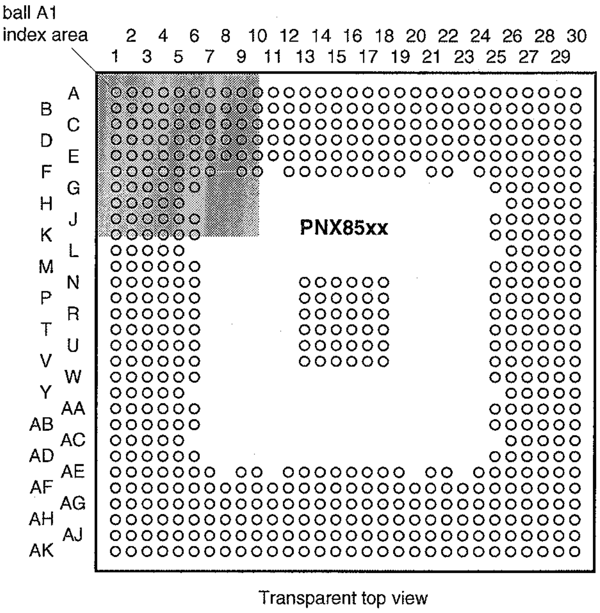
Figure 9-20 Internal block diagram and pin configuration

9.11.7 Diagram B04x, PNX85xx (IC 7H00)

Block Diagram


DDR-II
32 MB
16
DDR-II
32 MB
16
PNX85xx
A/V INPUTS
VGA
HDMI
MIPS32@240MHz
TV control, Pixel OSD
Source select
3D-Comb
Digital color decoder
Audio decoding
Full audio processing, inc SRS
MPEG-2 HD/SD decode
MA DI
8-bit video processing
Enhanced PQ processing
Single LVDS output
HDMI / DVI
CA option
LCD
Matrix Display
1368 x 768
SPDIF Out
TDA10060
Channel
TD1736OF
Tuner
TDA9897
IF
TDA8933T
Audio Amp.
8/16
USB2 Option
FLASH
16 MB

Pin Configuration

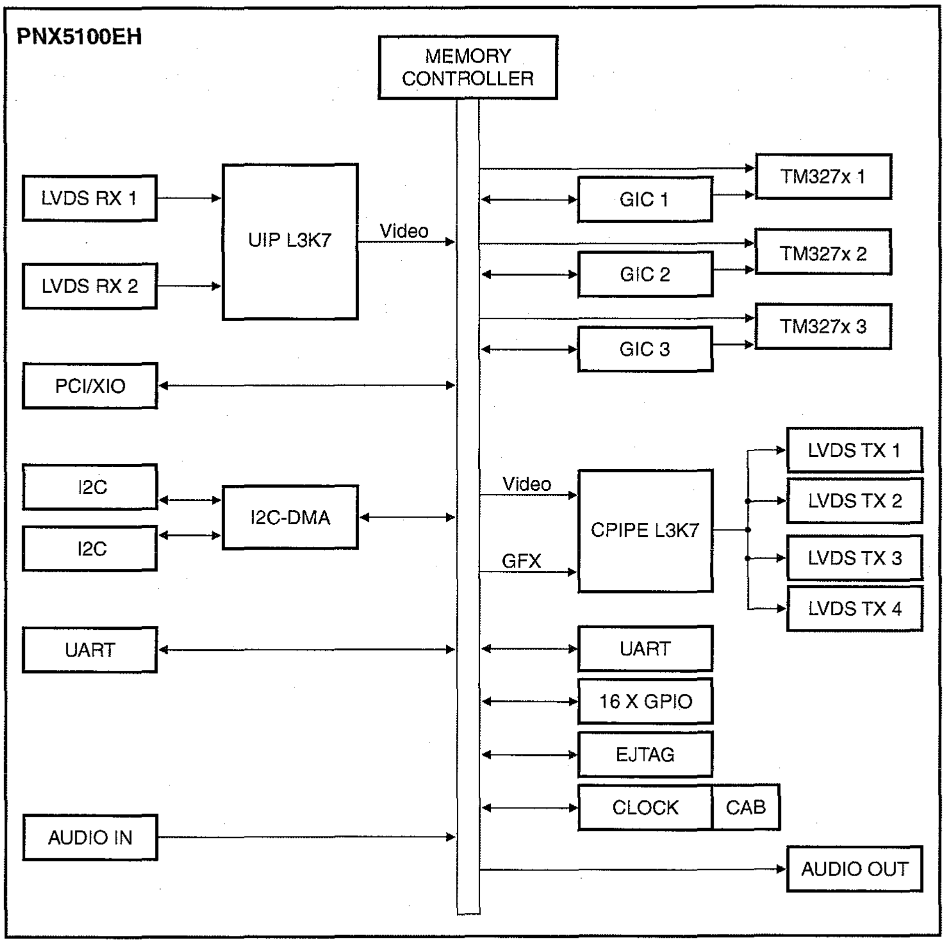

ball A1
index area
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF AG AH AJ AK
PNX85xx
Transparent top view

H_16800_128.eps
230707

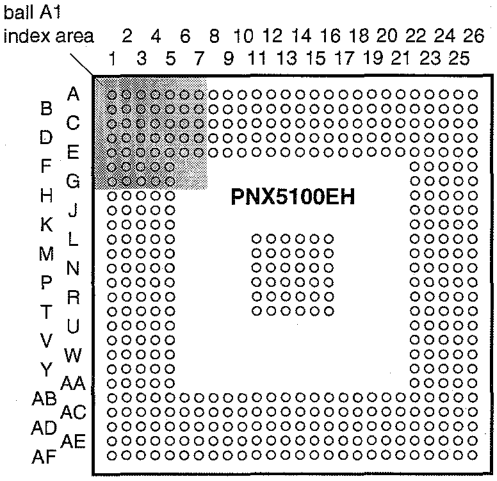
Figure 9-21 Pin configuration

9.11.8 Diagram B05x, PNX5100 (IC 7C00)

Block Diagram


PNX5100EH
MEMORY CONTROLLER
LVDS RX 1
LVDS RX 2
UIP L3K7
Video
PCI/XIO
I2C
I2C
I2C-DMA
UART
AUDIO IN
TM327x 1
GIC 1
TM327x 2
GIC 2
TM327x 3
GIC 3
Video
GFX
CPIPE L3K7
LVDS TX 1
LVDS TX 2
LVDS TX 3
LVDS TX 4
UART
16 X GPIO
EJTAG
CLOCK
CAB
AUDIO OUT

Pin Configuration

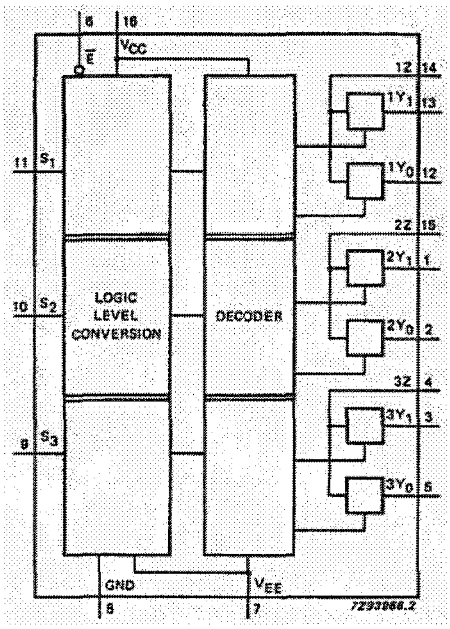

ball A1 index area
2 4 6 8 10 12 14 16 18 20 22 24 26
1 3 5 7 9 11 13 15 17 19 21 23 25
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF
PNX5100EH

I_17660_149.eps
180308

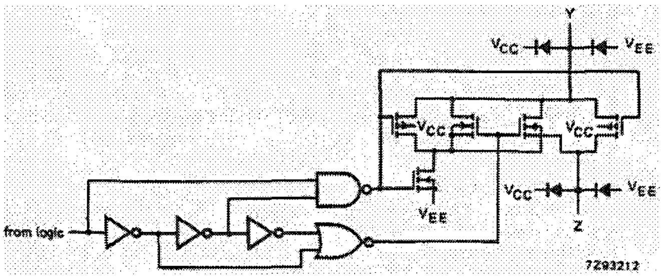
Figure 9-22 Pin configuration

9.11.9 Diagram B08A, 74HC4053PW (IC7E02)

Block Diagram


6
16
E̅
VCC
1Z 14
1Y1 13
1Y0 12
2Z 15
2Y1 1
2Y0 2
3Z 4
3Y1 3
3Y0 5
11 S1
10 S2
9 S3
LOGIC LEVEL CONVERSION
DECODER
GND 8
VEE 7
7Z93966.2

74HC4053PW


Y
VCC
VEE
VCC
VCC
VCC
VEE
VCC
VEE
Z
from logic
7Z93212

Pin Configuration

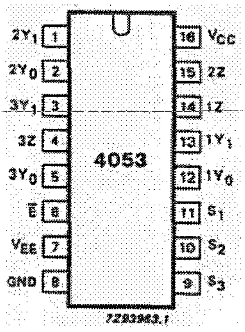

2Y1 1
2Y0 2
3Y1 3
3Z 4
3Y0 5
E̅ 6
VEE 7
GND 8
16 VCC
15 2Z
14 1Z
13 1Y1
12 1Y0
11 S1
10 S2
9 S3
4053
7Z93963.1

Fig.1 Pin configuration.

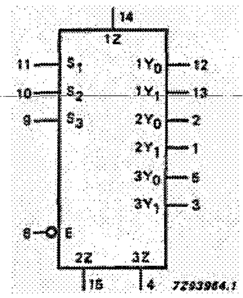

14
1Z
11 S1
10 S2
9 S3
1Y0 12
1Y1 13
2Y0 2
2Y1 1
3Y0 5
3Y1 3
6 E
2Z 15
3Z 4
7Z93964.1

Fig.2 Logic symbol.

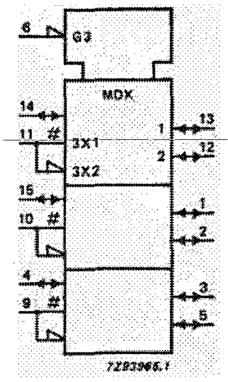

6
G3
MDX
14
11
3X1
3X2
1
2
13
12
15
10
1
2
4
9
3
5
7Z93965.1

Fig.3 IEC logic symbol.

I_18020_140.eps
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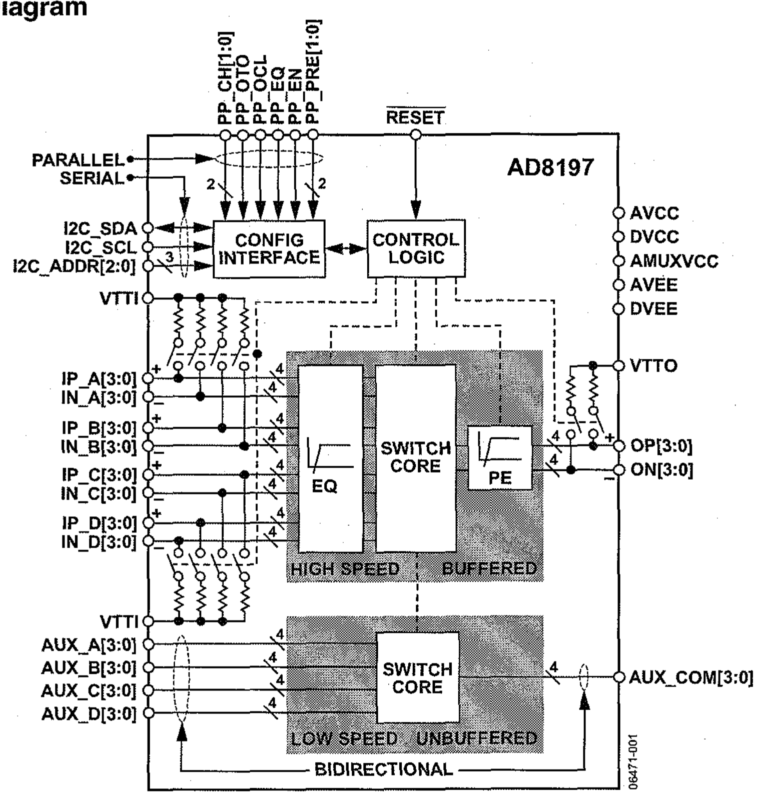
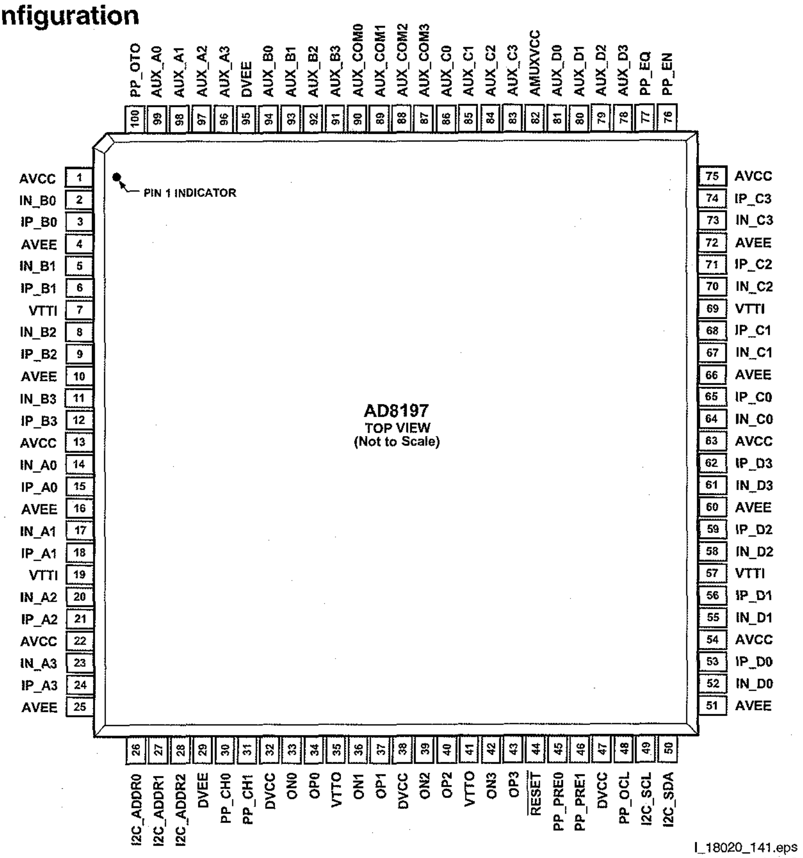
Figure 9-23 Pin configuration

9.11.10 Diagram B08G, AD8197A (IC7E13)

Block Diagram


PP_CH[1:0]
PP_OTO
PP_OCL
PP_EQ
PP_EN
PP_PRE[1:0]
RESET
AD8197
PARALLEL
SERIAL
2
2
I2C_SDA
I2C_SCL
I2C_ADDR[2:0]
3
CONFIG INTERFACE
CONTROL LOGIC
AVCC
DVCC
AMUXVCC
AVEE
DVEE
VTTI
VTTO
IP_A[3:0]
IN_A[3:0]
IP_B[3:0]
IN_B[3:0]
IP_C[3:0]
IN_C[3:0]
IP_D[3:0]
IN_D[3:0]
4
EQ
SWITCH CORE
PE
OP[3:0]
ON[3:0]
HIGH SPEED
BUFFERED
VTTI
AUX_A[3:0]
AUX_B[3:0]
AUX_C[3:0]
AUX_D[3:0]
SWITCH CORE
AUX_COM[3:0]
LOW SPEED
UNBUFFERED
BIDIRECTIONAL
06471-001

Pin Configuration

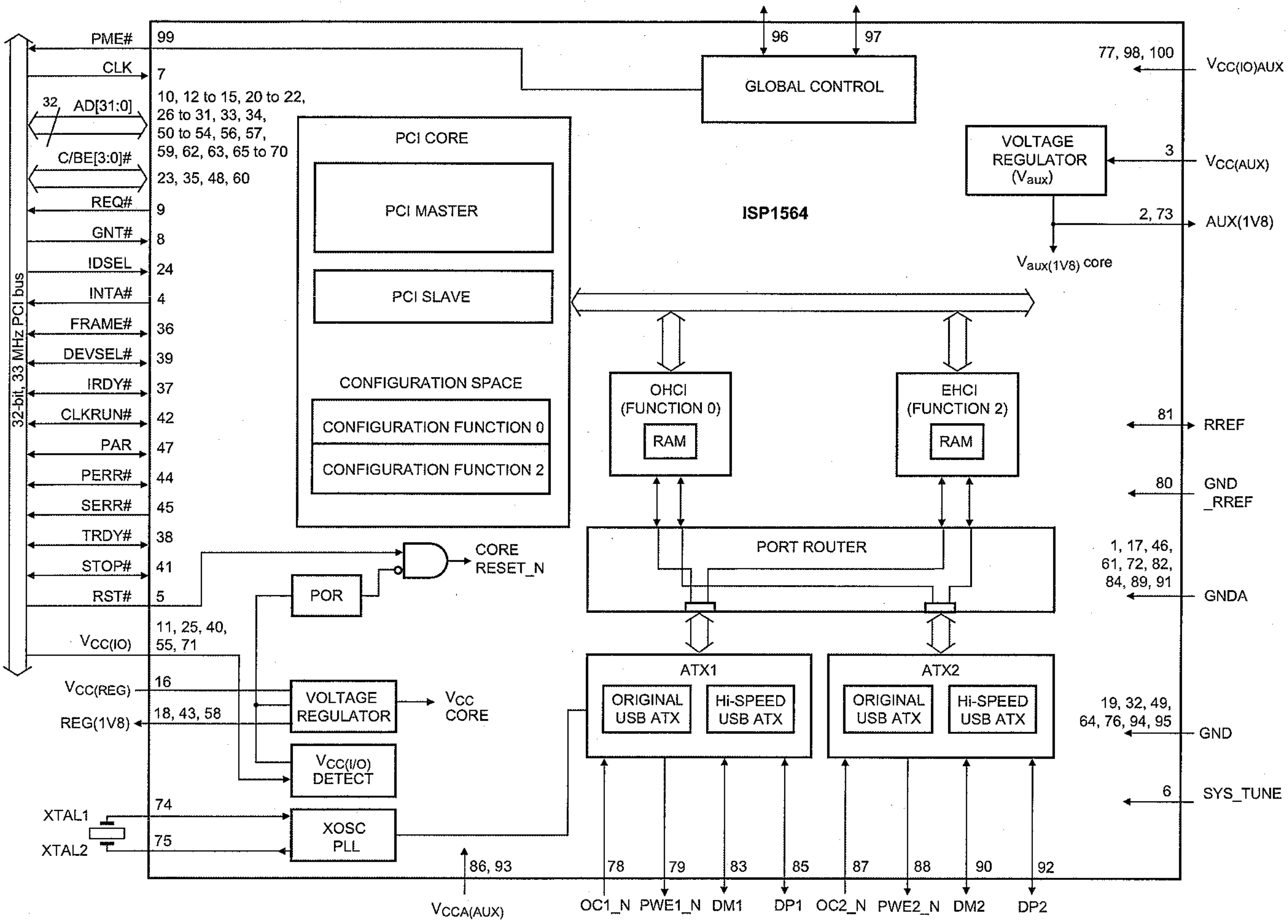

PIN 1 INDICATOR
AD8197
TOP VIEW
(Not to Scale)
1 AVCC
2 IN_B0
3 IP_B0
4 AVEE
5 IN_B1
6 IP_B1
7 VTTI
8 IN_B2
9 IP_B2
10 AVEE
11 IN_B3
12 IP_B3
13 AVCC
14 IN_A0
15 IP_A0
16 AVEE
17 IN_A1
18 IP_A1
19 VTTI
20 IN_A2
21 IP_A2
22 AVCC
23 IN_A3
24 IP_A3
25 AVEE
26 I2C_ADDR0
27 I2C_ADDR1
28 I2C_ADDR2
29 DVEE
30 PP_CH0
31 PP_CH1
32 DVCC
33 ON0
34 OP0
35 VTTO
36 ON1
37 OP1
38 DVCC
39 ON2
40 OP2
41 VTTO
42 ON3
43 OP3
44 RESET
45 PP_PRE0
46 PP_PRE1
47 DVCC
48 PP_OCL
49 I2C_SCL
50 I2C_SDA
51 AVEE
52 IN_D0
53 IP_D0
54 AVCC
55 IN_D1
56 IP_D1
57 VTTI
58 IN_D2
59 IP_D2
60 AVEE
61 IN_D3
62 IP_D3
63 AVCC
64 IN_C0
65 IP_C0
66 AVEE
67 IN_C1
68 IP_C1
69 VTTI
70 IN_C2
71 IP_C2
72 AVEE
73 IN_C3
74 IP_C3
75 AVCC
76 PP_EN
77 PP_EQ
78 AUX_D3
79 AUX_D2
80 AUX_D1
81 AUX_D0
82 AMUXVCC
83 AUX_C3
84 AUX_C2
85 AUX_C1
86 AUX_C0
87 AUX_COM3
88 AUX_COM2
89 AUX_COM1
90 AUX_COM0
91 AUX_B3
92 AUX_B2
93 AUX_B1
94 AUX_B0
95 DVEE
96 AUX_A3
97 AUX_A2
98 AUX_A1
99 AUX_A0
100 PP_OTO

I_18020_141.eps
190908

Figure 9-24 Internal block diagram and pin configuration

9.11.11 Diagram B09A, ISP1564HL (IC 7N00)

Block Diagram


SCL
SDA
96
97
GLOBAL CONTROL
77, 98, 100
$V_{CC(IO)AUX}$
VOLTAGE REGULATOR (V_{aux})
3
$V_{CC(AUX)}$
2, 73
AUX(1V8)
$V_{aux(1V8)}$ core
ISP1564
PCI CORE
PCI MASTER
PCI SLAVE
CONFIGURATION SPACE
CONFIGURATION FUNCTION 0
CONFIGURATION FUNCTION 2
OHCI (FUNCTION 0)
RAM
EHCI (FUNCTION 2)
RAM
PORT ROUTER
ATX1
ORIGINAL USB ATX
Hi-SPEED USB ATX
ATX2
ORIGINAL USB ATX
Hi-SPEED USB ATX
81
RREF
80
GND _RREF
1, 17, 46, 61, 72, 82, 84, 89, 91
GNDA
19, 32, 49, 64, 76, 94, 95
GND
6
SYS_TUNE
32-bit, 33 MHz PCI bus
PME#
99
CLK
7
32
AD[31:0]
10, 12 to 15, 20 to 22, 26 to 31, 33, 34, 50 to 54, 56, 57, 59, 62, 63, 65 to 70
C/BE[3:0]#
23, 35, 48, 60
REQ#
9
GNT#
8
IDSEL
24
INTA#
4
FRAME#
36
DEVSEL#
39
IRDY#
37
CLKRUN#
42
PAR
47
PERR#
44
SERR#
45
TRDY#
38
STOP#
41
RST#
5
CORE RESET_N
POR
$V_{CC(IO)}$
11, 25, 40, 55, 71
$V_{CC(REG)}$
16
VOLTAGE REGULATOR
V_{CC} CORE
REG(1V8)
18, 43, 58
$V_{CC(I/O)}$ DETECT
XTAL1
74
XOSC PLL
XTAL2
75
86, 93
$V_{CCA(AUX)}$
78
79
83
85
87
88
90
92
OC1_N
PWE1_N
DM1
DP1
OC2_N
PWE2_N
DM2
DP2

Pin Configuration

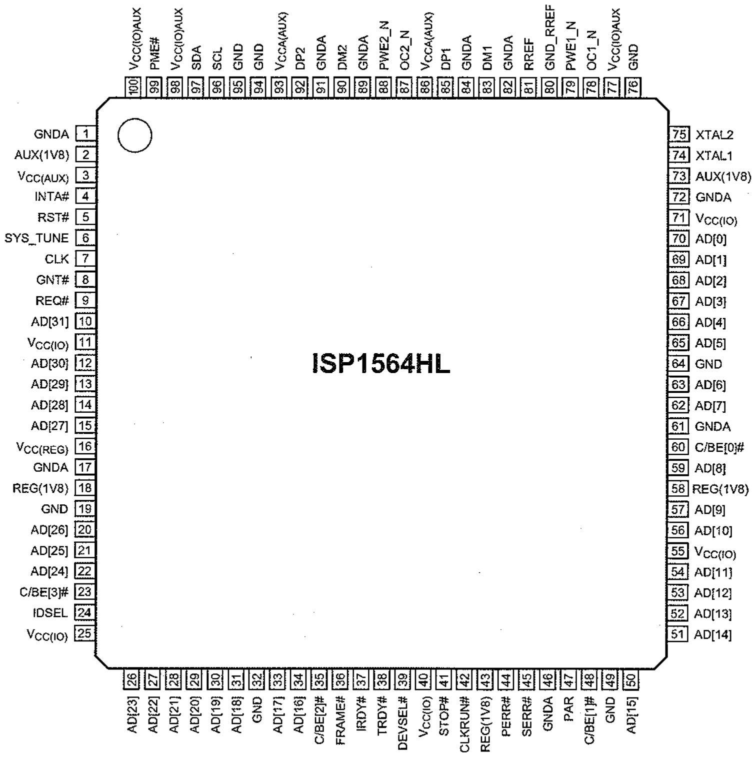

ISP1564HL
100 $V_{CC(IO)AUX}$
99 PME#
98 $V_{CC(IO)AUX}$
97 SDA
96 SCL
95 GND
94 GND
93 $V_{CCA(AUX)}$
92 DP2
91 GNDA
90 DM2
89 GNDA
88 PWE2_N
87 OC2_N
86 $V_{CCA(AUX)}$
85 DP1
84 GNDA
83 DM1
82 GNDA
81 RREF
80 GND_RREF
79 PWE1_N
78 OC1_N
77 $V_{CC(IO)AUX}$
76 GND
GNDA 1
AUX(1V8) 2
$V_{CC(AUX)}$ 3
INTA# 4
RST# 5
SYS_TUNE 6
CLK 7
GNT# 8
REQ# 9
AD[31] 10
$V_{CC(IO)}$ 11
AD[30] 12
AD[29] 13
AD[28] 14
AD[27] 15
$V_{CC(REG)}$ 16
GNDA 17
REG(1V8) 18
GND 19
AD[26] 20
AD[25] 21
AD[24] 22
C/BE[3]# 23
IDSEL 24
$V_{CC(IO)}$ 25
75 XTAL2
74 XTAL1
73 AUX(1V8)
72 GNDA
71 $V_{CC(IO)}$
70 AD[0]
69 AD[1]
68 AD[2]
67 AD[3]
66 AD[4]
65 AD[5]
64 GND
63 AD[6]
62 AD[7]
61 GNDA
60 C/BE[0]#
59 AD[8]
58 REG(1V8)
57 AD[9]
56 AD[10]
55 $V_{CC(IO)}$
54 AD[11]
53 AD[12]
52 AD[13]
51 AD[14]
26 AD[23]
27 AD[22]
28 AD[21]
29 AD[20]
30 AD[19]
31 AD[18]
32 GND
33 AD[17]
34 AD[16]
35 C/BE[2]#
36 FRAME#
37 IRDY#
38 TRDY#
39 DEVSEL#
40 $V_{CC(IO)}$
41 STOP#
42 CLKRUN#
43 REG(1V8)
44 PERR#
45 SERR#
46 GNDA
47 PAR
48 C/BE[1]#
49 GND
50 AD[15]

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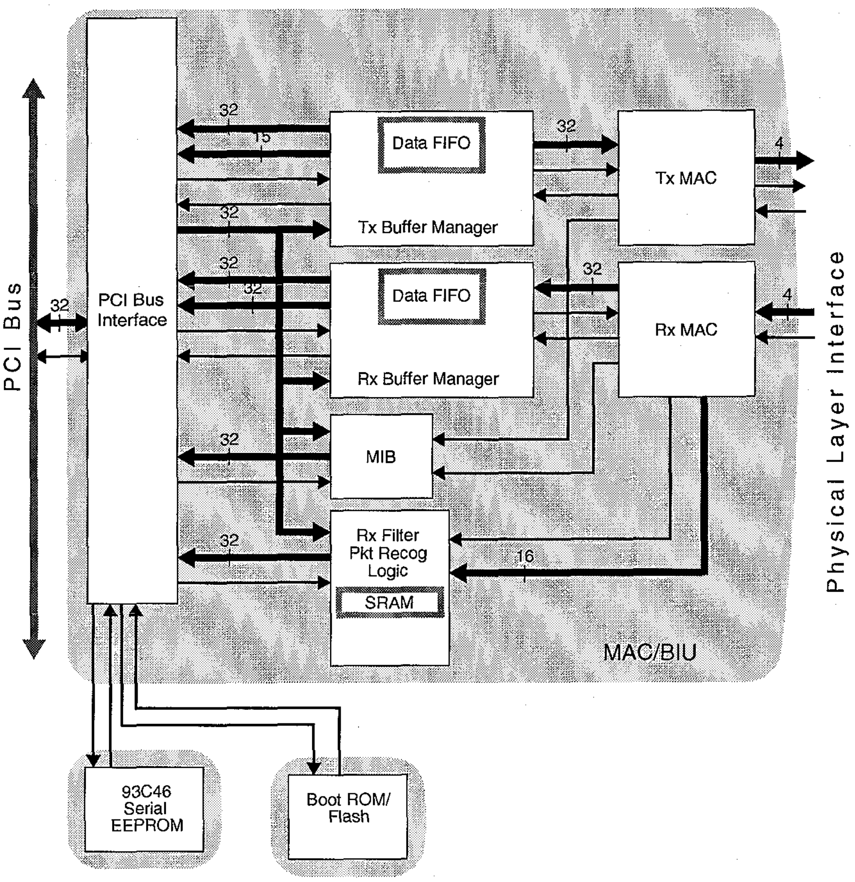
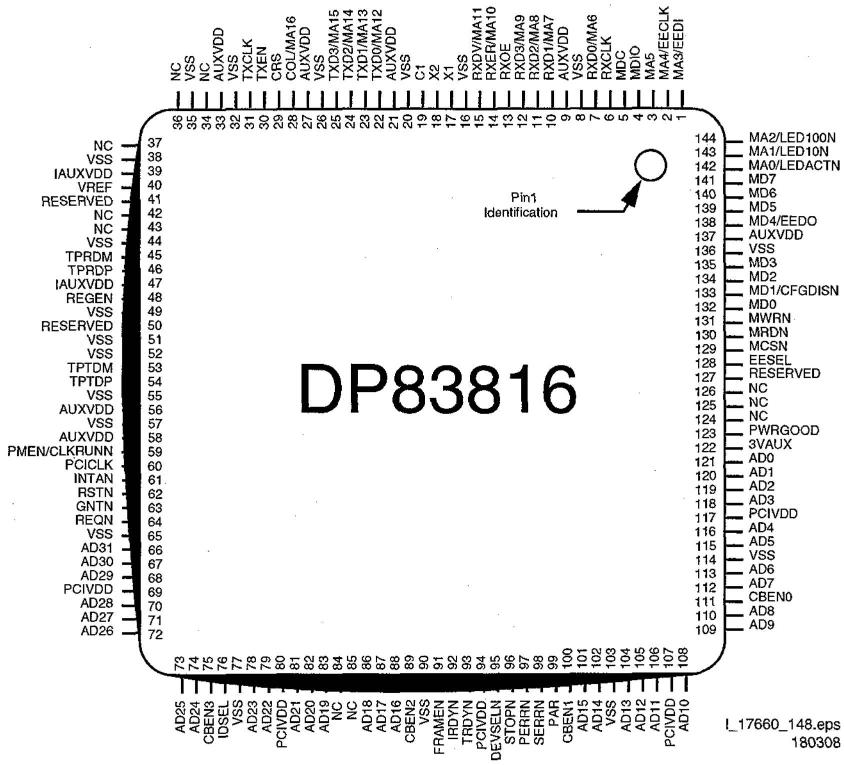
Figure 9-25 Internal block diagram and pin configuration

9.11.12 Diagram B09B, DP83816AVNG (IC7N04)

Block Diagram


PCI Bus
32
PCI Bus Interface
32
15
Data FIFO
Tx Buffer Manager
32
32
32
Data FIFO
Rx Buffer Manager
32
Tx MAC
4
32
Rx MAC
4
32
MIB
32
Rx Filter Pkt Recog Logic
SRAM
16
MAC/BIU
Physical Layer Interface
93C46 Serial EEPROM
Boot ROM/ Flash

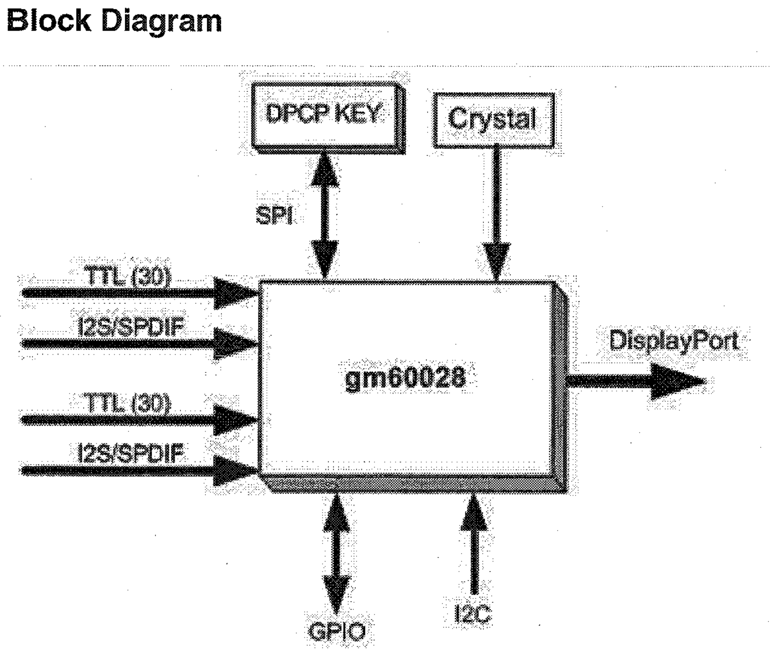
Pin Configuration


NC 36
VSS 35
NC 34
AUXVDD 33
VSS 32
TXCLK 31
TXEN 30
CRS 29
COL/MA16 28
AUXVDD 27
VSS 26
TXD3/MA15 25
TXD2/MA14 24
TXD1/MA13 23
TXD0/MA12 22
AUXVDD 21
VSS 20
C1 19
X2 18
X1 17
VSS 16
RXDV/MA11 15
RXER/MA10 14
RXOE 13
RXD3/MA9 12
RXD2/MA8 11
RXD1/MA7 10
AUXVDD 9
VSS 8
RXD0/MA6 7
RXCLK 6
MDC 5
MDIO 4
MA5 3
MA4/EECLK 2
MA3/EEDI 1
NC 37
VSS 38
IAUXVDD 39
VREF 40
RESERVED 41
NC 42
NC 43
VSS 44
TPRDM 45
TPRDP 46
IAUXVDD 47
REGEN 48
VSS 49
RESERVED 50
VSS 51
VSS 52
TPTDM 53
TPTDP 54
VSS 55
AUXVDD 56
VSS 57
AUXVDD 58
PMEN/CLKRUNN 59
PCICLK 60
INTAN 61
RSTN 62
GNTN 63
REQN 64
VSS 65
AD31 66
AD30 67
AD29 68
PCIVDD 69
AD28 70
AD27 71
AD26 72
AD25 73
AD24 74
CBEN3 75
IDSEL 76
VSS 77
AD23 78
AD22 79
PCIVDD 80
AD21 81
AD20 82
AD19 83
NC 84
NC 85
AD18 86
AD17 87
AD16 88
CBEN2 89
VSS 90
FRAMEN 91
IRDYN 92
TRDYN 93
PCIVDD 94
DEVSELN 95
STOPN 96
PERRN 97
SERRN 98
PAR 99
CBEN1 100
AD15 101
AD14 102
VSS 103
AD13 104
AD12 105
AD11 106
PCIVDD 107
AD10 108
144 MA2/LED100N
143 MA1/LED10N
142 MA0/LEDACTN
141 MD7
140 MD6
139 MD5
138 MD4/EEDO
137 AUXVDD
136 VSS
135 MD3
134 MD2
133 MD1/CFGDISN
132 MD0
131 MWRN
130 MRDN
129 MCSN
128 EESEL
127 RESERVED
126 NC
125 NC
124 NC
123 PWRGOOD
122 3VAUX
121 AD0
120 AD1
119 AD2
118 AD3
117 PCIVDD
116 AD4
115 AD5
114 VSS
113 AD6
112 AD7
111 CBEN0
110 AD8
109 AD9
Pin1 Identification
DP83816

I_17660_148.eps
180308

Figure 9-26 Internal block diagram and pin configuration

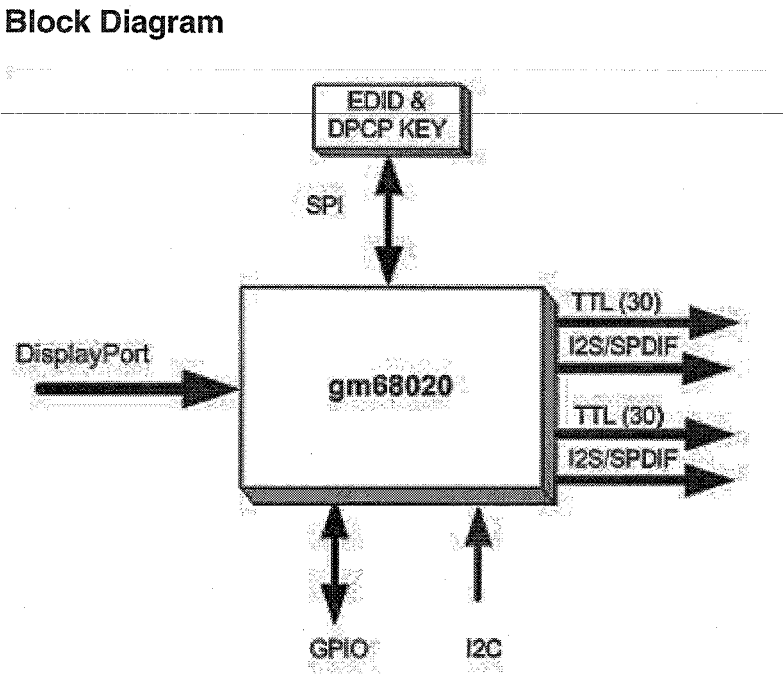
9.11.13 Diagram LD3, GM60028 (IC7300)


Block Diagram
DPCP KEY
Crystal
SPI
TTL (30)
I2S/SPDIF
TTL (30)
I2S/SPDIF
gm60028
DisplayPort
GPIO
I2C

I_18020_138.eps
190908

Figure 9-27 Internal block diagram

9.11.14 Diagram M03B, GM68020 (IC7F0A)

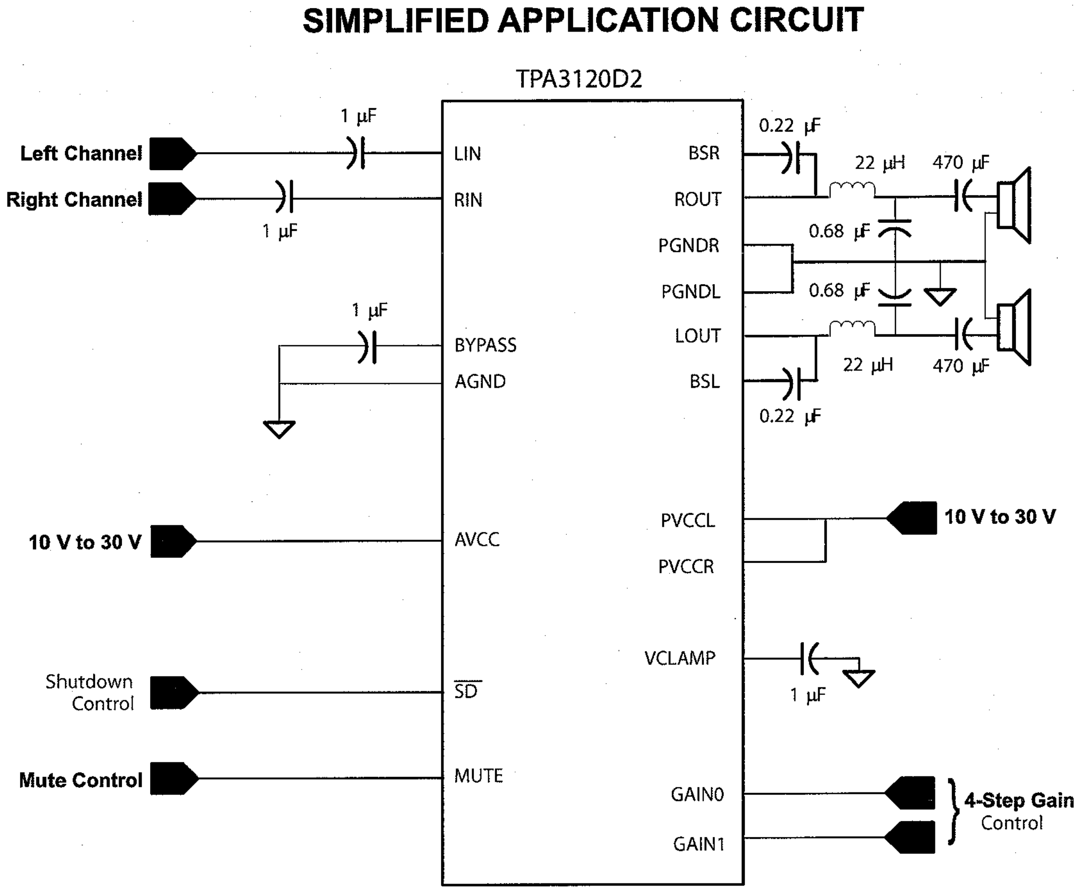

Block Diagram
EDID &
DPCP KEY
SPI
DisplayPort
gm68020
TTL (30)
I2S/SPDIF
TTL (30)
I2S/SPDIF
GPIO
I2C

I_18020_139.eps
190908

Figure 9-28 Internal block diagram

9.11.15 Diagram M02A, TPA3120DP (IC7D10)

Block Diagram


SIMPLIFIED APPLICATION CIRCUIT
TPA3120D2
Left Channel
Right Channel
1 μF
1 μF
1 μF
LIN
RIN
BYPASS
AGND
10 V to 30 V
AVCC
Shutdown Control
SD
Mute Control
MUTE
BSR
ROUT
PGNDR
PGNDL
LOUT
BSL
0.22 μF
22 μH
470 μF
0.68 μF
0.68 μF
22 μH
470 μF
0.22 μF
PVCCL
PVCCR
10 V to 30 V
VCLAMP
1 μF
GAIN0
GAIN1
4-Step Gain Control

Pin Configuration

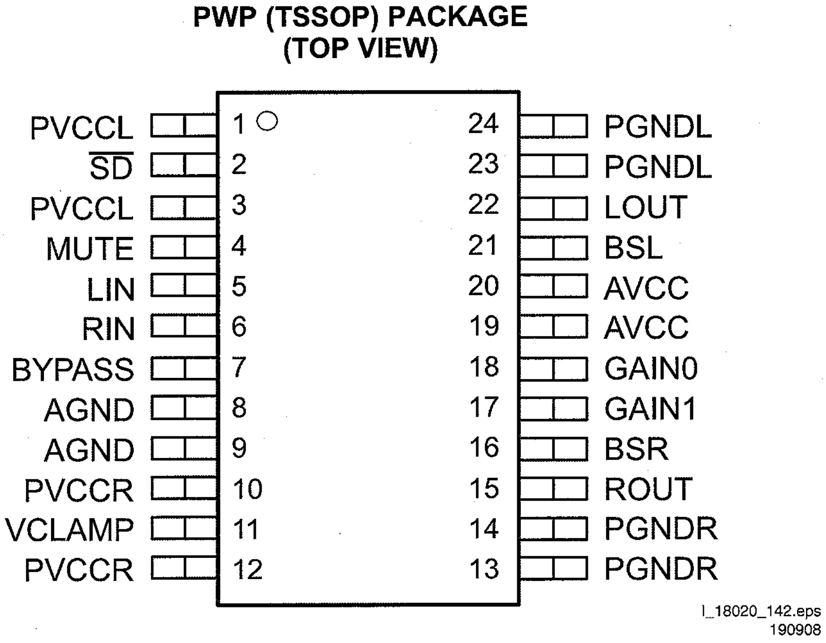
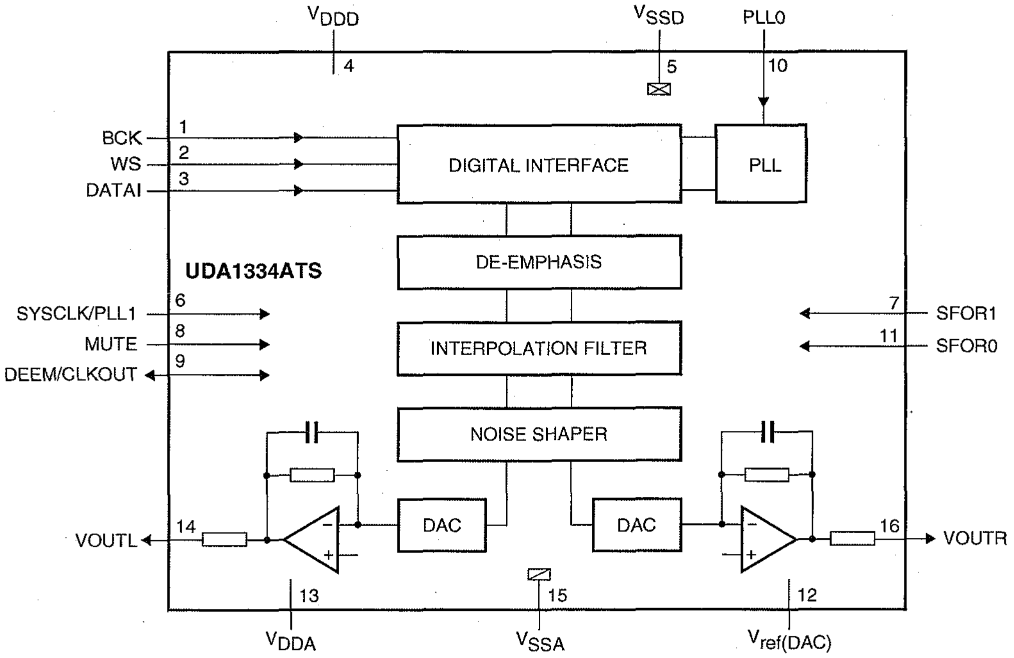

PWP (TSSOP) PACKAGE
(TOP VIEW)
PVCCL 1
SD 2
PVCCL 3
MUTE 4
LIN 5
RIN 6
BYPASS 7
AGND 8
AGND 9
PVCCR 10
VCLAMP 11
PVCCR 12
24 PGNDL
23 PGNDL
22 LOUT
21 BSL
20 AVCC
19 AVCC
18 GAIN0
17 GAIN1
16 BSR
15 ROUT
14 PGNDR
13 PGNDR
I_18020_142.eps
190908

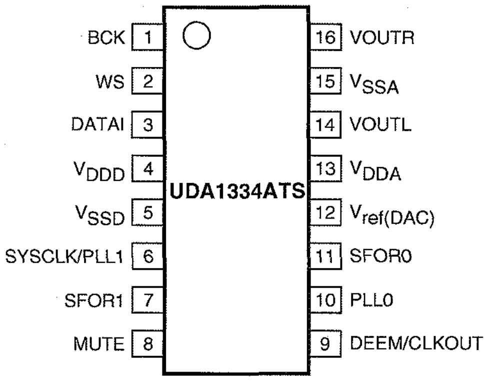
Figure 9-29 Internal block diagram and pin configuration

9.11.16 Diagram M02B, UDA1334 (IC7D53)

Block Diagram


VDDD
VSSD
PLL0
4
5
10
BCK
WS
DATAI
1
2
3
DIGITAL INTERFACE
PLL
DE-EMPHASIS
UDA1334ATS
SYSCLK/PLL1
MUTE
DEEM/CLKOUT
6
8
9
INTERPOLATION FILTER
7
11
SFOR1
SFOR0
NOISE SHAPER
VOUTL
14
DAC
DAC
16
VOUTR
13
15
12
VDDA
VSSA
Vref(DAC)

Pin Configuration


BCK 1
WS 2
DATAI 3
VDDD 4
VSSD 5
SYSCLK/PLL1 6
SFOR1 7
MUTE 8
UDA1334ATS
16 VOUTR
15 VSSA
14 VOUTL
13 VDDA
12 Vref(DAC)
11 SFOR0
10 PLL0
9 DEEM/CLKOUT

G_16860_081.eps
220207

Figure 9-30 Internal block diagram and pin configuration

10. Spare Parts List & CTN Overview

For the latest spare part overview, please consult the Philips Service website.

Table 10-1 Sets described in this manual:

CTN	Styling	Published in:
42PES0001D/10	Essence	3122 785 18020
42PES0001H/10	Essence	3122 785 18020

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- **All Chapters:** various textual changes.
- **Chapter 1:** Specification of SCART connectors changed, specification of HDMI connectors changed.
- **Chapter 4:** Instructions for LCD Panel replacement changed; introduction of one Spare Part Service Kit.
- **Chapter 5:** Contents of CSM changed to reflect current situation.
- **Chapter 8:** Contents of Service Options changed to reflect current situation.